LAMPIRAN A
PROGRAM PADA PENGONTROL MIKRO ATMEGA8535
PROGRAM UTAMA

//***************Program dengan metode space shift code***************
.include "c:\appnotes\m8535def.inc"
.org 0x0000
.def temp=r16
.def count=r17
.def data=r18
.def test1=r19
.def time=r20
.equ startcutoff=21 ;2,688 ms
.equ bit0cutoff=7 ;0,896 ms
.equ bit1cutoff=18 ;2,304 ms
.equ bit2cutoff=13 ;1,664 ms
.equ bit3cutoff=5 ;0,64 ms
.equ bit4cutoff=3 ;0,384 ms
.equ num1=0x80
.equ num2=0x81
.equ num3=0x82
.equ num4=0x83
.equ num5=0x84
.equ num6=0x85
.equ num7=0x86
.equ num8=0x87
.equ num9=0x88
.equ num0=0x89
.equ timer_value=0xf0fa
rjmp reset
reset:
  ldi temp,low(ramend)
  out spl,temp
  ldi temp,high(ramend)
  out sph,temp

  // inisialisasi i/o dan timer
  ldi temp,0xff
out ddrb,temp
out ddra,temp
ldi temp,0x00
out portb,temp
out porta,temp
out ddrc,temp
ldi temp,0x01
out portc,temp
ldi temp,0b00000101
out tccr0,temp;set prescaler 1024

// toggle switch
mainer:
ldi test1,0

main0:
sbr test1,0
main1:
sbr test1,1

main2:
sbr test1,1
main3:
sbr test1,2

main4:
sbr test1,2
main5:
sbr test1,4

main6:
sbr test1,3
main7:
sbr test1,8

// delay_132ms
ldi temp,0b00000100
out timsk,temp
ldi temp, high(timer_value)
out tcnt1h, temp
ldi temp, low(timer_value)
out tcnt1l, temp
ldi temp, 0b00000101
out tccr1b, temp

looptimer:
in r20, tifr
sbrs r20, tov1
rjmp looptimer
ldi temp, 0b00000100
out tifr, temp

// deteksi dan baca start bit
main:
sbic pinc, 0; wait for start bit
rjmp main

ldi temp, 0
out tcnt0, temp

parta:
sbis pinc, 0
rjmp parta

in temp, tcnt0
cpi temp, startcutoff; test pulse size
brlo partb
rjmp main

partb:
cpi temp, bit1cutoff
breq main
brge partc
rjmp main
// deteksi dan baca data
partc: ;decoding subroutine
ldi count,8;counting
clr data

partd:
sbic pinc,0
rjmp partd

ldi temp,0
out tcnt0,temp

parte:
sbis pinc,0
rjmp parte

in temp,tcnt0
cpi temp,bit2cutoff
brlo partf
rjmp main

partf:
cpi temp,bit0cutoff
brlo partg
lsr data
sbr data,128
dec count
breq check_data ;all data received
rjmp partd ;or continue decoding

partg:
cpi temp,bit3cutoff
breq main
brge main
cpi temp,bit4cutoff
breq main
brge selang1
brlo main
selang1:
lsr data
cbr data,128
dec count
breq check_data ;all data received
rjmp partd ;or continue decoding

check_data:
cpi data,num1
breq onlight0
cpi data,num2
breq onlight1
cpi data,num3
breq onlight2
cpi data,num4
breq onlight3
cpi data,num9
breq onlight4
cpi data,num0
breq onlight5
rjmp main0

onlight0:
 sbrc test1,0
 rjmp lamp0_off
 sbi portb,0 ;lamp1_on
 rjmp main1
lamp0_off:
cbi portb,0 ;lamp1_off
 cbr test1,1
 rjmp main0

onlight1:
 sbrc test1,1
 rjmp lamp1_off
 sbi portb,1 ;lamp2_on
 rjmp main3
lamp1_off:
cbi portb,1         ;lamp2_off
cbr test1,2
rjmp main2

onlight2:
 sbrc test1,2
 rjmp lamp2_off
 sbi portb,2         ;lamp3_on
 rjmp main5
lamp2_off:
cbi portb,2         ;lamp3_off
cbr test1,4
rjmp main4

onlight3:
 sbrc test1,3
 rjmp lamp3_off
 sbi portb,3         ;lamp4_on
 rjmp main7
lamp3_off:
cbi portb,3         ;lamp4_off
cbr test1,8
rjmp main6

onlight4:
 clr temp
 out portb,temp      ;all_lamp_off
 rjmp mainer

onlight5:
 ser temp
 out portb,temp      ;all_lamp_on
 ldi test1,0xff
 rjmp main0
//*******************Program Metode Pulse Shift Code*******************
.include "c:\appnotes\m8535def.inc"
.org 0x0000
.def temp=r16
.def count=r17
.def count1=r24
.def data=r18
.def test1=r19
.def time=r20
.def data1=r21
.def data2=r22
.def data3=r23
.equ startcutoff=26 ;3,328 ms
.equ bit0cutoff=17 ;2,176 ms
.equ bit1cutoff=23 ;2,944 ms
.equ bit2cutoff=21 ;2,688 ms
.equ bit3cutoff=7 ;0,896 ms
.equ bit4cutoff=3 ;0,384 ms
.equ timer_value=0xf0fa
rjmp reset
reset:
  ldi temp,low(ramend)
  out spl,temp
  ldi temp,high(ramend)
  out sph,temp
start:
  ldi temp,0xff
  out ddb,temp
  out dda,temp
  ldi temp,0x00
  out portb,temp
  out porta,temp
  out ddc,temp
  ldi temp,0xff
  out portc,temp
  ldi temp,0b00000101
  out tccr0,temp
mainer:
  ldi test1,0

  //toggle switch
  main0:
    sbrc test1,0

  main1:
    sbr test1,1

  main2:
    sbrc test1,1
    main3:
    sbr test1,2

  main4:
    sbrc test1,2
    main5:
    sbr test1,4

  main6:
    sbrc test1,3
    main7:
    sbr test1,8

  // delay 132_ms
  ldi temp,0b00000100
  out timsk,temp
  ldi temp,high(timer_value)
  out tcnt1h,temp
  ldi temp,low(timer_value)
  out tcnt1l,temp
  ldi temp,0b00000101
  out tccr1b,temp

  looptimer:
in r20,tifr
sbrs r20,tov1
rjmp looptimer
ldi temp,0b00000100
out tifr,temp

//deteksi dan baca start bit
main:
sbic pinc,0;wait for start bit
rjmp main

parta:
sbis pinc,0
rjmp parta

ldi temp,0
out tcnt0,temp

clear:
sbic pinc,0
rjmp clear

in temp,tcnt0
cpi temp,startcutoff;test pulse size
brlo partb
rjmp main

partb:
cpi temp,bit1cutoff
breq main
brge partc
rjmp main

// deteksi dan baca 22 bit
partc::decoding subroutine
ldi count1,0
repeat:
ldi count,8;counting
clr data

partd:
    sbis pinc,0
    rjmp partd

    in temp,tcnt0
    cpi temp,bit2cutoff
    brlo partf
    rjmp main

    in temp,tcnt0
    cpi temp,bit0cutoff
    brlo partf
    rjmp main

    in temp,tcnt0
    cpi temp,bit3cutoff
    brge main
    cpi temp,bit4cutoff
    brlo main
    lsr data
    sbr data,128
    inc count1
    cpi count1,22
    breq partm
    dec count
    breq parth ;all data received
    rjmp partd ;or continue decoding

    in temp,tcnt0
    cpi temp,bit3cutoff
    brge main
    cpi temp,bit4cutoff
    brlo main
    lsr data
    sbr data,128
    inc count1
cpi count1,22
breq partm
dec count
breq parth ;all data received
rjmp partd ;or continue decoding

parth:;decoding subroutine
cpi count1,8
breq finished_data1
cpi count1,16
breq finished_data2
rjmp main
finished_data1:
mov data1,data
rjmp repeat
finished_data2:
mov data2,data
rjmp repeat

partm:
mov data3,data

cpi data1,0x00
breq a
cpi data1,0x40
breq b
cpi data1,0x20
breq c
cpi data1,0x60
breq d
cpi data1,0x80
breq e
cpi data1,0xa0
breq f
rjmp main

a:
cpi data2,0xfa
breq p1
rjmp main

b:
cpi data2,0xfa
breq p2
rjmp main

c:
cpi data2,0xfa
breq p3
rjmp main

d:
cpi data2,0xfa
breq p4
rjmp main

e:
cpi data2,0xfa
breq p5
rjmp main

f:
cpi data2,0xfa
breq p6
rjmp main

p1: //tombol 1
cpi data3,0xbc
breq onlight0
rjmp main
p3: //tombol 3
cpi data3,0xb8
breq onlight1
rjmp main
p2: //tombol 2
cpi data3,0xb4
breq onlight2
rjmp main
p4:       //tombol 4
cpi data3,0xb0
breq onlight3
rjmp main
p5:       //tombol5
cpi data3,0xac
breq onlight4
rjmp main
p6:       //tombol6
cpi data3,0xa8
breq onlight5
rjmp main

onlight0:
sbrc test1,0
rjmp lamp0_off
sbi portb,0   ;lamp1_on
rjmp main1
lamp0_off:
cbi portb,0   ;lamp1_off
cbr test1,1
rjmp main0

onlight1:
sbrc test1,1
rjmp lamp1_off
sbi portb,1   ;lamp2_on
rjmp main3
lamp1_off:
cbi portb,1   ;lamp2_off
cbr test1,2
rjmp main2

onlight2:
sbrc test1,2
rjmp lamp2_off
sbi portb,2 ;lamp3_on
rjmp main5
lamp2_off:
cbi portb,2 ;lamp3_off
cbr test1,4
rjmp main4

onlight3:
sbrc test1,3
rjmp lamp3_off
sbi portb,3 ;lamp4_on
rjmp main7
lamp3_off:
cbi portb,3 ;lamp4_off
cbr test1,8
rjmp main6

onlight4:
clr temp
out portb,temp ;all_lamp_off
rjmp mainer

onlight5:
ser temp
out portb,temp ;all_lamp_on
ldi test1,0xff
rjmp main0
LAMPIRAN B
DATA SHEET IR – 8510
NOTES:
1. This drawing measure is a standard value. All dimensions are in millimeter.
2. In case of designation is tolerance ± 0.3mm.
3. Lead spacing is measured where the lead emerge from the package.
4. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
5. These specification sheets include materials protected under copyright of EVERLIGHT corporation. Please don’t reproduce or cause anyone to reproduce them without EVERLIGHT consent.
6. When using this produce, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
Description:
1. The module is a small type infrared remote control system receiver which has been developed and designed by utilizing the latest hybrid technology.
2. This single unit type module incorporates a photo diode and a receiving preamplifier IC.
3. The demodulated output signal can directly be decoded by a microprocessor.

Feature:
1. High protection ability to EMI and metal case can be customized.
2. Mold type and metal case type to meet the design of front panel.
3. Elliptic lens to improve the characteristic against
4. Line-up for various center carrier frequencies.
5. Low voltage and low power consumption.
6. High immunity against ambient light.
7. Photodiode with integrated circuit.
8. TTL and CMOS compatibility.

Application:
1. Optical switch
2. Light detecting portion of remote control
   - AV instruments such as Audio, TV, VCR, CD, MD, etc.
   - Home appliances such as Air-conditioner, Fan, etc.
   - The other equipments with wireless remote control.
   - CATV set top boxes
   - Multi-media Equipment
### Absolute maximum ratings:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
<th>Notice</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>4.3~5.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>Topr</td>
<td>-10~+60</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-20~+70</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Soldering Temperature</td>
<td>Tsol</td>
<td>260</td>
<td>°C</td>
<td>4mm from mold body less than 5 seconds</td>
</tr>
</tbody>
</table>

### Electro Optical Characteristics:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>4.7</td>
<td>5</td>
<td>5.3</td>
<td>V</td>
<td>DC voltage</td>
</tr>
<tr>
<td>Supply Current</td>
<td>lcc</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>mA</td>
<td>No signal input</td>
</tr>
<tr>
<td>B.P.F Center Frequency</td>
<td>fo</td>
<td>-</td>
<td>37.9</td>
<td>-</td>
<td>KHz</td>
<td></td>
</tr>
<tr>
<td>Peak Wavelength</td>
<td>λp</td>
<td>-</td>
<td>940</td>
<td>-</td>
<td>nm</td>
<td></td>
</tr>
<tr>
<td>Transmission Distance</td>
<td>L₀</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>m</td>
<td>At the ray axis *1</td>
</tr>
<tr>
<td></td>
<td>L₄5</td>
<td>2.5</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Half Angle</td>
<td>θ</td>
<td>-</td>
<td>45</td>
<td>-</td>
<td>deg</td>
<td>At the ray axis *2</td>
</tr>
<tr>
<td>High Level Pulse Width</td>
<td>Tₜ</td>
<td>400</td>
<td>-</td>
<td>800</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>Low Level Pulse Width</td>
<td>Tₗ</td>
<td>400</td>
<td>-</td>
<td>800</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>Vₜ</td>
<td>4.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>Vₗ</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

*1: The ray receiving surface at a vertex and relation to the ray axis in the range of φ = 0° and φ = 45°.

*2: A range from 30cm to the arrival distance. Average value of 50 pulses.
TEST METHOD:

The specified electro-optical characteristics is satisfied under the following Conditions at the controllable distance.

① Measurement place
   A place that is nothing of extreme light reflected in the room.

② External light
   Project the light of ordinary white fluorescent lamps which are not high Frequency lamps and must be less than 10 Lux at the module surface. (Ee ≤ 10Lux)

③ Standard transmitter
   A transmitter whose output is so adjusted as to \( V_o = 400 \text{mVp-p} \) and the output Wave form shown in Fig.-1. According to the measurement method shown in Fig.-2 the standard transmitter is specified. However, the infrared photodiode to be used for the transmitter should be \( \lambda_p = 940 \text{nm} \), \( \Delta \lambda = 50 \text{nm} \). Also, photo diode is used of PD438B (\( V_E = 5V \)).
   (Standard light / Light source temperature 2856°K).

④ Measuring system
   According to the measuring system shown in Fig.-3
Module schematic & circuit:

Fig.-1 Transmitter Wave Form

- Carrier frequency is adjusted to center frequency of each product.
- Output Pulse of Device
- Duty = 0.5

Fig.-2 Measuring Method

Fig.-3 Measuring System

\[ \text{Duty} = 0.5 \]
### Reliability test item and condition:
The reliability of products shall be satisfied with items listed below.

**Confidence level:** 90%

**LTPD:** 10%

<table>
<thead>
<tr>
<th>Test Items</th>
<th>Test Conditions</th>
<th>Failure Judgement Criteria</th>
<th>Samples(n)</th>
<th>Defective(c)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation life</td>
<td>Vcc=5V, Ta:25°C 1000hrs</td>
<td></td>
<td>n=22, c=0</td>
<td></td>
</tr>
</tbody>
</table>
| Temperature cycle           | 1 cycle -20°C +25°C +70°C (30min) 5min (30min) 50 cycle test | $L_0 \leq L_x 0.8$  
$L_{as} \leq L_x 0.8$ | n=22, c=0  |              |
| Thermal shock               | -10°C to +70°C (5min) (10sec) (5min) 50 cycle test |                           | n=22, c=0  |              |
| High temperature storage    | Temp: +70°C 1000hrs              |                           | n=22, c=0  |              |
| Low temperature storage     | Temp: -20°C 1000hrs              |                           | n=22, c=0  |              |
| High temperature High humidity | Ta: 85°C RH 85% 1000hrs          | L: Lower specification limit | n=22, c=0  |              |
| Solder heat                 | Temp: 260±5°C 5sec 4mm Form the bottom of the package |                           | n=22, c=0  |              |
| Solderability               | Temp: 230±5°C 5sec 4mm Form the bottom of the package | More than 90% of Lead to be covered by soldering | n=22, c=0  |              |
LAMPIRAN C
DATA SHEET ULN – 2803
EIGHT DARLINGTON ARRAYS

- Eight Darlington transistors with common emitters
- Output current to 500 mA
- Output voltage to 50 V
- Integral suppression diodes
- Versions for all popular logic families
- Output can be paralleled
- Inputs pinned opposite outputs to simplify board layout

DESCRIPTION
The ULN2801A-ULN2805A each contain eight Darlington transistors with common emitters and integral suppression diodes for inductive loads. Each Darlington features a peak load current rating of 600 mA (500 mA continuous) and can withstand at least 50 V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families: the ULN2801A is designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5 kΩ input resistor and zener for 14-25 V PMOS; the ULN2803A has a 2.7 kΩ input resistor for 5 V TTL and CMOS; the ULN2804A has a 10.5 kΩ input resistor for 6-15 V CMOS and the ULN2805A is designed to sink a minimum of 300 mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copper lead frame and feature the convenient input-opposite output pinout to simplify board layout.

September 1997
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_o$</td>
<td>Output Voltage</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>$V_i$</td>
<td>Input Voltage</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>for ULN2802A, ULN2803A, ULN2804A</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>for ULN2805A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_C$</td>
<td>Continuous Collector Current</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Continuous Base Current</td>
<td>25</td>
<td>mA</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>Power Dissipation</td>
<td>1.0</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>(one Darlington pair)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(total package)</td>
<td>2.25</td>
<td></td>
</tr>
<tr>
<td>$T_{emb}$</td>
<td>Operating Ambient Temperature Range</td>
<td>-20 to 85</td>
<td>ºC</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>Storage Temperature Range</td>
<td>-55 to 150</td>
<td>ºC</td>
</tr>
<tr>
<td>$T_{j}$</td>
<td>Junction Temperature Range</td>
<td>-20 to 150</td>
<td>ºC</td>
</tr>
</tbody>
</table>

### THERMAL DATA

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th-j-amb}$</td>
<td>Thermal Resistance Junction-ambient</td>
<td>Max.</td>
<td>55</td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS (Tamb = 25ºC unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Fig.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CEX}$</td>
<td>Output Leakage Current</td>
<td>$V_{CE} = 500V$</td>
<td>50</td>
<td>100</td>
<td>µA</td>
<td>1a</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_{amb} = 70ºC, V_i = 50V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{BE} = 50V, V_i = 6V$</td>
<td>500</td>
<td>µA</td>
<td></td>
<td>1b</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>for ULN2804A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BE}$</td>
<td>Collector-emitter Saturation Voltage</td>
<td>$I_C = 100mA, I_E = 250µA$</td>
<td>0.9</td>
<td>1.1</td>
<td>1.3</td>
<td>V</td>
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<td>$I_C = 200mA, I_E = 50µA$</td>
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<td>1.3</td>
<td>1.6</td>
<td>V</td>
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<td>$I_C = 350mA, I_E = 50µA$</td>
<td>1.3</td>
<td>1.6</td>
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<tr>
<td>$I_{(on)}$</td>
<td>Input Current</td>
<td>for ULN2802A</td>
<td>0.82</td>
<td>1.25</td>
<td>mA</td>
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<td></td>
<td></td>
<td>for ULN2803A</td>
<td>0.93</td>
<td>1.35</td>
<td>mA</td>
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<td></td>
<td></td>
<td>for ULN2804A</td>
<td>0.36</td>
<td>0.5</td>
<td>mA</td>
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<td></td>
<td></td>
<td>$V_i = 5V$</td>
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<td>for ULN2805A</td>
<td>1.145</td>
<td>1.45</td>
<td>mA</td>
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<td></td>
<td>$V_i = 3V$</td>
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<td>$I_{off}$</td>
<td>Input Current</td>
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<td>15</td>
<td>65</td>
<td>µA</td>
<td>4</td>
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<td>$V_{(on)}$</td>
<td>Input Voltage</td>
<td>$V_{CE} = 2V$</td>
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<td>for ULN2802A</td>
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<td>$I_C = 300mA$</td>
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<td></td>
<td>for ULN2803A</td>
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<tr>
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<td>for ULN2804A</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>for ULN2805A</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 350mA$</td>
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<tr>
<td>$I_F$</td>
<td>DC Forward Current Gain</td>
<td>for ULN2801A</td>
<td>1000</td>
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<td>–</td>
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</tr>
<tr>
<td>$C_i$</td>
<td>Input Capacitance</td>
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<td>15</td>
<td>25</td>
<td>pF</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>$t_{on}$</td>
<td>Turn-on Delay Time</td>
<td>$0.5 V_i, 0.5 V_o$</td>
<td>0.25</td>
<td>1</td>
<td>µs</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-off Delay Time</td>
<td>$0.5 V_i, 0.5 V_o$</td>
<td>0.25</td>
<td>1</td>
<td>µs</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>$I_{cl}$</td>
<td>Clamp Diode Leakage Current</td>
<td>$V_R = 50V$</td>
<td>50</td>
<td>µA</td>
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<td>6</td>
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<tr>
<td></td>
<td></td>
<td>$T_{amb} = 70ºC, V_R = 50V$</td>
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<tr>
<td>$V_{cl}$</td>
<td>Clamp Diode Forward Voltage</td>
<td>$I_R = 350mA$</td>
<td>1.7</td>
<td>2</td>
<td>V</td>
<td>7</td>
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</table>
Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-Programmable Flash
  - Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
  - In-System Programming by On-chip Boot Program
  - True Read-While-Write Operation
  - 512 Bytes EEPROM
  - Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 6-channel, 10-bit ADC
  - 8 Single-ended Channels
  - 7 Differential Channels for TOFF Package Only
  - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x for TOFF Package Only
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega8535
  - 4.5 - 5.5V for ATmega8535L
- Speed Grades
  - 0 - 8 MHz for ATmega8535L
  - 0 - 16 MHz for ATmega8535

Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.
Pin Configurations

Figure 1. Pinout ATmega8535

NOTE: MLP Bottom pad should be soldered to ground.

Disclaimer

Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.
Overview

The ATmega8535 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the ATmega8535 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram
The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughput up to ten times faster than conventional CISC microcontrollers.

The ATmega8535 provides the following features: 8k bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain in TQFP package, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main oscillator and the asynchronous timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8535 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega8535 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

### AT90S8535 Compatibility

The ATmega8535 provides all the features of the AT90S8535. In addition, several new features are added. The ATmega8535 is backward compatible with AT90S8535 in most cases. However, some incompatibilities between the two microcontrollers exist. To solve this problem, an AT90S8535 compatibility mode can be selected by programming the S8535C fuse. ATmega8535 is pin compatible with AT90S8535, and can replace the AT90S8535 on current Printed Circuit Boards. However, the location of fuse bits and the electrical characteristics differs between the two devices.

Programming the S8535C fuse will change the following functionality:

- The timed sequence for changing the Watchdog Time-out period is disabled. See "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 43 for details.
- The double buffering of the USART Receive Register is disabled. See "AVR USART vs. AVR UART – Compatibility" on page 143 for details.
Pin Descriptions

$V_{CC}$  
Digital supply voltage.

$GND$  
Ground.

Port A (PA7..PA0)  
Port A serves as the analog inputs to the A/D Converter. Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B (PB7..PB0)  
Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port B also serves the functions of various special features of the ATmega8535 as listed on page 58.

Port C (PC7..PC0)  
Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D (PD7..PD0)  
Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmega8535 as listed on page 62.

RESET  
Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 39. Shorter pulses are not guaranteed to generate a reset.

XTAL1  
Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2  
Output from the inverting Oscillator amplifier.

AVCC  
AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to $V_{CC}$ even if the ADC is not used. If the ADC is used, it should be connected to $V_{CC}$ through a low-pass filter.

AREF  
AREF is the analog reference pin for the A/D Converter.
### Register Summary

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Page</th>
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<tr>
<td>000000</td>
<td>SFR0</td>
<td>I</td>
<td>T</td>
<td>H</td>
<td>S</td>
<td>V</td>
<td>N</td>
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</tbody>
</table>

**Note:**
- **Address**—Address of the register in memory.
- **Name**—Name of the register.
- **Bit 7**—Bit 7 of the register.
- **Bit 6**—Bit 6 of the register.
- **Bit 5**—Bit 5 of the register.
- **Bit 4**—Bit 4 of the register.
- **Bit 3**—Bit 3 of the register.
- **Bit 2**—Bit 2 of the register.
- **Bit 1**—Bit 1 of the register.
- **Bit 0**—Bit 0 of the register.
- **Page**—Page number in the document.
### Register Summary (Continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
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Notes:
1. Refer to the USART description for details on how to access UBRRH and UCSRC.
2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.