Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

Pin Configurations

(continued)
The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

Vcc
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups.

Port 2 also serves the functions of various special features of the AT89C51 as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVOC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN
Program Store Enable is the read strobe to external program memory.
When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP
External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Oscillator Characteristics
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Status of External Pins During Idle and Power Down Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Program Memory</th>
<th>ALE</th>
<th>PSEN</th>
<th>PORT0</th>
<th>PORT1</th>
<th>PORT2</th>
<th>PORT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>Internal</td>
<td>1</td>
<td>1</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Idle</td>
<td>External</td>
<td>1</td>
<td>1</td>
<td>Float</td>
<td>Data</td>
<td>Address</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>Internal</td>
<td>0</td>
<td>0</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Power Down</td>
<td>External</td>
<td>0</td>
<td>0</td>
<td>Float</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
</tbody>
</table>

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

![Oscillator Connections Diagram](image1)

Note: C1, C2 = 30 pF ± 10 pF for Crystals  
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration

![External Clock Drive Configuration Diagram](image2)
Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before Vcc is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Lock Bit Protection Modes

<table>
<thead>
<tr>
<th>Program Lock Bits</th>
<th>Protection Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB1</td>
<td>LB2</td>
</tr>
<tr>
<td>1</td>
<td>U</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
</tr>
<tr>
<td>3</td>
<td>P</td>
</tr>
<tr>
<td>4</td>
<td>P</td>
</tr>
</tbody>
</table>

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of EA be in agreement with the current logic level at that pin in order for the device to function properly.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (VCC) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user’s system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

<table>
<thead>
<tr>
<th>Top-Side Mark</th>
<th>VPP = 12V</th>
<th>VPP = 5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT89C51 xxxx</td>
<td>AT89C51 xxxx</td>
<td></td>
</tr>
<tr>
<td>yyyy</td>
<td>yyyy-5 yyyy</td>
<td></td>
</tr>
<tr>
<td>Signature</td>
<td>(030H)=1EH  (030H)=1EH</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(031H)=51H  (031H)=51H</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(032H)=FFH  (032H)=FFH</td>
<td></td>
</tr>
</tbody>
</table>

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/VPP to 12V for the high-voltage programming mode.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.
Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all “1”s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows:

- \( (030H) = 1EH \) indicates manufactured by Atmel
- \( (031H) = 51H \) indicates 89C51
- \( (032H) = FFH \) indicates 12V programming
- \( (032H) = 05H \) indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>RST</th>
<th>PSEN</th>
<th>ALE/PROG</th>
<th>EA/V&lt;sub&gt;pp&lt;/sub&gt;</th>
<th>P2.6</th>
<th>P2.7</th>
<th>P3.6</th>
<th>P3.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Code Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Read Code Data</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Write Lock</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit - 1</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Bit - 2</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Bit - 3</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Chip Erase</td>
<td>H</td>
<td>L</td>
<td>(1)</td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Read Signature Byte</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

Note: 1. Chip Erase requires a 10-ms PROG pulse.
Flash Programming and Verification Characteristics

$T_A = 0^\circ C$ to $70^\circ C$, $V_{CC} = 5.0 \pm 10\%$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{PP}^{(1)}$</td>
<td>Programming Enable Voltage</td>
<td>11.5</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{PP}^{(1)}$</td>
<td>Programming Enable Current</td>
<td>1.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$1/t_{CLCL}$</td>
<td>Oscillator Frequency</td>
<td>3</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{AVGL}$</td>
<td>Address Setup to PROG Low</td>
<td></td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{GHAX}$</td>
<td>Address Hold After PROG</td>
<td></td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{DVGL}$</td>
<td>Data Setup to PROG Low</td>
<td></td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{GHDX}$</td>
<td>Data Hold After PROG</td>
<td></td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{EHSH}$</td>
<td>P2.7 (ENABLE) High to $V_{PP}$</td>
<td></td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{SHGL}$</td>
<td>$V_{PP}$ Setup to PROG Low</td>
<td>10</td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{GSHL}^{(1)}$</td>
<td>$V_{PP}$ Hold After PROG</td>
<td>10</td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{LGHT}$</td>
<td>PROG Width</td>
<td>1</td>
<td>110</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{AVOV}$</td>
<td>Address to Data Valid</td>
<td></td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{ELQV}$</td>
<td>ENABLE Low to Data Valid</td>
<td></td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{EHQZ}$</td>
<td>Data Float After ENABLE</td>
<td>0</td>
<td></td>
<td>48$t_{CLCL}$</td>
</tr>
<tr>
<td>$t_{GHBL}$</td>
<td>PROG High to BUSY Low</td>
<td>1.0</td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{WC}$</td>
<td>Byte Write Cycle Time</td>
<td>2.0</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

Note: 1. Only used in 12-volt programming mode.
Flash Programming and Verification Waveforms - High Voltage Mode ($V_{PP} = 12V$)

Flash Programming and Verification Waveforms - Low Voltage Mode ($V_{PP} = 5V$)
**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>(Except EA)</td>
<td>-0.5</td>
<td>0.2 VCC - 0.1</td>
<td>V</td>
</tr>
<tr>
<td>VA1</td>
<td>(Except XTAL1, RST)</td>
<td>-0.5</td>
<td>0.2 VCC - 0.3</td>
<td>V</td>
</tr>
<tr>
<td>VH</td>
<td>(XTAL1, RST)</td>
<td>0.2 VCC + 0.9</td>
<td>VCC + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>VO</td>
<td>IOL = 1.6 mA</td>
<td>0.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VO1</td>
<td>IOL = 3.2 mA</td>
<td>0.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>IOL = -60 μA, VCC = 5V ± 10%</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH1</td>
<td>IOL = -25 μA</td>
<td>0.75 VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IOL = -10 μA</td>
<td>0.9 VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH1</td>
<td>IOL = -800 μA, VCC = 5V ± 10%</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IOL = -300 μA</td>
<td>0.75 VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IOL = -80 μA</td>
<td>0.9 VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>VIN = 0.45V</td>
<td>-50</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IT</td>
<td>VIN = 2V, VCC = 5V ± 10%</td>
<td>-650</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>ILE</td>
<td>0.45 &lt; VIN &lt; VCC</td>
<td>±10</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>RRST</td>
<td>50</td>
<td>300</td>
<td>KΩ</td>
<td></td>
</tr>
<tr>
<td>CI</td>
<td>Test Freq. = 1 MHz, TA = 25°C</td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Active Mode, 12 MHz</td>
<td>20</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Idle Mode, 12 MHz</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC = 6V</td>
<td>100</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC = 3V</td>
<td>40</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

**NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Characteristics**

**NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Under steady state (non-transient) conditions, IOL must be externally limited as follows:
   - Maximum IOL per port pin: 10 mA
   - Maximum IOL per 8-bit port: Port 0: 26 mA
     - Ports 1, 2, 3: 15 mA
   - Maximum total IOL for all output pins: 71 mA
   - If IOL exceeds the test condition, VO may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum VCC for Power Down is 2V.
## AT89C51

### AC Characteristics
(Under Operating Conditions; Load Capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; Load Capacitance for all other outputs = 80 pF)

### External Program and Data Memory Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Oscillator</th>
<th>16 to 24 MHz Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1/(t_{CLCL})</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>(t_{LHLL})</td>
<td>ALE Pulse Width</td>
<td>127</td>
<td>(2t_{CLCL} - 40)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{AVLL})</td>
<td>Address Valid to ALE Low</td>
<td>43</td>
<td>(t_{CLCL} - 13)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LLAX})</td>
<td>Address Hold After ALE Low</td>
<td>48</td>
<td>(t_{CLCL} - 20)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LLIV})</td>
<td>ALE Low to Valid Instruction In</td>
<td>233</td>
<td>(4t_{CLCL} - 65)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LLPL})</td>
<td>ALE Low to PSEN Low</td>
<td>43</td>
<td>(t_{CLCL} - 13)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PLPH})</td>
<td>PSEN Pulse Width</td>
<td>205</td>
<td>(3t_{CLCL} - 20)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PLIV})</td>
<td>PSEN Low to Valid Instruction In</td>
<td>145</td>
<td>(3t_{CLCL} - 45)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PXIX})</td>
<td>Input Instruction Hold After PSEN</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PXIZ})</td>
<td>Input Instruction Float After PSEN</td>
<td>59</td>
<td>(t_{CLCL} - 10)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PXAV})</td>
<td>PSEN to Address Valid</td>
<td>75</td>
<td>(t_{CLCL} - 8)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{AVIV})</td>
<td>Address to Valid Instruction In</td>
<td>312</td>
<td>(5t_{CLCL} - 55)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PLAZ})</td>
<td>PSEN Low to Address Float</td>
<td>10</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{RLRH})</td>
<td>RD Pulse Width</td>
<td>400</td>
<td>(6t_{CLCL} - 100)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{WLWH})</td>
<td>WR Pulse Width</td>
<td>400</td>
<td>(6t_{CLCL} - 100)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{RLDV})</td>
<td>RD Low to Valid Data In</td>
<td>252</td>
<td>(5t_{CLCL} - 90)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{RHDZ})</td>
<td>Data Hold After RD</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{RHDZ})</td>
<td>Data Float After RD</td>
<td>97</td>
<td>(2t_{CLCL} - 28)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LDV})</td>
<td>ALE Low to Valid Data In</td>
<td>517</td>
<td>(8t_{CLCL} - 150)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{AVDV})</td>
<td>Address to Valid Data In</td>
<td>585</td>
<td>(9t_{CLCL} - 165)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{LLWL})</td>
<td>ALE Low to RD or WR Low</td>
<td>200</td>
<td>300</td>
<td>(3t_{CLCL} - 50)</td>
</tr>
<tr>
<td>(t_{AVWL})</td>
<td>Address to RD or WR Low</td>
<td>203</td>
<td>(4t_{CLCL} - 75)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{QVWX})</td>
<td>Data Valid to WR Transition</td>
<td>23</td>
<td>(t_{CLCL} - 20)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{QVWH})</td>
<td>Data Valid to WR High</td>
<td>433</td>
<td>(7t_{CLCL} - 120)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{WHQX})</td>
<td>Data Hold After WR</td>
<td>33</td>
<td>(t_{CLCL} - 20)</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{RLAZ})</td>
<td>RD Low to Address Float</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{WHFH})</td>
<td>RD or WR High to ALE High</td>
<td>43</td>
<td>(t_{CLCL} - 20)</td>
<td>(t_{CLCL} + 25)</td>
</tr>
</tbody>
</table>
External Program Memory Read Cycle

External Data Memory Read Cycle
External Data Memory Write Cycle

![External Data Memory Write Cycle Diagram]

External Clock Drive Waveforms

![External Clock Drive Waveforms Diagram]

External Clock Drive

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{1}{t_{CLCL}}$</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{CLCL}$</td>
<td>Clock Period</td>
<td>41.6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CHCX}$</td>
<td>High Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLCX}$</td>
<td>Low Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLCH}$</td>
<td>Rise Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CHCL}$</td>
<td>Fall Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
Serial Port Timing: Shift Register Mode Test Conditions

\(V_{CC} = 5.0 \text{ V } \pm 20\%; \text{ Load Capacitance} = 80 \text{ pF}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Osc</th>
<th>Variable Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_XLX_L</td>
<td>Serial Port Clock Cycle Time</td>
<td>1.0</td>
<td>12t_CL_CL</td>
<td>(\mu\text{s})</td>
</tr>
<tr>
<td>t_QVX_H</td>
<td>Output Data Setup to Clock Rising Edge</td>
<td>700</td>
<td>10t_CL_CL-133</td>
<td>ns</td>
</tr>
<tr>
<td>t_XHO_X</td>
<td>Output Data Hold After Clock Rising Edge</td>
<td>50</td>
<td>2t_CL_CL-117</td>
<td>ns</td>
</tr>
<tr>
<td>t_XHD_X</td>
<td>Input Data Hold After Clock Rising Edge</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>t_XHD_V</td>
<td>Clock Rising Edge to Input Data Valid</td>
<td>700</td>
<td>10t_CL_CL-133</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Shift Register Mode Timing Waveforms

![Shift Register Mode Timing Waveforms Diagram](Diagram)

### AC Testing Input/Output Waveforms

![AC Testing Input/Output Waveforms Diagram](Diagram)

**Note:** 1. AC Inputs during testing are driven at \(V_{CC} - 0.5\text{V}\) for a logic 1 and 0.45V for a logic 0. Timing measurements are made at \(V_{IH}\) min. for a logic 1 and \(V_{IL}\) max. for a logic 0.

### Float Waveforms

![Float Waveforms Diagram](Diagram)

**Note:** 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded \(V_{OH}/V_{OL}\) level occurs.
## Ordering Information

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>5V ± 20%</td>
<td>AT89C51-12AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AA</td>
<td>44A</td>
<td>Automotive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JA</td>
<td>44J</td>
<td>(-40°C to 105°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PA</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QA</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>5V ± 20%</td>
<td>AT89C51-16AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QI</td>
<td>44Q</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td>AT89C51-16AA</td>
<td>44A</td>
<td>Automotive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JA</td>
<td>44J</td>
<td>(-40°C to 105°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PA</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QA</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>5V ± 20%</td>
<td>AT89C51-20AC</td>
<td>44A</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JC</td>
<td>44J</td>
<td>(0°C to 70°C)</td>
</tr>
<tr>
<td></td>
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<td>AT89C51-20PC</td>
<td>40P6</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>AT89C51-20QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20AI</td>
<td>44A</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JI</td>
<td>44J</td>
<td>(-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20QI</td>
<td>44Q</td>
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### Ordering Information

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>5V ± 20%</td>
<td>AT89C51-24AC</td>
<td>44A</td>
<td>Commercial (0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JC</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PC</td>
<td>44P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24AI</td>
<td>44A</td>
<td>Industrial (-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JI</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PI</td>
<td>44P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QI</td>
<td>44Q</td>
<td></td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>44A 44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)</td>
</tr>
<tr>
<td>44J 44 Lead, Plastic J-Leaded Chip Carrier (PLCC)</td>
</tr>
<tr>
<td>40P6 40 Lead, 0.600” Wide, Plastic Dual Inline Package (PDIP)</td>
</tr>
<tr>
<td>44Q 44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)</td>
</tr>
</tbody>
</table>
■ NOTES:

1. This drawing measure is a standard value. All dimensions are in millimeter.
2. In case of designation is tolerance ± 0.3mm.
3. Lead spacing is measured where the lead emerge from the package.
4. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
5. These specification sheets include materials protected under copyright of EVERLIGHT corporation. Please don't reproduce or cause anyone to reproduce them without EVERLIGHT consent.
6. When using this produce, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
### Description:

1. The module is a small type infrared remote control system receiver which has been developed and designed by utilizing the latest hybrid technology.
2. This single unit type module incorporates a photo diode and a receiving preamplifier IC.
3. The demodulated output signal can directly be decoded by a microprocessor.

### Feature:

1. High protection ability to EMI and metal case can be customized.
2. Mold type and metal case type to meet the design of front panel.
3. Elliptic lens to improve the characteristic against
4. Line-up for various center carrier frequencies.
5. Low voltage and low power consumption.
6. High immunity against ambient light.
7. Photodiode with integrated circuit.
8. TTL and CMOS compatibility.

### Application:

1. Optical switch
2. Light detecting portion of remote control
   - AV instruments such as Audio, TV, VCR, CD, MD, etc.
   - Home appliances such as Air-conditioner, Fan, etc.
   - The other equipments with wireless remote control.
   - CATV set top boxes
   - Multi-media Equipment
### Absolute maximum ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
<th>Notice</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>4.3~5.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>Topr</td>
<td>-10〜+60</td>
<td>℃</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>Tstg</td>
<td>-20〜+70</td>
<td>℃</td>
<td></td>
</tr>
<tr>
<td>Soldering Temperature</td>
<td>Tsol</td>
<td>260</td>
<td>℃</td>
<td>4mm from mold body less than 5 seconds</td>
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</tbody>
</table>

### Electro Optical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>4.7</td>
<td>5</td>
<td>5.3</td>
<td>V</td>
<td>DC voltage</td>
</tr>
<tr>
<td>Supply Current</td>
<td>Icc</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>mA</td>
<td>No signal input</td>
</tr>
<tr>
<td>B.P.F Center Frequency</td>
<td>fo</td>
<td>-</td>
<td>37.9</td>
<td>-</td>
<td>KHz</td>
<td></td>
</tr>
<tr>
<td>Peak Wavelength</td>
<td>λp</td>
<td>-</td>
<td>940</td>
<td>-</td>
<td>nm</td>
<td></td>
</tr>
<tr>
<td>Transmission Distance</td>
<td>L₀</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>m</td>
<td>At the ray axis *1</td>
</tr>
<tr>
<td></td>
<td>L₄₅</td>
<td>2.5</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Half Angle</td>
<td>θ</td>
<td>-</td>
<td>45</td>
<td>-</td>
<td>deg</td>
<td></td>
</tr>
<tr>
<td>High Level Pulse Width</td>
<td>Tₗ</td>
<td>400</td>
<td>-</td>
<td>800</td>
<td>μs</td>
<td>At the ray axis *2</td>
</tr>
<tr>
<td>Low Level Pulse Width</td>
<td>Tₗ</td>
<td>400</td>
<td>-</td>
<td>800</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>High Level Output Voltage</td>
<td>Vₗ</td>
<td>4.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low Level Output Voltage</td>
<td>Vₗ</td>
<td>0.5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*1: The ray receiving surface at a vertex and relation to the ray axis in the range of φ= 0° and φ=45°.
*2: A range from 30cm to the arrival distance. Average value of 50 pulses.
TEST METHOD:
The specified electro-optical characteristics is satisfied under the following Conditions at the controllable distance.

① Measurement place
   A place that is nothing of extreme light reflected in the room.

② External light
   Project the light of ordinary white fluorescent lamps which are not high Frequency lamps and must be less then 10 Lux at the module surface.
   \( (E_e \leq 10 \text{Lux}) \)

③ Standard transmitter
   A transmitter whose output is so adjusted as to \( V_0=400 \text{mVp-p} \) and the output Wave form shown in Fig.-1. According to the measurement method shown in Fig.-2 the standard transmitter is specified. However, the infrared photodiode to be used for the transmitter should be \( \lambda_p=940 \text{nm}, \Delta\lambda=50 \text{nm} \). Also, photo diode is used of PD438B \( (V_R=5V) \).
   \( \text{(Standard light / Light source temperature } 2856^\circ\text{K)} \).

④ Measuring system
   According to the measuring system shown in Fig.-3
Carrier frequency is adjusted to center frequency of each product.

Fig.-1  Transmitter Wave Form  

- IR TRANSMITTER OUTPUT WAVE FORM
- Duty=0.5

Fig.-2  Measuring Method

- Standard Transmitter
- Oscilloscope
- 10uF

Fig.-3  Measuring System

- Angle Of Horizontal & Vertical Direction
- Transmission Distance L
TYPICAL ELECTRICAL/OPTICAL/CHARACTERISTICS CURVES

Fig.-4 Relative Spectral Sensitivity vs. Wavelength

Fig.-5 Relative Transmission Distance vs. Direction

Fig.-6 Output Pulse Length vs. Arrival Distance

Fig.-7 Arrival Distance vs. Supply Voltage

Fig.-8 Relative Transmission Distance vs. Center Carrier Frequency

Fig.-9 Arrival Distance vs. Ambient Temperature
## Reliability test item and condition:

The reliability of products shall be satisfied with items listed below.

Confidence level: 90%
LTPD: 10%

<table>
<thead>
<tr>
<th>Test Items</th>
<th>Test Conditions</th>
<th>Failure Judgement Criteria</th>
<th>Samples(n)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation life</td>
<td>Vcc=5V, Ta: 25℃ 1000hrs</td>
<td>$L_0 \leq L \times 0.8$</td>
<td>n=22, c=0</td>
</tr>
<tr>
<td>Temperature cycle</td>
<td>1 cycle -20℃ +25℃ +70℃ (30min) 5min (30min) 50 cycle test</td>
<td>$L_{45} \leq L \times 0.8$</td>
<td>n=22, c=0</td>
</tr>
<tr>
<td>Thermal shock</td>
<td>-10℃ to +70℃ (5min) (10sec) (5min) 50 cycle test</td>
<td></td>
<td>n=22, c=0</td>
</tr>
<tr>
<td>High temperature storage</td>
<td>Temp: +70℃ 1000hrs</td>
<td></td>
<td>n=22, c=0</td>
</tr>
<tr>
<td>Low temperature storage</td>
<td>Temp: -20℃ 1000hrs</td>
<td></td>
<td>n=22, c=0</td>
</tr>
<tr>
<td>High temperature High humidity</td>
<td>Ta: 85℃ RH: 85% 1000hrs</td>
<td>L: Lower specification limit</td>
<td>n=22, c=0</td>
</tr>
<tr>
<td>Solder heat</td>
<td>Temp: 260± 5℃ 5sec 4mm Form the bottom of the package.</td>
<td></td>
<td>n=22, c=0</td>
</tr>
<tr>
<td>Solderability</td>
<td>Temp: 230± 5℃ 5sec 4mm Form the bottom of the package.</td>
<td>More than 90% of Lead to be covered by soldering</td>
<td>n=22, c=0</td>
</tr>
</tbody>
</table>
■ Packing Specifications

1. Plastic Case

2. Box

3. Carton

Packing Quantity Specification

1. 40 Pcs/1Plastic Case, 4Plastic Cases/1Box
2. 10 Boxes/1Carton

CPN : Customer’s Production Number
P/N : Production Number
QTY : Packing Quantity
CAT : Ranks
HUE : Peak Wavelength
REF : Reference
LOT NO : Lot Number
MADE IN TAIWAN : Production place
awal:
    mov a,#00h
    mov r0,#8
    mov r1,#0
    mov p1,#00h
    mov tmod,#21h
start:
    jb p2.1,$
    acall delay2
    acall delay
mulai:
    jb p2.1,tambah
    ljmp tetep
two:
    jb p2.1,tambah1
    ljmp tetep1
three:
    jb p2.1,tambah2
    ljmp tetep2
four:
    jb p2.1,tambah3
    ljmp tetep3
five:
    jb p2.1,tambah4
    ljmp tetep4			tambah:
        inc r1
        nop
        nop
        nop
        ljmp two
tetep:
        nop
        nop
        nop
        ljmp two
tambah1:
        inc r1
        nop
        nop
        nop
        ljmp three
tetep1:
nop
nop
nop
ljmp three
tambah2:
  inc r1
  nop
  nop
  nop
  jmp four
tetep2:
  nop
  nop
  nop
  jmp four
tambah3:
  inc r1
  nop
  nop
  nop
  jmp five
tetep3:
  nop
  nop
  nop
  jmp five
tambah4:
  inc r1
  nop
  nop
  nop
  jmp poiu			
tetep4:
  nop
  nop
  nop
  jmp poiu	poiu:
  cjne r1,#05,satu
  sjmp nol
satu:
  setb acc.0
  rr A
  djnz r0,mulai
  jmp aaa
nol:
    clr acc.0
    rr A
    djnz r0,mulai
aaa:
    mov p0,a
    cjne a,#01h,cex
    ljmp awal1
cex:
    cjne a,#02h,cex1
    ljmp awal1
cex1:
    cjne a,#02h,kirim_ulang
    ljmp awal1
kirim_ulang:
    mov r2,#20
ool:
    setb p1.0
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    clr p1.0
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
djnz r1,ool
    ljmp start
awal1:
mov a,#00h
mov r0,#8
mov r1,#0
mov p1,#00h
mov tmod,#21h

start1:
  jb p2.1,$
  acall delay2
  acall delay

mulai1:
  jb p2.1,tambah0
  ljmp tetep0

two1:
  jb p2.1,tambah11
  ljmp tetep11

three1:
  jb p2.1,tambah21
  ljmp tetep21

four1:
  jb p2.1,tambah31
  ljmp tetep31

five1:
  jb p2.1,tambah41
  ljmp tetep41

tambah0:
  inc r1
  nop
  nop
  nop
  ljmp two1

tetep0:
  nop
  nop
  nop
  ljmp two1

tambah11:
  inc r1
  nop
  nop
  nop
  ljmp three1

tetep11:
  nop
  nop
  nop
  ljmp three1
tambah21:
  inc r1
  nop
  nop
  nop
  ljmp four1
tetep21:
  nop
  nop
  nop
  nop
  ljmp four1
tambah31:
  inc r1
  nop
  nop
  nop
  ljmp five1
tetep31:
  nop
  nop
  nop
  nop
  ljmp five1
tambah41:
  inc r1
  nop
  nop
  nop
  nop
  ljmp poiu1
tetep41:
  nop
  nop
  nop
  nop
  ljmp poiu1
poi1:
  cjne r1,#05,satu1
  sjmp nol1
satu1:
  setb acc.0
  rr A
  djnz r0,mulai1
  sjmp aaa1
nol1:
  clr acc.0
  rr A
  djnz r0,mulai1
aaa1:
mov p0,a
cjne a,#0fah,kirim_ulang1
ljmp awal1

kirim_ulang1:
    mov r2,#20
ool1:
    setb p1.0
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    clr p1.0
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    djnz r1,ool1
    ljmp start1

awal00:
    mov a,#00h
    mov r0,#8
    mov r1,#0
    mov p1,#00h
    mov tmmod,#21h
start00:
    jb p2.1,$
    acall delay2
    acall delay
mulai00:
    jb p2.1,tambah00
ljmp tetep00

two00:
    jb p2.1,tambah100
    ljmp tetep100
three00:
    jb p2.1,tambah200
    ljmp tetep200
four00:
    jb p2.1,tambah300
    ljmp tetep300
five00:
    jb p2.1,tambah400
    ljmp tetep400
tambah00:
    inc r1
    nop
    nop
    nop
    ljmp two00
tetep00:
    nop
    nop
    nop
    ljmp two00
tambah100:
    inc r1
    nop
    nop
    nop
    ljmp three00
tetep100:
    nop
    nop
    nop
    ljmp three00
tambah200:
    inc r1
    nop
    nop
    nop
    ljmp four00
tetep200:
    nop
    nop
    nop
    ljmp four00
tambah300:
    inc r1
    nop
    nop
    nop
    ljmp five00

tetep300:
    nop
    nop
    nop
    ljmp five00

tambah400:
    inc r1
    nop
    nop
    nop
    ljmp poiu00

tetep400:
    nop
    nop
    nop
    ljmp poiu00

poiu00:
    cjne r1,#05,satu00
    sjmp nol00

satu00:
    setb acc.0
    rr A
    djnz r0,mulai00
    sjmp aaa00

nol00:
    clr acc.0
    rr A
    djnz r0,mulai00

aaa00:
    mov p0,a
    cjne a,#00h,kirim_ulang00
    ljmp awal00

kirim_ulang00:
    mov r2,#20

ool00:
    setb p1.0
    nop
    nop
    nop
    nop
nop
nop
clr p1.0
nop
djnz r1,ool00
ljmp start00

kirim_serial:
    mov th1,#0f3h
    mov tl1,#0f3h
    setb tr1
    mov r1,#01h
    mov r2,#55h
    mov r3,#00h
    mov a,r1
    mov sbuf,a
    jnb ti,$
    clr ti
    mov a,r2
    mov sbuf,a
    jnb ti,$
    clr ti
    mov a,r3
    mov sbuf,a
    jnb ti,$
    clr ti
    sjmp selesai

delay:
    mov th0,#7fh
mov tl0,#0ffh
setb tr0
jnb tf0,$
clr tr0
clr tf0
ret

delay2:
    mov th0,#00h
    mov tl0,#00h
    setb tr0
    jnb tf0,$
    clr tr0
clr tf0
ret
selesai:
    end
$mod51

org 0000h
ljmp start

org 000bh
cpl p1.0
reti

start:
  mov a,#00000001b
  setb p1.0
  acall delay
  mov R0,#9
  setb et0
  mov tmod,#12h
  mov th0,#0f0h
  mov tl0,#0f0h
  setb ea

haha:
  mov th1,#00h
  mov tl1,#00h
  setb tr1
  setb tr0
  jnb tf1,$
  clr tr0
  clr tr1
  clr tf1
  rl A

banding:
  djnz r0,jalan
  sjmp start

jalan:
  rr A
  jb Acc.0,satu
  sjmp nol

nol:
  mov th1,#00h
  mov tl1,#00h
  setb tr1
  setb tr0
  jnb tf1,$
  clr tr0
  clr tr1
  clr tf1
sjmp banding

satu:
    clr p1.0
    mov th1,#00h
    mov tl1,#00h
    setb tr1
    jnb tf1,$
    clr tr1
    clr tf1
    sjmp banding

cek_bit:
    mov th1,#00h
    mov tl1,#00h
    setb tr1

cek:
    jb p2.1,kk
    clr tf1
    clr tr1
    sjmp start

kk:
    jnb tf1,cek
    clr tf1
    clr tr1

start1:
    mov a,#11111010b
    setb p1.0
    acall delay
    mov R0,#9
    setb et0
    mov tmod,#12h
    mov th0,#0f0h
    mov tl0,#0f0h
    setb ea

haha1:
    mov th1,#00h
    mov tl1,#00h
    setb tr1
    setb tr0
    jnb tf1,$
    clr tr0
    clr tr1
    clr tf1
    rl A
banding1:
    djnz r0,jalan1
    sjmp start1
jalan1:
    rr A
    jb Acc.0,satu1
    sjmp nol1
nol1:
    mov th1,#00h
    mov tl1,#00h
    setb tr1
    setb tr0
    jnb tf1,$
    clr tr0
    clr tr1
    clr tf1
    sjmp banding1
satu1:
    clr p1.0
    mov th1,#00h
    mov tl1,#00h
    setb tr1
    jnb tf1,$
    clr tf1
    sjmp banding1
cek_bit1:
    mov th1,#00h
    mov tl1,#00h
    setb tr1
cek1:
    jb p2.1,kk1
    clr tf1
    clr tr1
    sjmp start1
kk1:
    jnb tf1,cek1
    clr tf1
    clr tr1
start2:
    mov a,#00000000b
    setb p1.0
    acall delay
    mov R0,#9
setb et0
mov tmod,#12h
mov th0,#0f0h
mov tl0,#0f0h
setb ea
haha2:
mov th1,#00h
mov tl1,#00h
setb tr1
setb tr0
jnb tf1,$
clr tr0
clr tr1
clr tf1
rl A

banding2:
djnz r0,jalan2
sjmp start2
jalan2:
rr A
jb Acc.0,satu2
sjmp nol2
nol2:
mov th1,#00h
mov tl1,#00h
setb tr1
setb tr0
jnb tf1,$
clr tr0
clr tr1
clr tf1
sjmp banding2
satu2:
clr p1.0
mov th1,#00h
mov tl1,#00h
setb tr1
setb tr0
jnb tf1,$
clr tr1
clr tf1
sjmp banding2
cek_bit2:
mov th1,#00h
mov tl1,#00h
setb tr1
cek2:
    jb p2.1,kk2
    clr tf1
    clr tr1
    sjmp start2
kk2:
    jnb tf1,cek2
    clr tf1
    clr tr1
    sjmp selesai
delay:
    mov r7,#8
loop:
    mov r6,#250
loop2:
    mov r5,#250
loop3:
    djnz r5,$
    djnz r6,loop2
    djnz r7,loop
    ret
selesai:
    end