LAMPIRAN-A

DATASHEET KOMPONEN
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

Featuring continuous load current ratings to 500 mA for each of the drivers, the Series ULN28xxA/LW and ULQ28xxA/LW high-voltage, high-current Darlington arrays are ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads. Typical power loads totaling over 260 W (350 mA x 8, 95 V) can be controlled at an appropriate duty cycle depending on ambient temperature and number of drivers turned on simultaneously. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. All devices feature open-collector outputs with integral clamp diodes.

The ULx2803A, ULx2803LW, ULx2823A, and ULN2823LW have series input resistors selected for operation directly with 5 V TTL or CMOS. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

The ULx2804A, ULx2804LW, ULx2824A, and ULN2824LW have series input resistors for operation directly from 6 V to 15 V CMOS or PMOS logic outputs.

The ULx2803A/LW and ULx2804A/LW are the standard Darlington arrays. The outputs are capable of sinking 500 mA and will withstand at least 50 V in the off state. Outputs may be paralleled for higher load current capability. The ULx2823A/LW and ULx2824A/LW will withstand 95 V in the off state.

These Darlington arrays are furnished in 18-pin dual in-line plastic packages (suffix ‘A’) or 18-lead small-outline plastic packages (suffix ‘LW’). All devices are pinned with outputs opposite inputs to facilitate ease of circuit board layout. Prefix ‘ULN’ devices are rated for operation over the temperature range of -20°C to +85°C; prefix ‘ULQ’ devices are rated for operation to -40°C.

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Output Current to 500 mA
- Output Voltage to 95 V
- Transient-Protected Outputs
- Dual In-Line Package or Wide-Body Small-Outline Package

**The ULx2804, ULx2823, & ULx2824 are last-time buy. Orders accepted until October 19, 2001.**

x = Character to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown. See matrix on next page.
2803 THRU 2824
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

DEVICE PART NUMBER DESIGNATION

<table>
<thead>
<tr>
<th>Logic</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>5V</td>
<td>ULN2803A* ULN2803LW*</td>
</tr>
<tr>
<td>TTL, CMOS</td>
<td>ULN2823A* ULN2823LW</td>
</tr>
<tr>
<td>6-15 V</td>
<td>ULN2804A* ULN2804LW*</td>
</tr>
<tr>
<td>CMOS, PMOS</td>
<td>ULN2824A* ULN2824LW</td>
</tr>
</tbody>
</table>

* Also available for operation between -40°C and +85°C. To order, change prefix from 'ULN' to 'ULQ'.

The ULx2804, ULx2823, & ULx2824 are last-time buy. Orders accepted until October 19, 2001.

PARTIAL SCHEMATICS

ULx28x3A/LW (Each Driver)

ULx28x4A/LW (Each Driver)

x = Character to identify specific device. Specification shown applies to family of devices with remaining digits as shown. See matrix above.
Types ULx2803A, ULx2803LW, ULx2804A, and ULx2804LW
ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Test Fig.</th>
<th>Applicable Devices</th>
<th>Test Conditions</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>ICEX</td>
<td>1A</td>
<td>All</td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 50 V, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 50 V, T&lt;sub&gt;A&lt;/sub&gt; = 70°C</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1B</td>
<td>ULx2804x</td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 50 V, T&lt;sub&gt;A&lt;/sub&gt; = 70°C, V&lt;sub&gt;IN&lt;/sub&gt; = 1.0 V</td>
<td>—</td>
</tr>
<tr>
<td>Collector-Emitter Saturation Voltage</td>
<td>V&lt;sub&gt;CE(SAT)&lt;/sub&gt;</td>
<td>2</td>
<td>All</td>
<td>I&lt;sub&gt;C&lt;/sub&gt; = 100 mA, I&lt;sub&gt;B&lt;/sub&gt; = 250 µA</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I&lt;sub&gt;C&lt;/sub&gt; = 200 mA, I&lt;sub&gt;B&lt;/sub&gt; = 350 µA</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>I&lt;sub&gt;C&lt;/sub&gt; = 350 mA, I&lt;sub&gt;B&lt;/sub&gt; = 500 µA</td>
<td>—</td>
</tr>
<tr>
<td>Input Current</td>
<td>I&lt;sub&gt;IN(ON)&lt;/sub&gt;</td>
<td>3</td>
<td>ULx2803x</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 3.85 V</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 5.0 V</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 12 V</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>I&lt;sub&gt;IN(OFF)&lt;/sub&gt;</td>
<td>4</td>
<td>All</td>
<td>I&lt;sub&gt;C&lt;/sub&gt; = 500 µA, T&lt;sub&gt;A&lt;/sub&gt; = 70°C</td>
<td>50</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>V&lt;sub&gt;IN(ON)&lt;/sub&gt;</td>
<td>5</td>
<td>ULx2803x</td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 2.0 V, I&lt;sub&gt;C&lt;/sub&gt; = 200 mA</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 2.0 V, I&lt;sub&gt;C&lt;/sub&gt; = 250 mA</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 2.0 V, I&lt;sub&gt;C&lt;/sub&gt; = 300 mA</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ULx2804x</td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 2.0 V, I&lt;sub&gt;C&lt;/sub&gt; = 125 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 2.0 V, I&lt;sub&gt;C&lt;/sub&gt; = 200 mA</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 2.0 V, I&lt;sub&gt;C&lt;/sub&gt; = 275 mA</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;C&lt;/sub&gt;E = 2.0 V, I&lt;sub&gt;C&lt;/sub&gt; = 350 mA</td>
<td>—</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>—</td>
<td>All</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>Turn-On Delay</td>
<td>t&lt;sub&gt;PLH&lt;/sub&gt;</td>
<td>8</td>
<td>All</td>
<td>0.5 E&lt;sub&gt;IN&lt;/sub&gt; to 0.5 E&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>—</td>
</tr>
<tr>
<td>Turn-Off Delay</td>
<td>t&lt;sub&gt;PHL&lt;/sub&gt;</td>
<td>8</td>
<td>All</td>
<td>0.5 E&lt;sub&gt;IN&lt;/sub&gt; to 0.5 E&lt;sub&gt;OUT&lt;/sub&gt;</td>
<td>—</td>
</tr>
<tr>
<td>Clamp Diode Leakage Current</td>
<td>I&lt;sub&gt;R&lt;/sub&gt;</td>
<td>6</td>
<td>All</td>
<td>V&lt;sub&gt;R&lt;/sub&gt; = 50 V, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;R&lt;/sub&gt; = 50 V, T&lt;sub&gt;A&lt;/sub&gt; = 70°C</td>
<td>—</td>
</tr>
<tr>
<td>Clamp Diode Forward Voltage</td>
<td>V&lt;sub&gt;F&lt;/sub&gt;</td>
<td>7</td>
<td>All</td>
<td>I&lt;sub&gt;F&lt;/sub&gt; = 350 mA</td>
<td>—</td>
</tr>
</tbody>
</table>

Complete part number includes prefix to operating temperature range: ULN = -20°C to +85°C, ULQ = -40°C to +85°C and a suffix to identify package style: A = DIP, LW = SOIC.

The ULx2804 is last-time buy.
Orders accepted until October 19, 2001.
## Types ULx2823A, ULN2823LW, ULx2824A, and ULN2824LW

**ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted).**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Test Fig.</th>
<th>Applicable Devices</th>
<th>Test Conditions</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Leakage Current</td>
<td>$I_{CEX}$</td>
<td>1A</td>
<td>All</td>
<td>$V_{CE} = 95 \text{ V}, T_A = 25^\circ \text{C}$</td>
<td>$- &lt; 1$ $50 \ \mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{CE} = 95 \text{ V}, T_A = 70^\circ \text{C}$</td>
<td>$- &lt; 1$ $100 \ \mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1B ULx2824x</td>
<td>$V_{CE} = 95 \text{ V}, T_A = 70^\circ \text{C}, V_{IN} = 1.0 \text{ V}$</td>
<td>$- &lt; 5$ $500 \ \mu\text{A}$</td>
</tr>
<tr>
<td>Collector-Emitter Saturation Voltage</td>
<td>$V_{CE(SAT)}$</td>
<td>2</td>
<td>All</td>
<td>$I_C = 100 \text{ mA}, I_B = 250 \ \mu\text{A}$</td>
<td>$- 0.9$ $1.1 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$I_C = 200 \text{ mA}, I_B = 350 \ \mu\text{A}$</td>
<td>$- 1.1$ $1.3 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$I_C = 350 \text{ mA}, I_B = 500 \ \mu\text{A}$</td>
<td>$- 1.3$ $1.6 \ \text{V}$</td>
</tr>
<tr>
<td>Input Current</td>
<td>$I_{IN(ON)}$</td>
<td>3</td>
<td>ULx2823x</td>
<td>$V_{IN} = 3.85 \text{ V}$</td>
<td>$- 0.93$ $1.35 \ \text{mA}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ULx2824x</td>
<td>$V_{IN} = 5.0 \text{ V}$</td>
<td>$- 0.35$ $0.5 \ \text{mA}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{IN} = 12 \text{ V}$</td>
<td>$- 1.0$ $1.45 \ \text{mA}$</td>
</tr>
<tr>
<td></td>
<td>$I_{IN(OFF)}$</td>
<td>4</td>
<td>All</td>
<td>$I_C = 500 \ \mu\text{A}, T_A = 70^\circ \text{C}$</td>
<td>$50$ $65$ $-$ $\mu\text{A}$</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>$V_{IN(ON)}$</td>
<td>5</td>
<td>ULx2823x</td>
<td>$V_{CE} = 2.0 \text{ V}, I_C = 200 \text{ mA}$</td>
<td>$- - -$ $2.4 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{CE} = 2.0 \text{ V}, I_C = 250 \text{ mA}$</td>
<td>$- - -$ $2.7 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{CE} = 2.0 \text{ V}, I_C = 300 \text{ mA}$</td>
<td>$- - -$ $3.0 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ULx2824x</td>
<td>$V_{CE} = 2.0 \text{ V}, I_C = 125 \text{ mA}$</td>
<td>$- - -$ $5.0 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{CE} = 2.0 \text{ V}, I_C = 200 \text{ mA}$</td>
<td>$- - -$ $6.0 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{CE} = 2.0 \text{ V}, I_C = 275 \text{ mA}$</td>
<td>$- - -$ $7.0 \ \text{V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{CE} = 2.0 \text{ V}, I_C = 350 \text{ mA}$</td>
<td>$- - -$ $8.0 \ \text{V}$</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$C_{IN}$</td>
<td>—</td>
<td>All</td>
<td>—</td>
<td>$15$ $25$ $\text{pF}$</td>
</tr>
<tr>
<td>Turn-On Delay</td>
<td>$t_{PLH}$</td>
<td>8</td>
<td>All</td>
<td>$0.5 \ E_{IN}$ to $0.5 \ E_{OUT}$</td>
<td>$0.25$ $1.0 \ \mu\text{s}$</td>
</tr>
<tr>
<td>Turn-Off Delay</td>
<td>$t_{PHL}$</td>
<td>8</td>
<td>All</td>
<td>$0.5 \ E_{IN}$ to $0.5 \ E_{OUT}$</td>
<td>$0.25$ $1.0 \ \mu\text{s}$</td>
</tr>
<tr>
<td>Clamp Diode Leakage Current</td>
<td>$I_R$</td>
<td>6</td>
<td>All</td>
<td>$V_R = 95 \text{ V}, T_A = 25^\circ \text{C}$</td>
<td>$- - -$ $50 \ \mu\text{A}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_R = 95 \text{ V}, T_A = 70^\circ \text{C}$</td>
<td>$- - -$ $100 \ \mu\text{A}$</td>
</tr>
<tr>
<td>Clamp Diode Forward Voltage</td>
<td>$V_F$</td>
<td>7</td>
<td>All</td>
<td>$I_F = 350 \text{ mA}$</td>
<td>$- 1.7$ $2.0 \ \text{V}$</td>
</tr>
</tbody>
</table>

Complete part number includes prefix to operating temperature range: ULN = -20°C to +85°C, ULQ = -40°C to +85°C and a suffix to identify package style: A = DIP, LW = SOIC. Note that the ULQ2823LW and ULQ2824LW are not presently available.

The ULx2823 & ULx2824 are last-time buy. Orders accepted until October 19, 2001.
x = Characters to identify specific device. Specification shown applies to family of devices with remaining digits as shown.
x = Characters to identify specific device. Characteristic shown applies to family of devices with remaining digits as shown.
PACKAGE DESIGNATOR “A” DIMENSIONS
Dimensions in Inches
(controlling dimensions)

Dimensions in Millimeters
(for reference only)

NOTES: 1. Exact body and lead configuration at vendor’s option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.
NOTES: 1. Exact body and lead configuration at vendor’s option within limits shown.
2. Lead spacing tolerance is non-cumulative.
The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.
ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit µP Compatible A/D Converters

General Description
The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates “stand alone”
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3” standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications
- Resolution: 8 bits
- Total error: ±1/4 LSB, ±1/2 LSB and ±1 LSB
- Conversion time: 100 µs

Connection Diagram

Ordering Information

<table>
<thead>
<tr>
<th>TEMP RANGE</th>
<th>0°C TO 70°C</th>
<th>0°C TO 70°C</th>
<th>–40°C TO +85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>ERROR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>±1/4 Bit Adjusted</td>
<td>ADC0802LCWM</td>
<td>ADC0801LCN</td>
<td></td>
</tr>
<tr>
<td>±1/2 Bit Unadjusted</td>
<td>ADC0804LCWM</td>
<td>ADC0804LCN</td>
<td>ADC0805LCN/ADC0804LCJ</td>
</tr>
<tr>
<td>±1/4 Bit Unadjusted</td>
<td>ADC0804LCJ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PACKAGE OUTLINE</td>
<td>M20B—Small Outline</td>
<td>N20A—Molded DIP</td>
<td></td>
</tr>
</tbody>
</table>

© 2001 National Semiconductor Corporation  DS005671  www.national.com
Typical Applications

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Full-Scale Adjusted</th>
<th>$V_{REF}/2 = 2.500 V_{DC}$ (No Adjustments)</th>
<th>$V_{REF}/2 = \text{No Connection}$ (No Adjustments)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0801</td>
<td>$\pm 1/4 \text{ LSB}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0802</td>
<td>$\pm 1/2 \text{ LSB}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0803</td>
<td>$\pm 1/2 \text{ LSB}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0804</td>
<td>$\pm 1 \text{ LSB}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0805</td>
<td></td>
<td></td>
<td>$\pm 1 \text{ LSB}$</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings (Notes 1, 2)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (VCC) (Note 3) 6.5V
Voltage
Logic Control Inputs −0.3V to +18V
At Other Input and Outputs −0.3V to (VCC+0.3V)
Lead Temp. (Soldering, 10 seconds) Dual-In-Line Package (plastic) 260˚C
Dual-In-Line Package (ceramic) 300˚C
Surface Mount Package Vapor Phase (60 seconds) 215˚C

Operating Ratings (Notes 1, 2)
Temperature Range TMIN≤TA≤TMAX
ADC0804LCJ −40˚C≤TA≤+85˚C
ADC0801/02/03/05LCN −40˚C≤TA≤+85˚C
ADC0804LCN 0˚C≤TA≤+70˚C
ADC0802/04LCWM 0˚C≤TA≤+70˚C
Range of VCC 4.5 VDC to 6.3 VDC

Electrical Characteristics
The following specifications apply for VCC=5 VDC, TMIN≤TA≤TMAX and fCLK=640 kHz unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0801: Total Adjusted Error (Note 8)</td>
<td>With Full-Scale Adj. (See Section 2.5.2)</td>
<td>±1/4</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0802: Total Unadjusted Error (Note 8)</td>
<td>VREF/2=2.500 VDC</td>
<td>±1/2</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0803: Total Adjusted Error (Note 8)</td>
<td>With Full-Scale Adj. (See Section 2.5.2)</td>
<td>±1/2</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0804: Total Unadjusted Error (Note 8)</td>
<td>VREF/2=2.500 VDC</td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC0805: Total Unadjusted Error (Note 8)</td>
<td>VREF/2-No Connection</td>
<td>±1</td>
<td>LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREF/2 Input Resistance (Pin 9)</td>
<td>ADC0801/02/03/05</td>
<td>2.5</td>
<td>8.0</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ADC0804 (Note 9)</td>
<td>0.75</td>
<td>1.1</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td>Analog Input Voltage Range</td>
<td>(Note 4) V(+) or V(−) Gnd–0.05 VDC ±1/16</td>
<td>VCC+0.05 VDC ±1/16</td>
<td>VDC ±1/8</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>DC Common-Mode Error</td>
<td>Over Analog Input Voltage Range</td>
<td>±1/16</td>
<td>±1/8</td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>VCC=5 VDC ±10% Over Allowed VIN(+) and VIN(−) Voltage Range (Note 4)</td>
<td>±1/16</td>
<td>±1/8</td>
<td>LSB</td>
<td></td>
</tr>
</tbody>
</table>

AC Electrical Characteristics
The following specifications apply for VCC=5 VDC and TMIN≤TA≤TMAX unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC</td>
<td>Conversion Time</td>
<td>fCLK=640 kHz (Note 6)</td>
<td>103</td>
<td>114</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>TC</td>
<td>Conversion Time</td>
<td>(Notes 5, 6)</td>
<td>66</td>
<td>73</td>
<td>1/fCLK</td>
<td></td>
</tr>
<tr>
<td>fCLK</td>
<td>Clock Frequency</td>
<td>VCC=5V, (Note 5)</td>
<td>100</td>
<td>640</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock Duty Cycle</td>
<td>40</td>
<td>60</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CR</td>
<td>Conversion Rate in Free-Running Mode</td>
<td>INTR tied to WR with CS=0 VDC, fCLK=640 kHz</td>
<td>8770</td>
<td>9708</td>
<td>conv/s</td>
<td></td>
</tr>
<tr>
<td>tWR/WRIL</td>
<td>Width of WR Input (Start Pulse Width)</td>
<td>CS=0 VDC (Note 7)</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tACC</td>
<td>Access Time (Delay from Falling Edge of RD to Output Data Valid)</td>
<td>CL=100 pF</td>
<td>135</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t1H, t2H</td>
<td>TRI-STATE Control (Delay from Rising Edge of RD to Hi-Z State)</td>
<td>CL=10 pF, RL=10k</td>
<td>125</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWR, tRI</td>
<td>Delay from Falling Edge of WR or RD to Reset of INTR</td>
<td>300</td>
<td>450</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance of Logic Control Inputs</td>
<td>5</td>
<td>7.5</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5 \, V_{DC}$ and $T_{MIN} \leq T_{A} \leq T_{MAX}$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{OUT}$</td>
<td>TRI-STATE Output Capacitance (Data Buffers)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$ (1)</td>
<td>Logical “1” Input Voltage (Except Pin 4 CLK IN)</td>
<td>$V_{CC} = 5.25 , V_{DC}$</td>
<td>2.0</td>
<td>15</td>
<td></td>
<td>$V_{DC}$</td>
</tr>
<tr>
<td>$V_{IN}$ (0)</td>
<td>Logical “0” Input Voltage (Except Pin 4 CLK IN)</td>
<td>$V_{CC} = 4.75 , V_{DC}$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>$V_{DC}$</td>
</tr>
<tr>
<td>$I_{IN}$ (1)</td>
<td>Logical “1” Input Current (All Inputs)</td>
<td>$V_{IN} = 5 , V_{DC}$</td>
<td>0.005</td>
<td>1</td>
<td></td>
<td>$\mu A_{DC}$</td>
</tr>
<tr>
<td>$I_{IN}$ (0)</td>
<td>Logical “0” Input Current (All Inputs)</td>
<td>$V_{IN} = 0 , V_{DC}$</td>
<td>–1</td>
<td>–0.005</td>
<td></td>
<td>$\mu A_{DC}$</td>
</tr>
</tbody>
</table>

**CONTROL INPUTS** [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ (1)</td>
<td>Logical “1” Input Voltage (Except Pin 4 CLK IN)</td>
<td>$V_{CC} = 5.25 , V_{DC}$</td>
<td>2.0</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$ (0)</td>
<td>Logical “0” Input Voltage (Except Pin 4 CLK IN)</td>
<td>$V_{CC} = 4.75 , V_{DC}$</td>
<td>0.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$ (1)</td>
<td>Logical “1” Input Current (All Inputs)</td>
<td>$V_{IN} = 5 , V_{DC}$</td>
<td>0.005</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$ (0)</td>
<td>Logical “0” Input Current (All Inputs)</td>
<td>$V_{IN} = 0 , V_{DC}$</td>
<td>–1</td>
<td>–0.005</td>
<td></td>
</tr>
</tbody>
</table>

**CLOCK IN AND CLOCK R**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$ (1)</td>
<td>Logical “1” Input Voltage (Except Pin 4 CLK IN)</td>
<td>$V_{CC} = 5.25 , V_{DC}$</td>
<td>2.0</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$ (0)</td>
<td>Logical “0” Input Voltage (Except Pin 4 CLK IN)</td>
<td>$V_{CC} = 4.75 , V_{DC}$</td>
<td>0.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$ (1)</td>
<td>Logical “1” Input Current (All Inputs)</td>
<td>$V_{IN} = 5 , V_{DC}$</td>
<td>0.005</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$ (0)</td>
<td>Logical “0” Input Current (All Inputs)</td>
<td>$V_{IN} = 0 , V_{DC}$</td>
<td>–1</td>
<td>–0.005</td>
<td></td>
</tr>
</tbody>
</table>

**DATA OUTPUTS AND INTR**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OUT}$</td>
<td>TRI-STATE Disabled Output Leakage (All Data Buffers)</td>
<td>$V_{OUT} = 0 , V_{DC}$</td>
<td>–3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SOURCE}$</td>
<td>$V_{OUT}$ Short to Gnd, $T_{A} = 25^\circ C$</td>
<td>4.5</td>
<td>6</td>
<td></td>
<td>$mA_{DC}$</td>
</tr>
<tr>
<td>$I_{SINK}$</td>
<td>$V_{OUT}$ Short to $V_{CC}$, $T_{A} = 25^\circ C$</td>
<td>9.0</td>
<td>16</td>
<td></td>
<td>$mA_{DC}$</td>
</tr>
</tbody>
</table>

**POWER SUPPLY**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current (Includes Ladder Current)</td>
<td>$I_{CLK} = 640 , kHz$, $V_{REF}/2 = NC$, $T_{A} = 25^\circ C$ and $CS = 5V$</td>
<td>1.1</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>ADC0804LCN/LCWM</td>
<td></td>
<td></td>
<td>1.9</td>
<td>2.5</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
2. All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.
3. A zener diode exists, internally, from $V_{CC}$ to Gnd and has a typical breakdown voltage of 7 $V_{OC}$.
4. For $V_{IN}(−) > V_{IN}(+) + 2$ mA. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the $V_{CC}$ supply. Be careful, during testing at low $V_{CC}$ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog $V_{IN}$ does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 $V_{DC}$ to 5 $V_{OC}$ input voltage range will therefore require a minimum supply voltage of 4.950 $V_{OC}$ over temperature variations, initial tolerance and loading.
5. Accuracy is guaranteed at $f_{CLK} = 640 \, kHz$. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.
6. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see Figure 4 and section 2.0.
AC Electrical Characteristics (Continued)

Note 7: The CS input is assumed to bracket the WR strobe input and therefore timing is dependent on the WR pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the WR pulse (see timing diagrams).

Note 8: None of these ADs requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and Figure 7.

Note 9: The VREF/2 pin is the center point of a two-resistor divider connected from VCC to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically 16 kΩ. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically 2.2 kΩ.

Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Typical Performance Characteristics

Logic Input Threshold Voltage

Delay From Falling Edge of RD to Output Data Valid

CLK IN Schmitt Trip Levels

vs. Supply Voltage

vs. Load Capacitance

vs. Supply Voltage

\[ f_{CLK} \text{ vs. Clock Capacitor} \]

\[ \text{Full-Scale Error vs Conversion Time} \]

\[ \text{Effect of Unadjusted Offset Error vs. VREF/2 Voltage} \]

\[ \text{Output Current vs Temperature} \]

\[ \text{Power Supply Current vs Temperature (Note 9)} \]

\[ \text{Linearity Error at Low VREF/2 Voltages} \]
TRI-STATE Test Circuits and Waveforms

Timing Diagrams (All timing is measured from the 50% voltage points)
Timing Diagrams  (All timing is measured from the 50% voltage points)  (Continued)

Output Enable and Reset with INTR

Note: Read strobe must occur 8 clock periods ($8 / f_{CLK}$) after assertion of interrupt to guarantee reset of INTR.

Typical Applications

6800 Interface

Ratiometric with Full-Scale Adjust

Note: before using caps at $V_{IN}$ or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.
Typical Applications (Continued)

Absolute with a 2.500V Reference

Zero-Shift and Span Adjust: 2V ≤ V_{IN} ≤ 5V

Span Adjust: 0V ≤ V_{IN} ≤ 3V

*For low power, see also LM385–2.5

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
Typical Applications (Continued)

Directly Converting a Low-Level Signal

V_{REF}/2 = 256 mV

A µP Interfaced Comparator

For:
V_{IN}(+) > V_{IN}(-)
Output=FF_{HEX}
For:
V_{IN}(+) < V_{IN}(-)
Output=00_{HEX}

1 mV Resolution with µP Controlled Range

V_{REF}/2 = 128 mV
1 LSB = 1 mV
V_{DAC} ≤ V_{IN} ≤ (V_{DAC} + 256 mV)
0 ≤ V_{DAC} < 2.5V
Typical Applications (Continued)

Digitizing a Current Flow

Self-Clocking Multiple A/Ds

External Clocking

* Use a large R value to reduce loading at CLK R output.
**Typical Applications (Continued)**

**Self-Clocking in Free-Running Mode**

*After power-up, a momentary grounding of the WR input is needed to guarantee operation.*

**µP Interface for Free-Running A/D**

**Operating with “Automotive” Ratiometric Transducers**

*V_{IN}(-)=0.15 V_{CC}*

15% of V_{CC} ≤ V_{XDR} ≤ 85% of V_{CC}

**Ratiometric with V_{REF}/2 Forced**

**µP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)**

*See Figure 5 to select R value DB7=1 for V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)*

Omit circuitry within the dotted area if hysteresis is not needed
**Typical Applications** (Continued)

**Handling ±10V Analog Inputs**

![Diagram](DS005671-70)

*Beckman Instruments #694-3-R10K resistor array

**Low-Cost, µP Interfaced, Temperature-to-Digital Converter**

![Diagram](DS005671-71)

**µP Interfaced Temperature-to-Digital Converter**

![Diagram](DS005671-72)

* Circuit values shown are for $0^\circ C \leq T_A \leq +128^\circ C$

***Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.***
Typical Applications (Continued)

Handling ±5V Analog Inputs

![Handling ±5V Analog Inputs Diagram]

*Beckman Instruments #694-3-R10K resistor array

μP Interfaced Comparator with Hysteresis

![μP Interfaced Comparator with Hysteresis Diagram]

Diodes are 1N914

Read-Only Interface

![Read-Only Interface Diagram]

Protecting the Input

![Protecting the Input Diagram]
Typical Applications (Continued)

Analog Self-Test for a System

A Low-Cost, 3-Decade Logarithmic Converter

*LM389 transistors
A, B, C, D = LM324A quad op amp
Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

A, B, C, D = LM324A

Noise Filtering the Analog Input

fc = 20 Hz
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

Output Buffers with A/D Data Enabled

*A/D output data is updated 1 CLK period prior to assertion of INTR

Increasing Bus Drive and/or Reducing Time on Bus

*Allows output data to set-up at falling edge of CS
**Typical Applications (Continued)**

1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the \( V_{REF} /2 \) pin). The digital output codes that correspond to these inputs are shown as \( D-1, D, \) and \( D+1 \). For the perfect A/D, not only will center-value (\( A-1, A, A+1, \ldots \)) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located \( \pm 1/2 \) LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend

---

**Note 11:** Oversample whenever possible [keep \( f_s > 2 f(-60) \)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

**Note 12:** Consider the amplitude errors which are introduced within the passband of the filter.
Functional Description (Continued)

±1/2 LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

*Figure 2* shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±1/4 LSB. In other words, if we apply an analog input equal to the center-value ±1/4 LSB, we guarantee that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than 1/2 LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +1/2 LSB because the digital code appeared 1/2 LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

---

**FIGURE 1. Clarifying the Error Specs of an A/D Converter**

Accuracy=±0 LSB: A Perfect A/D

**FIGURE 2. Clarifying the Error Specs of an A/D Converter**

Accuracy=±1/4 LSB
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage \( [V_{IN(+)} - V_{IN(-)}] \) to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted (INTR makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting INTR to the WR input with CS = 0. To ensure start-up under all possible conditions, an external WR pulse is required during the first power-up cycle.

On the high-to-low transition of the WR input the internal SAR latches and the shift register stages are reset. As long as the CS input and WR input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.

A functional diagram of the A/D converter is shown in Figure 4. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having CS and WR simultaneously low. This sets the start flip-flop (F/F) and the resulting “1” level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a “1” to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this “1” to the Q output of F/F1. The AND gate, G1, combines this “1” output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either WR or CS is a “1”) the start F/F is reset and the 8-bit shift register then can have the “1” clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a “1” level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide CS and WR signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.
After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the INTR input signal.

Note that this SET control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at 1/8 of the frequency of the external clock). If the data output is continuously enabled (CS and RD both held low), the INTR output will still signal the end of conversion (by a high-to-low transition), because the SET input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This INTR output will therefore stay low for the duration of the SET signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When data is to be read, the combination of both CS and RD being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs (CS, RD, and WR) meet standard T2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the CS input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the WR input (pin 3) and the Output Enable function is caused by an active low pulse at the RD input (pin 2).
Functional Description (Continued)

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The \( V_{IN}(-) \) input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling \( V_{IN}(+) \) and \( V_{IN}(-) \) is 4-1/2 clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

\[
\Delta V_e(\text{MAX}) = (V_p) \left( \frac{4.5}{f_{\text{CLK}}} \right)
\]

where:
- \( \Delta V_e \) is the error voltage due to sampling delay
- \( V_p \) is the peak value of the common-mode voltage
- \( f_{\text{cm}} \) is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, \( f_{\text{cm}} \), and using a 640 kHz A/D clock, \( f_{\text{CLK}} \), would allow a peak value of the common-mode voltage, \( V_p \), which is given by:

\[
V_p = \frac{\Delta V_e(\text{MAX})}{(2\pi f_{\text{cm}})(4.5)}
\]

or

\[
V_p = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)}(4.5)
\]

which gives

\[ V_p \approx 1.9\text{V}. \]

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in Figure 5.

Fault Mode

If the voltage source applied to the \( V_{IN}(+) \) or \( V_{IN}(-) \) pin exceeds the allowed operating range of \( V_{CC}+50\text{mV} \), large input currents can flow through a parasitic diode to the \( V_{CC} \) pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the \( V_{CC} \) pin (with the current bypassed with this diode, the voltage at the \( V_{IN}(+) \) pin can exceed the \( V_{CC} \) voltage by the forward voltage of this diode).

2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the \( V_{IN}(+) \) input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the \( V_{IN}(+) \) input at 5V, this DC current is at a maximum of approximately 5 \( \mu\text{A} \). Therefore, bypass capacitors should not be used at the analog inputs or the \( V_{\text{REF}}/2 \) pin for high resistance sources (> 1 k\( \Omega \)). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (< 1 k\( \Omega \)) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (< 1 k\( \Omega \)), a 0.1 \( \mu\text{F} \) bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long
Functional Description (Continued)

2.3.4 Noise
The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust \( V_{\text{REF}/2} \)) for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust
For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V\(_{\text{DC}}\), 2.5 V\(_{\text{DC}}\) or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 6.

Notice that the reference voltage for the IC is either \( V_{\text{CC}} \) supply pin, or is equal to the voltage that is externally forced at the \( V_{\text{REF}/2} \) pin. This allows for a ratiometric voltage reference using the \( V_{\text{CC}} \) supply. A 5 V\(_{\text{DC}}\) reference voltage can be used for the \( V_{\text{CC}} \) supply or a voltage less than 2.5 V\(_{\text{DC}}\) can be applied to the \( V_{\text{REF}/2} \) input for increased application flexibility. The internal gain to the \( V_{\text{REF}/2} \) input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V\(_{\text{DC}}\) to 3.5 V\(_{\text{DC}}\), instead of 0 V to 5 V\(_{\text{DC}}\), the span would be 3V as shown in Figure 7. With 0.5 V\(_{\text{DC}}\) applied to the \( V_{\text{IN}(-)} \) pin to absorb the offset, the reference voltage can be made equal to \( \frac{1}{2} \) of the 3V span or 1.5 V\(_{\text{DC}}\). The A/D now will encode the \( V_{\text{IN}(+)} \) signal from 0.5V to 3.5 V\(_{\text{DC}}\) with the 0.5V input corresponding to zero and the 3.5 V\(_{\text{DC}}\) input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

2.4.2 Reference Accuracy Requirements
The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For \( V_{\text{REF}/2} \) voltages of 2.4 V\(_{\text{DC}}\) nominal value, initial errors of ±10 mV\(_{\text{DC}}\) will cause conversion errors of ±1 LSB due to the gain of 2 of the \( V_{\text{REF}/2} \) input. In reduced span applications, the initial value and the stability of the \( V_{\text{REF}/2} \) input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the \( V_{\text{REF}/2} \) input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over 0°C to 70°C. Other temperature range parts are also available.

FIGURE 6. The \( V_{\text{REFERENCE}} \) Design on the IC

DS005671-15
2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, \( V_{IN(MIN)} \), is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D \( V_{IN(-)} \) input at this \( V_{IN(MIN)} \) value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the \( V_{IN(-)} \) input and applying a small magnitude positive voltage to the \( V_{IN(+)\text{ offset zero}} \) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal \( \frac{1}{2} \text{ LSB} \) value (\( \frac{1}{2} \text{ LSB} = 9.8 \text{ mV} \) for \( V_{REF}/2 = 2.500 \text{ V DC} \)).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is \( \frac{1}{2} \text{ LSB} \) less than the desired analog full-scale voltage range and then adjusting the magnitude of the \( V_{REF}/2 \) input (pin 9 or the \( V_{CC} \) supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A \( V_{IN(+)\text{ offset zero}} \) voltage that equals this desired zero reference plus \( \frac{1}{2} \text{ LSB} \) (where the LSB is calculated for the desired analog span, \( 1 \text{ LSB} = \text{analog span}/256 \)) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the 00\text{HEX} to 01\text{HEX} code transition.

The full-scale adjustment should then be made (with the proper \( V_{IN(-)} \) voltage applied) by forcing a voltage to the \( V_{IN(+)\text{ offset zero}} \) input which is given by:

\[
V_{IN(+)} = V_{MAX} - 1.5 \left( \frac{V_{MAX} - V_{MIN}}{256} \right)
\]

where:

- \( V_{MAX} \) = The high end of the analog input range
- \( V_{MIN} \) = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The \( V_{REF}/2 \) (or \( V_{CC} \)) voltage is then adjusted to provide a code change from FE\text{HEX} to FF\text{HEX}. This completes the adjustment procedure.

2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 8.

FIGURE 7. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range
2.10 Power Supplies

Noise spikes on the VCC supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter VCC pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the VCC supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground point should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any VREF/2 bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of 1/4 LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 9.

For ease of testing, the VREF/2 (pin 9) should be supplied with 2.560 VDC and a VCC supply voltage of 5.12 VDC should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 VDC (5.120 – 1/2 LSB) should be applied to the V IN(+)+ pin with the V IN(−) pin grounded. The value of the VREF/2 input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of VREF/2 should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) voltages obtained from the “VMS” and “VLS” columns in Table 1 shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the “VMS” and “VLS” columns in Table 1, the nominal value of the digital display (when VREF/2 = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 VDC. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.
For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in Figure 8. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, “A–C”, directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of Figure 11, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides 1/4 LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB’s) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user’s program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for CS and the MEMR and MEMW strobes) or it can be controlled as an I/O device by using the I/O R and I/O W strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the CS input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in Figure 12.
TABLE 1. DECODING THE DIGITAL OUTPUT LEDS

<table>
<thead>
<tr>
<th>HEX</th>
<th>BINARY</th>
<th>FRACTIONAL BINARY VALUE FOR CENTER VALUES WITH $V_{REF}/2=2.560,V_{DC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>MS GROUP</strong></td>
</tr>
<tr>
<td>F</td>
<td>1111</td>
<td>15/16</td>
</tr>
<tr>
<td>E</td>
<td>1110</td>
<td>7/8</td>
</tr>
<tr>
<td>D</td>
<td>1101</td>
<td>13/16</td>
</tr>
<tr>
<td>C</td>
<td>1100</td>
<td>3/4</td>
</tr>
<tr>
<td>B</td>
<td>1011</td>
<td>11/16</td>
</tr>
<tr>
<td>A</td>
<td>1010</td>
<td>5/8</td>
</tr>
<tr>
<td>9</td>
<td>1001</td>
<td>9/16</td>
</tr>
<tr>
<td>8</td>
<td>1000</td>
<td>1/2</td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td>7/16</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>3/8</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>5/16</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>1/4</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>3/16</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>1/8</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>1/16</td>
</tr>
<tr>
<td>0</td>
<td>0000</td>
<td>00</td>
</tr>
</tbody>
</table>

**Note 15:** Display Output = VMS Group + VLS Group
**Note 16:** Pin numbers for the DP8228 system controller, others are INS8080A.

**Note 17:** Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

**FIGURE 12. ADC0801_INS8080A CPU Interface**
Note 18: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

Note 19: All address used were arbitrarily chosen.

The standard control bus signals of the 8080 CS, RD and WR can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in Figure 12 may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate CS for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as CS inputs—one for each I/O device.

4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see Figure 13) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals RD, WR and INT of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The RD and WR signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.
Functional Description (Continued)

4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General RD and WR strobes are provided and separate memory request, MREQ, and I/O request, IORQ, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the RD and WR strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 14.

SAMPLE PROGRAM FOR Figure 13 INS8048 INTERFACE

```
04 10  JMP  10H  : Program starts at addr 10
04 50  JMP  50H  : Interrupt jump vector
          JMP  10H  : Main program
99 FE  ANL  P1, #0FEH     ; Chip select
     MOVX  A, @R1  ; Read the lst data
          MOVX  A, @R1,A  ; to reset the intr
89 01  ORL  P1, #1       ; Set port pin high
88 20  MOV  R0, #20H     ; Data address
89 FF  MOV  R1, #0FH     ; Dummy address
BA 10  MOV  R2, #10H     ; Counter for 16 bytes
23 FF  MOV  A, #0FH      ; Set ACC for intr loop
99 FE  ANL  P1, #0FEH    ; Send CS (bit 0 of P1)
91    MOVX  A, @R1, A    ; Send WR out
05    EN I               ; Enable interrupt
96 21  JNZ  LOOP        ; Wait for interrupt
EA 1B  DJNZ  R2, AGAIN   ; If 16 bytes are read
00    NOP               ; go to user's program
00    NOP
81    MOVX  A, @R1      ; Input data, CS still low
A0    MOV  @R0, A       ; Store in memory
18    INC  R0           ; Increment storage counter
89 01  ORL  P1, #1      ; Reset CS signal
27    CLR A             ; Clear ACC to get out of
93    RETR             ; the interrupt loop

FIGURE 13. INS8048 Interface

FIGURE 14. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to
**Functional Description** (Continued)

A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the φ2 clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 15 shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the CS decoding is shown using 1/2 DM8092. Note that in many 6800 systems, an already decoded 4/5 line is brought out to the common bus at pin 21. This can be tied directly to the CS pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In Figure 16 the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the CS pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no CS decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D RD pin can be grounded.

A sample interface program equivalent to the previous one is shown below Figure 16. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in Figure 17.

---

Note 20: Numbers in parentheses refer to MC6800 CPU pin out.

Note 21: Number or letters in brackets refer to standard M6800 system common bus code.

**FIGURE 15. ADC0801-MC6800 CPU Interface**
Functional Description (Continued)

### SAMPLE PROGRAM FOR Figure 15 ADC0801-MC6800 CPU INTERFACE

| 0010 | DF 36      | DATAIN | STX   | TEMP2 | ; Save contents of X |
| 0012 | CE 00 2C   |        | LDX   | #$002C| ; Upon IRQ low CPU |
| 0015 | FF FF FF   | STX    | #$FF8 |       | ; jumps to 002C     |
| 0018 | B7 50 00   | STAA   | #$5000|       | ; Start ADC0801     |
| 001B | 0E         |        | CLI   |       |                   |
| 001C | 3E         |        | CONVRT| WAI   | ; Wait for interrupt|
| 001D | DE 34      |        | LDX   | TEMP1 |                   |
| 001F | 8C 02 0F   |        | CFX   | #$020F| ; Is final data stored? |
| 0022 | 27 14      |        | BEQ   | ENDF  |                   |
| 0024 | B7 50 00   |        | STAA  | #$5000| ; Repeats ADC0801   |
| 0027 | 08         |        | INX   |       |                   |
| 0028 | DF 34      |        | STX   | TEMP1 |                   |
| 002A | 20 F0      |        | BRA   | CONVRT|                   |
| 002C | DE 34      |        | INTRPT| LDX   | TEMP1              |
| 002E | B6 50 00   |        | LDAA  | #$5000| ; Read data        |
| 0031 | A7 00      |        | STAA  | X     | ; Store it at X    |
| 0033 | 3B         |        | RTI   |       |                   |
| 0034 | 02 00      |        | TEMP1 | FDB   | $0200              |
| 0038 | CE 0D 00   |        | LDAA  | #$0000| ; Starting address for storage |
| 0039 | EE 00 00   |        | ENDF  | LDX   | #$0200             |
| 003B | DF 34      |        | STX   | TEMP1 | ; Reinitialize TEMP1|
| 003D | DE 34      |        | LDX   | TEMP2 |                   |
| 003F | 39         |        | RTS   |       | ; Return from subroutine |
|       |            |        |       |       | ; User's program    |

**Note 22:** In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

![Diagram](DS005671-A1)

**Figure 16. ADC0801–MC6820 PIA Interface**

(See diagram for connections and labels.)

---

www.national.com 30
The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the CS inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user’s program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user’s program. All CPU registers then recover the original data they had before servicing DATA IN.

5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.
Note 23: Numbers in parentheses refer to MC6800 CPU pin out.

Note 24: Numbers of letters in brackets refer to standard M6800 system common bus code.

FIGURE 17. Interfacing Multiple A/Ds in an MC6800 System
Functional Description (Continued)

Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user’s program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. Figure 18 is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 µV for 1/4 LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

\[ V_o = \left[ (V_{IN}^+) - (V_{IN}^-) \right] + \left[ 1 + \frac{2R_2}{R_1} \right] \]

\[ = \left[ (V_{OS2} - V_{OS1} - V_{OS3} \pm I_X R_X) \right] + \left[ 1 + \frac{2R_2}{R_1} \right] \]

where \( I_X \) is the current through resistor \( R_X \). All of the offset error terms can be cancelled by making \( \frac{2I_X R_X}{R_1} = V_{OS1} + V_{OS3} - V_{OS2} \). This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programmable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in Figure 19. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp’s differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at \( V_x \) increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic “1” (5V) on

---

**Functional Description (Continued)**

**SAMPLE PROGRAM FOR Figure 17 INTERFACING MULTIPLE A/D’s IN AN MC6800 SYSTEM**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>HEX CODE</th>
<th>MNEMONICS</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0010</td>
<td>DF 44</td>
<td>DATAIN</td>
<td>; Save Contents of X</td>
</tr>
<tr>
<td>0012</td>
<td>CE 00 2A</td>
<td>LDX</td>
<td>; Upon IRQ LOW CPU</td>
</tr>
<tr>
<td>0015</td>
<td>FF FF F8</td>
<td>STX</td>
<td>; Jumps to 002A</td>
</tr>
<tr>
<td>0018</td>
<td>B7 50 00</td>
<td>STAA</td>
<td>; Starts all A/D’s</td>
</tr>
<tr>
<td>001B</td>
<td>0E</td>
<td>CLI</td>
<td>; Wait for interrupt</td>
</tr>
<tr>
<td>001C</td>
<td>3E</td>
<td>WAI</td>
<td>; Return from subroutine</td>
</tr>
<tr>
<td>001D</td>
<td>CE 50 00</td>
<td>LDX</td>
<td>; INDEX1</td>
</tr>
<tr>
<td>0020</td>
<td>DF 40</td>
<td>STX INDEX</td>
<td>; Reset both INDEX</td>
</tr>
<tr>
<td>0022</td>
<td>CE 02 00</td>
<td>LDX INDEX</td>
<td>; 1 and 2 to starting</td>
</tr>
<tr>
<td>0025</td>
<td>DF 42</td>
<td>STX INDEX2</td>
<td>; addresses</td>
</tr>
<tr>
<td>0027</td>
<td>DE 44</td>
<td>LDX TEMP</td>
<td>; INDEX2</td>
</tr>
<tr>
<td>0029</td>
<td>39</td>
<td>RTS</td>
<td>; Return from subroutine</td>
</tr>
<tr>
<td>002A</td>
<td>DE 40</td>
<td>INTRPT LDX</td>
<td>; INDEX1</td>
</tr>
<tr>
<td>002C</td>
<td>A6 00</td>
<td>LDAA X</td>
<td>; Read data in from A/D at X</td>
</tr>
<tr>
<td>002E</td>
<td>08</td>
<td>INX</td>
<td>; Increment X by one</td>
</tr>
<tr>
<td>002F</td>
<td>DF 40</td>
<td>STX INDEX1</td>
<td>; X → INDEX1</td>
</tr>
<tr>
<td>0031</td>
<td>DE 42</td>
<td>LDX INDEX2</td>
<td>; INDEX2 → X</td>
</tr>
</tbody>
</table>

**SAMPLE PROGRAM FOR Figure 17 INTERFACING MULTIPLE A/D’s IN AN MC6800 SYSTEM**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>HEX CODE</th>
<th>MNEMONICS</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0033</td>
<td>A7 00</td>
<td>STAA X</td>
<td>; Store data at X</td>
</tr>
<tr>
<td>0035</td>
<td>8C 02 07</td>
<td>CPX #$0207</td>
<td>; Have all A/D’s been read?</td>
</tr>
<tr>
<td>0038</td>
<td>27 05</td>
<td>BEQ RETURN</td>
<td>; Yes: branch to RETURN</td>
</tr>
<tr>
<td>003A</td>
<td>08</td>
<td>INX</td>
<td>; No: increment X by one</td>
</tr>
<tr>
<td>003B</td>
<td>DF 42</td>
<td>STX INDEX2</td>
<td>; X → INDEX2</td>
</tr>
<tr>
<td>003D</td>
<td>20 EB</td>
<td>BRA INTRPT</td>
<td>; Branch to 002A</td>
</tr>
<tr>
<td>003F</td>
<td>3B</td>
<td>RETURN RTI</td>
<td></td>
</tr>
<tr>
<td>0040</td>
<td>50 00</td>
<td>INDEX1 FDB</td>
<td>$5000 ; Starting address for A/D</td>
</tr>
<tr>
<td>0042</td>
<td>02 00</td>
<td>INDEX2 FDB</td>
<td>$0200 ; Starting address for data storage</td>
</tr>
<tr>
<td>0044</td>
<td>00 00</td>
<td>TEMP FDB</td>
<td>$0000</td>
</tr>
</tbody>
</table>

Note 25: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user’s program.
Functional Description (Continued)

any output of Port B will source current into node \( V_X \) thus raising the voltage at \( V_X \) and making the output differential more negative. Conversely, a logic “0” (0V) will pull current out of node \( V_X \) and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, \( V_X \) can move \( \pm 12 \text{ mV} \) with a resolution of 50 \( \mu \text{V} \), which will null the offset error term to \( \frac{1}{4} \) LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Note 26: \( R_2 = 49.5 \ R_1 \)

Note 27: Switches are LMC13334 CMOS analog switches.

Note 28: The 9 resistors used in the auto-zero section can be \( \pm 5\% \) tolerance.

FIGURE 18. Gain of 100 Differential Transducer Preamp
Functional Description (Continued)

A flow chart for the zeroing subroutine is shown in Figure 20. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input \( V_{IN}(-) \geq V_{IN}(+) \). Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull \( V_X \) more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make \( V_X \) more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in Figure 21. All addresses used are compatible with the BLC 80/10 microcomputer system.

In particular:
- Port A and the ADC0801 are at port address E4
- Port B is at port address E5
- Port C is at port address E6
- PPI control word port is at port address E7
- Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. Figure 22 and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion (INTR asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the INTR outputs of all the converters. Each converter which initiates an interrupt will place a logic “0” in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.
FIGURE 20. Flow Chart for Auto-Zero Routine
Functional Description (Continued)

5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode (Continued)

The following notes apply:

• It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

• The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

• A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X3E00.

• The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

• The peripherals of concern are mapped into I/O space with the following port assignments:
### Functional Description (Continued)

<table>
<thead>
<tr>
<th>HEX PORT ADDRESS</th>
<th>PERIPHERAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>MM74C374 8-bit flip-flop</td>
</tr>
<tr>
<td>01</td>
<td>A/D 1</td>
</tr>
<tr>
<td>02</td>
<td>A/D 2</td>
</tr>
<tr>
<td>03</td>
<td>A/D 3</td>
</tr>
<tr>
<td>04</td>
<td>A/D 4</td>
</tr>
<tr>
<td>05</td>
<td>A/D 5</td>
</tr>
<tr>
<td>06</td>
<td>A/D 6</td>
</tr>
<tr>
<td>07</td>
<td>A/D 7</td>
</tr>
</tbody>
</table>

This port address also serves as the A/D identifying word in the program.

![Multiple A/Ds with Z-80 Type Microprocessor](image-url)

**FIGURE 22.** Multiple A/Ds with Z-80 Type Microprocessor
INTERRUPT SERVICING SUBROUTINE

<table>
<thead>
<tr>
<th>LOC</th>
<th>OBJ CODE</th>
<th>SOURCE STATEMENT</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0038</td>
<td>E5</td>
<td>PUSH HL</td>
<td>Save contents of all registers affected by</td>
</tr>
<tr>
<td>0039</td>
<td>C5</td>
<td>PUSH BC</td>
<td>this subroutine.</td>
</tr>
<tr>
<td>003A</td>
<td>F5</td>
<td>PUSH AF</td>
<td>Assumed INT mode earlier set.</td>
</tr>
<tr>
<td>003B</td>
<td>21 00 3E</td>
<td>LD (HL), X3E00</td>
<td>Initialize memory pointer where data will be stored.</td>
</tr>
<tr>
<td>003E</td>
<td>0E 01</td>
<td>LD C, X01</td>
<td>C register will be port ADDR of A/D converters.</td>
</tr>
<tr>
<td>0040</td>
<td>D300</td>
<td>OUT X00, A</td>
<td>Load peripheral status word into 8-bit latch.</td>
</tr>
<tr>
<td>0042</td>
<td>DB00</td>
<td>IN A, X00</td>
<td>Load status word into accumulator.</td>
</tr>
<tr>
<td>0044</td>
<td>47</td>
<td></td>
<td>Save the status word.</td>
</tr>
<tr>
<td>0045</td>
<td>79</td>
<td>TEST</td>
<td>Test to see if the status of all A/D's have</td>
</tr>
<tr>
<td>0046</td>
<td>FE 08</td>
<td>CP, X08</td>
<td>been checked. If so, exit subroutine</td>
</tr>
<tr>
<td>0048</td>
<td>CA 80 00</td>
<td>JPZ, DONE</td>
<td></td>
</tr>
<tr>
<td>004B</td>
<td>78</td>
<td>LD A, B</td>
<td>Test a single bit in status word by looking for</td>
</tr>
<tr>
<td>004C</td>
<td>1F</td>
<td>RRA</td>
<td>a &quot;1&quot; to be rotated into the CARRY (an INT</td>
</tr>
<tr>
<td>004D</td>
<td>47</td>
<td>LD B, A</td>
<td>is loaded as a &quot;1&quot;). If CARRY is set then load</td>
</tr>
<tr>
<td>004E</td>
<td>DA 5500</td>
<td>JPC, LOAD</td>
<td>contents of A/D at port ADDR in C register.</td>
</tr>
<tr>
<td>0051</td>
<td>0C</td>
<td>NEXT</td>
<td>If CARRY is not set, increment C register to point</td>
</tr>
<tr>
<td>0052</td>
<td>C3 4500</td>
<td>JP, TEST</td>
<td>to next A/D, then test next bit in status word.</td>
</tr>
<tr>
<td>0055</td>
<td>ED 78</td>
<td>LOAD</td>
<td>Read data from interrupting A/D and invert</td>
</tr>
<tr>
<td>0057</td>
<td>EE FF</td>
<td>XOR FF</td>
<td>the data.</td>
</tr>
<tr>
<td>0059</td>
<td>77</td>
<td>LD (HL), A</td>
<td>Store the data</td>
</tr>
<tr>
<td>005A</td>
<td>2C</td>
<td>INC L</td>
<td></td>
</tr>
<tr>
<td>005B</td>
<td>71</td>
<td>LD (HL), C</td>
<td>Store A/D identifier (A/D port ADDR).</td>
</tr>
<tr>
<td>005C</td>
<td>2C</td>
<td>INC L</td>
<td></td>
</tr>
<tr>
<td>005D</td>
<td>C3 51 00</td>
<td>JP, NEXT</td>
<td>Test next bit in status word.</td>
</tr>
<tr>
<td>0060</td>
<td>F1</td>
<td>DONE</td>
<td>Re-establish all registers as they were</td>
</tr>
<tr>
<td>0061</td>
<td>C1</td>
<td>POP BC</td>
<td>before the interrupt.</td>
</tr>
<tr>
<td>0062</td>
<td>E1</td>
<td>POP HL</td>
<td></td>
</tr>
<tr>
<td>0063</td>
<td>C9</td>
<td>RET</td>
<td>Return to original program</td>
</tr>
</tbody>
</table>
LIFE SUPPORT POLICY

NATIONAL’S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor
Corporation
Americas
Email: support@nsc.com

National Semiconductor
Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

www.national.com

National Semiconductor
Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor
Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.
SHARP's GP2D12/GP2D15 are general purpose type distance measuring sensors which consist of PSD* and infrared emitting diode and signal processing circuit. It enables to detect objects without any influence on the color of reflective objects, reflectivity, the lights of surroundings.

*PSD: Position Sensitive Detector

### Features

1. Less influence on the color of reflective objects, reflectivity
2. Line-up of distance output/distance judgement type
   - Distance output type (analog voltage): GP2D12
   - Detecting distance: 10 to 80cm
   - Distance judgement type: GP2D15
   - Judgement distance: 24cm (Adjustable within the range of 10 to 80cm)
3. External control circuit is unnecessary.
4. Low cost

### Applications

1. TVs
2. Personal computers
3. Cars
4. Copiers

---

(Notice) • In the absence of device specification sheets, SHARP takes no responsibility for any defects that may occur in equipment using any SHARP device shown in catalogs, data books, etc. Contact SHARP in order to obtain the latest device specification sheets before using any SHARP device.

• Specifications are subject to change without notice for improvement.

(Internet) • Data for SHARP's optoelectronic/power device is provided on internet. (Address http://www.sharp.co.jp/ecg/)
## Specifications

### GP2D12

Parameter | Symbol | Rating  | (Ta=25°C)
--- | --- | --- | ---
Supply voltage | Vcc | 4.5 to 5.5V | |
Dissipation current | Icc | MAX.35mA | |
Measuring range | L | 10 to 80cm | |
Output type | | Analog output | |
Operating temperature | Topr | -10 to +60°C | |

### GP2D15

Parameter | Symbol | Rating  | (Ta=25°C)
--- | --- | --- | ---
Supply voltage | Vcc | 4.5 to 5.5V | |
Dissipation current | Icc | MAX.35mA | |
Judgement distance | L | TYP.24cm | |
Output type | | Digital output | |
Operating temperature | Topr | -10 to +60°C | |

* Adjustable within the range of 10 to 80cm. <Custom products>
Features
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

Description
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel’s high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

Pin Configurations

AT89C51

Not Recommended for New Designs. Use AT89S51.
The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

**VCC**
Supply voltage.

**GND**
Ground.

**Port 0**
Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

**Port 1**
Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pullups. Port 1 also receives the low-order address bytes during Flash programming and verification.

**Port 2**
Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

**Port 3**
Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pullups. Port 3 also serves the functions of various special features of the AT89C51 as listed below:

<table>
<thead>
<tr>
<th>Port Pin</th>
<th>Alternate Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P3.0</td>
<td>RXD (serial input port)</td>
</tr>
<tr>
<td>P3.1</td>
<td>TXD (serial output port)</td>
</tr>
<tr>
<td>P3.2</td>
<td>INT0 (external interrupt 0)</td>
</tr>
<tr>
<td>P3.3</td>
<td>INT1 (external interrupt 1)</td>
</tr>
<tr>
<td>P3.4</td>
<td>T0 (timer 0 external input)</td>
</tr>
<tr>
<td>P3.5</td>
<td>T1 (timer 1 external input)</td>
</tr>
<tr>
<td>P3.6</td>
<td>WR (external data memory write strobe)</td>
</tr>
<tr>
<td>P3.7</td>
<td>RD (external data memory read strobe)</td>
</tr>
</tbody>
</table>

Port 3 also receives some control signals for Flash programming and verification.

**RST**
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

**ALE/PROG**
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE
pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP
External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Oscillator Characteristics
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

<table>
<thead>
<tr>
<th>Mode</th>
<th>Program Memory</th>
<th>ALE</th>
<th>PSEN</th>
<th>PORT0</th>
<th>PORT1</th>
<th>PORT2</th>
<th>PORT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>Internal</td>
<td>1</td>
<td>1</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Idle</td>
<td>External</td>
<td>1</td>
<td>1</td>
<td>Float</td>
<td>Data</td>
<td>Address</td>
<td>Data</td>
</tr>
<tr>
<td>Power-down</td>
<td>Internal</td>
<td>0</td>
<td>0</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
<tr>
<td>Power-down</td>
<td>External</td>
<td>0</td>
<td>0</td>
<td>Float</td>
<td>Data</td>
<td>Data</td>
<td>Data</td>
</tr>
</tbody>
</table>

Note: C1, C2 = 30 pF ± 10 pF for Crystals = 40 pF ± 10 pF for Ceramic Resonators
Power-down Mode
In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $V_{CC}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits
On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\text{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\text{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

<table>
<thead>
<tr>
<th>Program Lock Bits</th>
<th>Protection Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>LB1</td>
<td>LB2</td>
</tr>
<tr>
<td>1</td>
<td>U</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
</tr>
<tr>
<td>3</td>
<td>P</td>
</tr>
<tr>
<td>4</td>
<td>P</td>
</tr>
</tbody>
</table>
Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low-voltage programming mode provides a convenient way to program the AT89C51 inside the user’s system, while the high-voltage programming mode is compatible with conventional third-party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

<table>
<thead>
<tr>
<th>V_{PP} = 12V</th>
<th>V_{PP} = 5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top-side Mark</td>
<td>AT89C51</td>
</tr>
<tr>
<td></td>
<td>xxxx-5</td>
</tr>
<tr>
<td></td>
<td>yyyy</td>
</tr>
<tr>
<td>Signature</td>
<td>(030H) = 1EH</td>
</tr>
<tr>
<td></td>
<td>(031H) = 51H</td>
</tr>
<tr>
<td></td>
<td>(032H) = F FH</td>
</tr>
<tr>
<td></td>
<td>(030H) = 1EH</td>
</tr>
<tr>
<td></td>
<td>(031H) = 51H</td>
</tr>
<tr>
<td></td>
<td>(032H) = 05H</td>
</tr>
</tbody>
</table>

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figure 3 and Figure 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise E{AA/V}_{PP} to 12V for the high-voltage programming mode.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all “1”s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 51H indicates 89C51
- (032H) = FFH indicates 12V programming
- (032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.
## Flash Programming Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>RST</th>
<th>PSEN</th>
<th>ALE/PROG</th>
<th>EA/V&lt;sub&gt;pp&lt;/sub&gt;</th>
<th>P2.6</th>
<th>P2.7</th>
<th>P3.6</th>
<th>P3.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Code Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Read Code Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>Write Lock Bit - 1</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>Chip Erase</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>Read Signature Byte</td>
<td>H</td>
<td>L</td>
<td></td>
<td>H/12V</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

Note: 1. Chip Erase requires a 10 ms PROG pulse.

**Figure 3.** Programming the Flash

**Figure 4.** Verifying the Flash
Flash Programming and Verification Waveforms - High-voltage Mode ($V_{pp} = 12V$)

- **P1.0 - P1.7**
- **P2.0 - P2.3**

PORT 0

ALE/PROG

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

DATA IN

$V_{pp}$

DATA OUT

LOGIC 1

LOGIC 0

Flash Programming and Verification Waveforms - Low-voltage Mode ($V_{pp} = 5V$)

- **P1.0 - P1.7**
- **P2.0 - P2.3**

PORT 0

ALE/PROG

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

DATA IN

LOGIC 1

LOGIC 0

DATA OUT

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$

$P1.0 - P1.7$

$P2.0 - P2.3$

$ALE/PROG$

$EA/V_{pp}$

$P2.7$ (ENABLE)

$P3.4$ (RDY/BSY)

$V_{pp}$
### Flash Programming and Verification Characteristics

\( T_A = 0^\circ \text{C to 70}^\circ \text{C}, \ V_{CC} = 5.0 \pm 10\% \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{PP} ) (^{(1)})</td>
<td>Programming Enable Voltage</td>
<td>11.5</td>
<td>12.5</td>
<td>V</td>
</tr>
<tr>
<td>( I_{PP} ) (^{(1)})</td>
<td>Programming Enable Current</td>
<td>1.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( 1/t_{CLCL} )</td>
<td>Oscillator Frequency</td>
<td>3</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>( t_{AVGL} )</td>
<td>Address Setup to PROG Low</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{GHAX} )</td>
<td>Address Hold after PROG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DVGL} )</td>
<td>Data Setup to PROG Low</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{GHOX} )</td>
<td>Data Hold after PROG</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{EHSH} )</td>
<td>P2.7 (ENABLE) High to ( V_{PP} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SHGL} )</td>
<td>( V_{PP} ) Setup to PROG Low</td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>( t_{GHSL} ) (^{(1)})</td>
<td>( V_{PP} ) Hold after PROG</td>
<td>10</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>( t_{GLGH} )</td>
<td>PROG Width</td>
<td>1</td>
<td>110</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{AVQV} )</td>
<td>Address to Data Valid</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{ELQV} )</td>
<td>ENABLE Low to Data Valid</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{EHQZ} )</td>
<td>Data Float after ENABLE</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{GHBL} )</td>
<td>PROG High to BUSY Low</td>
<td>1.0</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>( t_{WC} )</td>
<td>Byte Write Cycle Time</td>
<td>2.0</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

**Note:** \( 1. \) Only used in 12-volt programming mode.
Absolute Maximum Ratings*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Low-voltage (Except EA)</td>
<td>-0.5</td>
<td>0.2 VCC - 0.1</td>
<td>V</td>
</tr>
<tr>
<td>VIL1</td>
<td>Input Low-voltage (EA)</td>
<td>-0.5</td>
<td>0.2 VCC - 0.3</td>
<td>V</td>
</tr>
<tr>
<td>VILH</td>
<td>Input High-voltage (Except XTAL1, RST)</td>
<td>0.2 VCC + 0.9</td>
<td>VCC + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output Low-voltage (Port 0, ALE, PSEN)</td>
<td>IOL = 1.6 mA</td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>VOH1</td>
<td>Output Low-voltage (Port 0 in External Bus Mode)</td>
<td>IOL = 3.2 mA</td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>VOH2</td>
<td>Output High-voltage (Ports 1,2,3, ALE, PSEN)</td>
<td>IOH = -60 µA, VCC = 5V ±10%</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>VOH3</td>
<td>Output High-voltage (Port 0 in External Bus Mode)</td>
<td>IOH = -25 µA</td>
<td>0.75 VCC</td>
<td>V</td>
</tr>
<tr>
<td>VOH4</td>
<td>Output High-voltage (Port 0 in External Bus Mode)</td>
<td>IOH = -10 µA</td>
<td>0.9 VCC</td>
<td>V</td>
</tr>
<tr>
<td>VOH5</td>
<td>Output High-voltage (Port 0 in External Bus Mode)</td>
<td>IOH = -800 µA, VCC = 5V ±10%</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>VOH6</td>
<td>Output High-voltage (Port 0 in External Bus Mode)</td>
<td>IOH = -300 µA</td>
<td>0.75 VCC</td>
<td>V</td>
</tr>
<tr>
<td>VOH7</td>
<td>Output High-voltage (Port 0 in External Bus Mode)</td>
<td>IOH = -80 µA</td>
<td>0.9 VCC</td>
<td>V</td>
</tr>
<tr>
<td>IL</td>
<td>Logical 0 Input Current (Ports 1,2,3)</td>
<td>VIN = 0.45V</td>
<td>-50</td>
<td>µA</td>
</tr>
<tr>
<td>ITL</td>
<td>Logical 1 to 0 Transition Current (Ports 1,2,3)</td>
<td>VIN = 2V, VCC = 5V ±10%</td>
<td>-650</td>
<td>µA</td>
</tr>
<tr>
<td>ILI</td>
<td>Input Leakage Current (Port 0, EA)</td>
<td>0.45 &lt; VIN &lt; VCC</td>
<td>±10</td>
<td>µA</td>
</tr>
<tr>
<td>RRST</td>
<td>Reset Pull-down Resistor</td>
<td></td>
<td>50</td>
<td>300</td>
</tr>
<tr>
<td>CIID</td>
<td>Pin Capacitance</td>
<td>Test Freq. = 1 MHz, TA = 25°C</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>ICC</td>
<td>Power Supply Current</td>
<td>Active Mode, 12 MHz</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Power-down Mode(2)</td>
<td>Idle Mode, 12 MHz</td>
<td>5</td>
<td>mA</td>
</tr>
</tbody>
</table>

Notes:
1. Under steady state (non-transient) conditions, IOL must be externally limited as follows:
   - Maximum IOL per port pin: 10 mA
   - Maximum IOL per 8-bit port: Port 0: 26 mA
   - Ports 1, 2, 3: 15 mA
   - Maximum total IIN for all output pins: 71 mA
   - If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum VCC for Power-down is 2V.
AC Characteristics
Under operating conditions, load capacitance for Port 0, ALE/PROG, and PSEN = 100 pF; load capacitance for all other outputs = 80 pF.

External Program and Data Memory Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Oscillator</th>
<th>16 to 24 MHz Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>1/τCLCL</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>τHLL</td>
<td>ALE Pulse Width</td>
<td>127</td>
<td>2τCLCL</td>
<td>40</td>
</tr>
<tr>
<td>τAVLL</td>
<td>Address Valid to ALE Low</td>
<td>43</td>
<td>τCLCL</td>
<td>13</td>
</tr>
<tr>
<td>τLAX</td>
<td>Address Hold after ALE Low</td>
<td>48</td>
<td>τCLCL</td>
<td>20</td>
</tr>
<tr>
<td>τLIV</td>
<td>ALE Low to Valid Instruction In</td>
<td>233</td>
<td>4τCLCL</td>
<td>65</td>
</tr>
<tr>
<td>τLLPL</td>
<td>ALE Low to PSEN Low</td>
<td>43</td>
<td>τCLCL</td>
<td>13</td>
</tr>
<tr>
<td>τPLPH</td>
<td>PSEN Pulse Width</td>
<td>205</td>
<td>3τCLCL</td>
<td>20</td>
</tr>
<tr>
<td>τPLIV</td>
<td>PSEN Low to Valid Instruction In</td>
<td>145</td>
<td>3τCLCL</td>
<td>45</td>
</tr>
<tr>
<td>τPXIX</td>
<td>Input Instruction Hold after PSEN</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>τPXIZ</td>
<td>Input Instruction Float after PSEN</td>
<td>59</td>
<td>τCLCL</td>
<td>10</td>
</tr>
<tr>
<td>τPXAV</td>
<td>PSEN to Address Valid</td>
<td>75</td>
<td>τCLCL</td>
<td>8</td>
</tr>
<tr>
<td>τAVV</td>
<td>Address to Valid Instruction In</td>
<td>312</td>
<td>5τCLCL</td>
<td>55</td>
</tr>
<tr>
<td>τPLAZ</td>
<td>PSEN Low to Address Float</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>τRLRH</td>
<td>RD Pulse Width</td>
<td>400</td>
<td>6τCLCL</td>
<td>100</td>
</tr>
<tr>
<td>τWLWH</td>
<td>WR Pulse Width</td>
<td>400</td>
<td>6τCLCL</td>
<td>100</td>
</tr>
<tr>
<td>τRLDV</td>
<td>RD Low to Valid Data In</td>
<td>252</td>
<td>5τCLCL</td>
<td>90</td>
</tr>
<tr>
<td>τRHDX</td>
<td>Data Hold after RD</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>τRHDZ</td>
<td>Data Float after RD</td>
<td>97</td>
<td>2τCLCL</td>
<td>28</td>
</tr>
<tr>
<td>τLLDV</td>
<td>ALE Low to Valid Data In</td>
<td>517</td>
<td>8τCLCL</td>
<td>150</td>
</tr>
<tr>
<td>τAVDV</td>
<td>Address to Valid Data In</td>
<td>585</td>
<td>9τCLCL</td>
<td>165</td>
</tr>
<tr>
<td>τLWL</td>
<td>ALE Low to RD or WR Low</td>
<td>200</td>
<td>300</td>
<td>3τCLCL</td>
</tr>
<tr>
<td>τAVWL</td>
<td>Address to RD or WR Low</td>
<td>203</td>
<td>4τCLCL</td>
<td>75</td>
</tr>
<tr>
<td>τQVWX</td>
<td>Data Valid to WR Transition</td>
<td>23</td>
<td>τCLCL</td>
<td>20</td>
</tr>
<tr>
<td>τQVWH</td>
<td>Data Valid to WR High</td>
<td>433</td>
<td>7τCLCL</td>
<td>120</td>
</tr>
<tr>
<td>τWHQX</td>
<td>Data Hold after WR</td>
<td>33</td>
<td>τCLCL</td>
<td>20</td>
</tr>
<tr>
<td>τRLAZ</td>
<td>RD Low to Address Float</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>τWHHL</td>
<td>RD or WR High to ALE High</td>
<td>43</td>
<td>τCLCL</td>
<td>20</td>
</tr>
</tbody>
</table>

1. AC Characteristics
2. External Program and Data Memory Characteristics
3. Table showing parameters and their values for different oscillators.
External Program Memory Read Cycle

External Data Memory Read Cycle
External Data Memory Write Cycle

![External Data Memory Write Cycle Diagram]

External Clock Drive Waveforms

![External Clock Drive Waveforms Diagram]

External Clock Drive

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{CLCL}$</td>
<td>Oscillator Frequency</td>
<td>0</td>
<td>24</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{CLCL}$</td>
<td>Clock Period</td>
<td>41.6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CHCX}$</td>
<td>High Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLCX}$</td>
<td>Low Time</td>
<td>15</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CLCH}$</td>
<td>Rise Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{CHCL}$</td>
<td>Fall Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
Serial Port Timing: Shift Register Mode Test Conditions
($V_{CC} = 5.0 \text{ V } \pm 20\%$; Load Capacitance = 80 pF)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>12 MHz Osc</th>
<th>Variable Oscillator</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>$t_{XLXL}$</td>
<td>Serial Port Clock Cycle Time</td>
<td>1.0</td>
<td>$12t_{CLCL}$</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_{QVXH}$</td>
<td>Output Data Setup to Clock Rising Edge</td>
<td>700</td>
<td>$10t_{CLCL}$</td>
<td>$-133$ ns</td>
</tr>
<tr>
<td>$t_{XHQX}$</td>
<td>Output Data Hold after Clock Rising Edge</td>
<td>50</td>
<td>$2t_{CLCL}$</td>
<td>$-117$ ns</td>
</tr>
<tr>
<td>$t_{XHDX}$</td>
<td>Input Data Hold after Clock Rising Edge</td>
<td>0</td>
<td>0</td>
<td>0 ns</td>
</tr>
<tr>
<td>$t_{XHDV}$</td>
<td>Clock Rising Edge to Input Data Valid</td>
<td>700</td>
<td></td>
<td>$10t_{CLCL}$</td>
</tr>
</tbody>
</table>

Shift Register Mode Timing Waveforms

AC Testing Input/Output Waveforms

Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5\text{ V}$ for a logic 1 and 0.45V for a logic 0. Timing measurements are made at $V_{IH}$ min. for a logic 1 and $V_{IL}$ max. for a logic 0.

Float Waveforms

Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded $V_{OH}$/$V_{OL}$ level occurs.
## Ordering Information

<table>
<thead>
<tr>
<th>Speed (MHz)</th>
<th>Power Supply</th>
<th>Ordering Code</th>
<th>Package</th>
<th>Operation Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>5V ±20%</td>
<td>AT89C51-12AC</td>
<td>44A</td>
<td>Commercial (0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JC</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12AI</td>
<td>44A</td>
<td>Industrial (-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12JI</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-12QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>5V ±20%</td>
<td>AT89C51-16AC</td>
<td>44A</td>
<td>Commercial (0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JC</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16AI</td>
<td>44A</td>
<td>Industrial (-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16JI</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-16QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>5V ±20%</td>
<td>AT89C51-20AC</td>
<td>44A</td>
<td>Commercial (0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JC</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20AI</td>
<td>44A</td>
<td>Industrial (-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20JI</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-20QI</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>5V ±20%</td>
<td>AT89C51-24AC</td>
<td>44A</td>
<td>Commercial (0°C to 70°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JC</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PC</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QC</td>
<td>44Q</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24AI</td>
<td>44A</td>
<td>Industrial (-40°C to 85°C)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24JI</td>
<td>44J</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24PI</td>
<td>40P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>AT89C51-24QI</td>
<td>44Q</td>
<td></td>
</tr>
</tbody>
</table>

### Package Type

- **44A**: 44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
- **44J**: 44-lead, Plastic J-leaded Chip Carrier (PLCC)
- **40P6**: 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
- **44Q**: 44-lead, Plastic Gull Wing Quad Flatpack (PQFP)
**Packaging Information**

### 44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

Controlling dimension: millimeters

### 44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC

### 40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

### 44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB

Controlling dimension: millimeters
LAMPIRAN-B

FOTO ALAT
LAMPIRAN-C

PROGRAM
$MOD51
AJMP START
DELAY: MOV R1,#0FFH
DEL1: MOV R2,#0FFH
DEL: DEC R2
CJNE R2,#00H, DEL
DEC R1
CJNE R1,#00H, DEL1
RET
DELAY1: MOV R1,#80H
D1: MOV R2,#0FFH
D2: DEC R2
CJNE R2,#00H, D2
DEC R1
CJNE R1,#00H, D1
DEC R3
CJNE R3,#00H,DELAY1
RET
;SUB-RUTIN MENAIKAN JALUR TEMBAKAN
NAIK: MOV P1,#20H
CALL DELAY1
MOV P1,#00H
MOV R3,#20H
CALL DELAY1
RET
;SUB-RUTIN MENURUNKAN JALUR TEMBAKAN
TURUN: MOV P1,#02H
CALL DELAY1
MOV P1,#00H
MOV R3,#20H
CALL DELAY1
RET
;SUB-RUTIN MENARIK PEGAS
LEMPAR: MOV P1,#10000000B
CALL DELAY1
MOV P1,#00H
MOV R3,#20H
CALL DELAY1
CALL TARIK
RET
;SUB-RUTIN MENARIK MOTOR PENARIK PEGAS
TARIK: MOV P1,#00000100B
MOV R3,#0AH
CALL DELAY1
MOV P1,#00H
MOV R3,#20H
CALL DELAY1
RET
;SUB-RUTIN MELEPASKAN MOTOR PENARIK PEGAS
MOV P1,#00000100B
MOV R3,#0AH
CALL DELAY1
MOV P1,#00H
MOV R3,#20H
CALL DELAY1
RET
START:
MOV A,P3
CJNE A,#48H,DUA0 ; JARAK 20 CM
MOV P2,#20H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA0:
CJNE A,#47H,DUA01 ; JARAK 20 CM
MOV P2,#20H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA01:
CJNE A,#46H,DUA1 ; JARAK 20 CM
MOV P2,#20H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA1:
CJNE A,#45H,DUA11 ; JARAK 21 CM
MOV P2,#21H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA11:
CJNE A,#44H,DUA12 ; JARAK 21 CM
MOV P2,#21H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA12:
CJNE A,#43H,DUA13 ; JARAK 21 CM
MOV P2,#21H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA13:
CJNE A,#42H,DUA2 ; JARAK 21 CM
MOV P2,#21H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA2:
CJNE A,#41H,DUA21 ; JARAK 22 CM
MOV P2,#22H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA21:
CJNE A,#40H,DUA22 ; JARAK 22 CM
MOV P2,#22H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA22:
CJNE A,#3FH,DUA3 ; JARAK 22 CM
MOV P2,#22H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN
DUA3: CJNE A,#3EH,DUA31 ; JARAK 23 CM
MOV P2,#23H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA31: CJNE A,#3DH,DUA4 ; JARAK 23 CM
MOV P2,#23H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA4: CJNE A,#3CH,DUA41 ; JARAK 24 CM
MOV P2,#24H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA41: CJNE A,#3BH,DUA42 ; JARAK 24 CM
MOV P2,#24H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA42: CJNE A,#3AH,DUA43 ; JARAK 24 CM
MOV P2,#24H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA43: CJNE A,#39H,DUA44 ; JARAK 24 CM
MOV P2,#24H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA44: CJNE A,#38H,DUA5 ; JARAK 24 CM
MOV P2,#24H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA5: CJNE A,#37H,DUA51 ; JARAK 25 CM
MOV P2,#25H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA51: CJNE A,#36H,DUA6 ; JARAK 25 CM
MOV P2,#25H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

DUA6: CJNE A,#35H,DUA61 ; JARAK 26 CM
MOV P2,#26H
CALL DELAY
MOV R3,#0B0H
CALL NAIK
MOV R3,#05H
CALL LEMPAR
MOV R3,#0ACH
CALL TURUN
AJMP NN

C-3
DUA61: CJNE A,#34H,DUA7 ;JARAK 26 CM
    MOV P2,#26H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#05H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

DUA7: CJNE A,#33H,DUA8 ;JARAK 27 CM
    MOV P2,#27H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#05H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

DUA8: CJNE A,#32H,DUA81 ;JARAK 28 CM
    MOV P2,#28H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#06H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

DUA81: CJNE A,#31H,DUA9 ;JARAK 28 CM
    MOV P2,#28H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#06H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

DUA9: CJNE A,#30H,DUA91 ;JARAK 29 CM
    MOV P2,#29H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#06H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

DUA91: CJNE A,#2FH,TG0 ;JARAK 29 CM
    MOV P2,#29H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#06H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

TG0: CJNE A,#2EH,TG2 ;JARAK 30 CM
    MOV P2,#30H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#06H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

TG2: CJNE A,#2DH,TG3 ;JARAK 32 CM
    MOV P2,#32H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#06H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

TG3: CJNE A,#2CH,TG5 ;JARAK 33 CM
    MOV P2,#33H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#06H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

TG5: CJNE A,#2BH,TG6 ;JARAK 35 CM
    MOV P2,#35H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#07H
    CALL LEMPAR
    MOV R3,#05H
    CALL TURUN
    AJMP NN
TG6: CJNE A,#2AH,TG7 ;JARAK 36 CM
    MOV P2,#36H
    CALL DELAY
    MOV R3,#60H
    CALL NAIK
    MOV R3,#07H
    CALL LEMPAR
    MOV R3,#5CH
    CALL TURUN
    AJMP NN

E1: CJNE A,#25H,E3 ;JARAK 41 CM
    MOV P2,#41H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#08H
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

TG7: CJNE A,#29H,TG8 ;JARAK 37 CM
    MOV P2,#37H
    CALL DELAY
    MOV R3,#60H
    CALL NAIK
    MOV R3,#07H
    CALL LEMPAR
    MOV R3,#5CH
    CALL TURUN
    AJMP NN

E3: CJNE A,#24H,E4 ;JARAK 43 CM
    MOV P2,#43H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#08H
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

TG8: CJNE A,#28H,TG9 ;JARAK 38 CM
    MOV P2,#38H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#07H
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

E4: CJNE A,#23H,E5 ;JARAK 44 CM
    MOV P2,#44H
    CALL DELAY
    MOV R3,#0B0H
    MOV R3,#88H
    CALL NAIK
    MOV R3,#08H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

TG9: CJNE A,#27H,E0 ;JARAK 39 CM
    MOV P2,#39H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#07H
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

E5: CJNE A,#22H,E6 ;JARAK 45 CM
    MOV P2,#45H
    CALL DELAY
    MOV R3,#0B0H
    MOV R3,#09H
    CALL NAIK
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

E0: CJNE A,#26H,E1 ;JARAK 40 CM
    MOV P2,#40H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#08H
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

E6: CJNE A,#21H,E7 ;JARAK 46 CM
    MOV P2,#46H
    CALL DELAY
    MOV R3,#0B0H
    MOV R3,#09H
    CALL NAIK
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN
E7: CJNE A,#20H,E8  ; JARAK 47 CM
    MOV P2,#47H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#09H
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

E8: CJNE A,#1FH,L0  ; JARAK 48 CM
    MOV P2,#48H
    CALL DELAY
    MOV R3,#60H
    CALL NAIK
    MOV R3,#0AH
    CALL LEMPAR
    MOV R3,#5CH
    CALL TURUN
    AJMP NN

L0: CJNE A,#1EH,L5  ; JARAK 50 CM
    MOV P2,#50H
    CALL DELAY
    MOV R3,#60H
    CALL NAIK
    MOV R3,#0AH
    CALL LEMPAR
    MOV R3,#5CH
    CALL TURUN
    AJMP NN

L5: CJNE A,#1DH,EN0  ; JARAK 55 CM
    MOV P2,#55H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#0BH
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

EN0: CJNE A,#1CH,EN5  ; JARAK 60 CM
    MOV P2,#60H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#0CH
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

EN5: CJNE A,#1BH,TJ0  ; JARAK 65 CM
    MOV P2,#65H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#0DH
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

TJ0: CJNE A,#1AH,TJ5  ; JARAK 70 CM
    MOV P2,#70H
    CALL DELAY
    MOV R3,#88H
    CALL NAIK
    MOV R3,#0CH
    CALL LEMPAR
    MOV R3,#84H
    CALL TURUN
    AJMP NN

TJ5: CJNE A,#19H,LP  ; JARAK 75 CM
    MOV P2,#75H
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#0EH
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

LP:  MOV P2,#80H  ; JARAK 80 CM
    CALL DELAY
    MOV R3,#0B0H
    CALL NAIK
    MOV R3,#0EH
    CALL LEMPAR
    MOV R3,#0ACH
    CALL TURUN
    AJMP NN

NN: MOV P1,#00H
    MOV R3,#0FFH
    CALL DELAY1

END