LAMPIRAN A
--Listing Program PLC Controller--

Listing program *master controller*

$mod51

CALL INIT

LAGI:

    MOV A,P1

    MOV R5,A

    MOV P0,#11111110B

    JB P0.4,NO2

    MOV R0,#01H

NO2:

    JB P0.5,NO3

    MOV R0,#03H

NO3:

    JB P0.6,NOA

    MOV R0,#05H

NOA:

    JB P0.7,NO4

    MOV A,R5

    ANL A,#0FH

    ADD A,#0F0H

    MOV R4,A

    MOV A,R0

    RR A

    RR A

    RR A

    RR A

    ADD A,#0FH

    ANL A,R4

    MOV P2,A

    CALL KIRIM

    CALL DELAY

A - 2

```
        MOV A,R5
        ANL A,#0F0H
        RL A
        RL A
        RL A
        RL A
        ADD A,#0F0H
        MOV R4,A
        MOV A,R0
        INC A
        RR A
        RR A
        RR A
        RR A
        ADD A,#0FH
        ANL A,R4
        MOV P2,A
        CALL KIRIM
NO4:
        MOV P0,#11111101B
        JB P0.4,NO5
        MOV R0,#07H
NO5:
        JB P0.5,NO6
        MOV R0,#09H
NO6:
        JB P0.6,NOB
        MOV R0,#0BH
NOB:
        JB P0.7,NO7
NO7:
```

A - 3

```
        MOV P0,#11111011B
        JB P0.4,NO8
NO8:
        MOV R0,#0DH
        JB P0.5,NO9
NO9:
        MOV R0,#0FH
        JB P0.6,NOC
NOC:
        JB P0.7,NOSTARR
NOSTARR:
        MOV P0,#11110111B
        JB P0.4,NO0
        MOV R4,#0F0H
        MOV A,R0
        RR A
        RR A
        RR A
        RR A
        ADD A,#0FH
        ANL A,R4
        MOV P2,A
        CALL KIRIM
        CALL DELAY
        MOV R4,#0F0H
        MOV A,R0
        INC A
        RR A
        RR A
        RR A
        RR A
```

A - 4

```
        ADD A,#0FH
        ANL A,R4
        MOV P2,A
        CALL KIRIM
NO0:
        JB P0.5,NOKRESS
NOKRESS:
        JB P0.6,NOD
        MOV R4,#0FFH
        MOV A,R0
        RR A
        RR A
        RR A
        RR A
        ADD A,#0FH
        ANL A,R4
        MOV P2,A
        CALL KIRIM
        CALL DELAY
        MOV R4,#0FFH
        MOV A,R0
        INC A
        RR A
        RR A
        RR A
        RR A
        ADD A,#0FH
        ANL A,R4
        MOV P2,A
        CALL KIRIM
NOD:
```

```
        JB P0.7,NON
NON:
        LJMP LAGI
INIT:
        MOV P0,#00H
        MOV P1,#00H
        MOV P2,#00H
        MOV   SP, #30H
        MOV   SCON, #50H
;inisialisasi baud rate (9600 bps)
        MOV   TMOD, #20H
        MOV   TL1, #0FDH
        MOV   TH1, #0FDH
        MOV   PCON, #00H
        SETB   TR1
        RET
KIRIM:
        CLR TI
        MOV SBUF,A
        JNB TI,$
        RET
DELAY:
DLY0:
        MOV R6,#0FFH
DLY1:
     DJNZ R6,DLY1
        RET
END
```

Listing program *slave controler*

SLAVE A

$mod51

```
        MOV   R0,#00H
        MOV   R1,#00H
        MOV   R2,#00H
        MOV   R3,#00H
        MOV   R4,#00H
        MOV   R5,#00H
        MOV   R6,#00H
        MOV   R7,#00H
        MOV   P0,00H
        MOV   P1,00H
        MOV   P2,00H
        LJMP  START
TERIMA:
        JNB   RI,$
        MOV   A,SBUF
        MOV   R1,A
        CLR   RI
        MOV A,#11110000B
        ANL A,R1
        MOV R2,A
        MOV A,#00001111B
        ANL A,R1
        MOV R3,A
        RR  A
        RR  A
        RR  A
        RR  A
        MOV R4,A
```

```
        RETI
START:      MOV   SP, #30H
            MOV   SCON, #50H
;inisialisasi baud rate (9600 bps)
      MOV   TMOD, #20H
      MOV   TL1, #0FDH
      MOV   TH1, #0FDH
      MOV   PCON, #00H
      SETB   TR1
ULANG:
      CALL TERIMA
      CJNE R2,#10H,ADDB
      MOV A,R3
      ORL A,#0F0H
      MOV R5,A
      MOV A,P0
      ANL A,R5
      ORL A,R3
      MOV P0,A
ADDB:
      CJNE R2,#20H,ADDCO
      MOV A,R4
      ORL A,#0FH
      MOV R5,A
      MOV A,P0
      ANL A,R5
      ORL A,R4
      MOV P0,A
ADDCO:
      CJNE R2,#30H,ADDD
      MOV A,R3
```

A - 8

```
        ORL A,#0F0H
        MOV R5,A
        MOV A,P1
        ANL A,R5
        ORL A,R3
        MOV P1,A
ADDD:
        CJNE R2,#40H,ADDE
        MOV A,R4
        ORL A,#0FH
        MOV R5,A
        MOV A,P1
        ANL A,R5
        ORL A,R4
        MOV P1,A
ADDE:
        CJNE R2,#50H,ADDF
        MOV A,R3
        ORL A,#0F0H
        MOV R5,A
        MOV A,P2
        ANL A,R5
        ORL A,R3
        MOV P2,A
ADDF:
        CJNE R2,#60H,ADDG
        MOV A,R4
        ORL A,#0FH
        MOV R5,A
        MOV A,P2
        ANL A,R5
```

A - 9

```
        ORL A,R4
        MOV P2,A
ADDG:
        LJMP ULANG:
DELAY:
        MOV R0,#0FH
DLY1:
        MOV R1,#0FFH
DLY0:
        DJNZ R1,DLY0
        DJNZ R0,DLY1
END
```
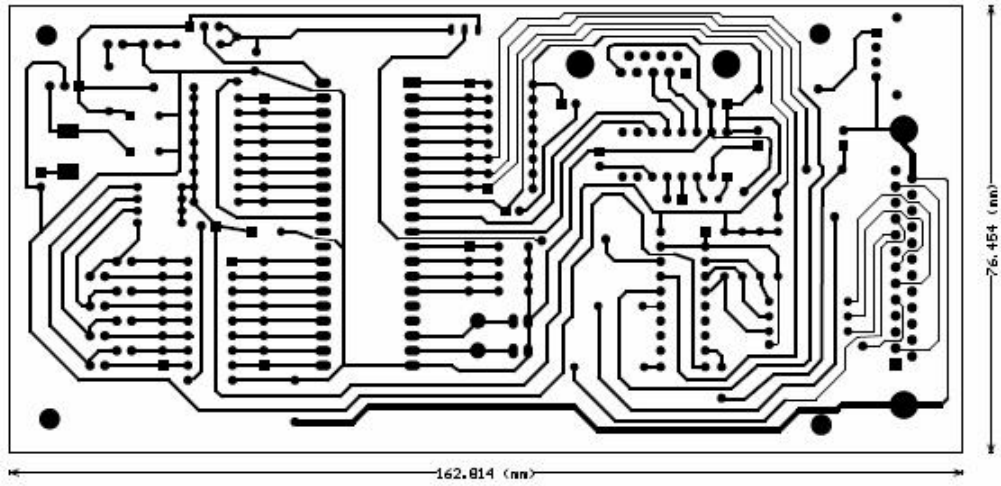
SLAVE B

$mod51

```
        MOV   R0,#00H
        MOV   R1,#00H
        MOV   R2,#00H
        MOV   R3,#00H
        MOV   R4,#00H
        MOV   R5,#00H
        MOV   R6,#00H
        MOV   R7,#00H
        MOV   P0,00H
        MOV   P1,00H
        MOV   P2,00H
        LJMP  START
TERIMA:
        JNB   RI,$
        MOV   A,SBUF
        MOV   R1,A
        CLR   RI
        MOV A,#11110000B
        ANL A,R1
        MOV R2,A
        MOV A,#00001111B
        ANL A,R1
        MOV R3,A
        RR  A
        RR  A
        RR  A
        RR  A
        MOV R4,A
        RETI
```

```
START:          MOV   SP, #30H
                MOV   SCON, #50H
;inisialisasi baud rate (9600 bps)
        MOV   TMOD, #20H
        MOV   TL1, #0FDH
        MOV   TH1, #0FDH
        MOV   PCON, #00H
        SETB  TR1
ULANG:
        CALL TERIMA
        CJNE R2,#70H,ADDB
        MOV A,R3
        ORL A,#0F0H
        MOV R5,A
        MOV A,P0
        ANL A,R5
        ORL A,R3
        MOV P0,A
ADDB:
        CJNE R2,#80H,ADDCO
        MOV A,R4
        ORL A,#0FH
        MOV R5,A
        MOV A,P0
        ANL A,R5
        ORL A,R4
        MOV P0,A
ADDCO:
        CJNE R2,#90H,ADDD
        MOV A,R3
        ORL A,#0F0H
```

```
        MOV R5,A
        MOV A,P1
        ANL A,R5
        ORL A,R3
        MOV P1,A
ADDD:
        CJNE R2,#A0H,ADDE
        MOV A,R4
        ORL A,#0FH
        MOV R5,A
        MOV A,P1
        ANL A,R5
        ORL A,R4
        MOV P1,A
ADDE:
        CJNE R2,#B0H,ADDF
        MOV A,R3
        ORL A,#0F0H
        MOV R5,A
        MOV A,P2
        ANL A,R5
        ORL A,R3
        MOV P2,A
ADDF:
        CJNE R2,#C0H,ADDG
        MOV A,R4
        ORL A,#0FH
        MOV R5,A
        MOV A,P2
        ANL A,R5
        ORL A,R4
```

A -13

```
        MOV P2,A
ADDG:
        LJMP ULANG:
DELAY:
        MOV R0,#0FH
DLY1:
        MOV R1,#0FFH
DLY0:
        DJNZ R1,DLY0
        DJNZ R0,DLY1
END
```

LAMPIRAN B
--Rangkaian Dan PCB--

Skema Keseluruhan Sistem PLC
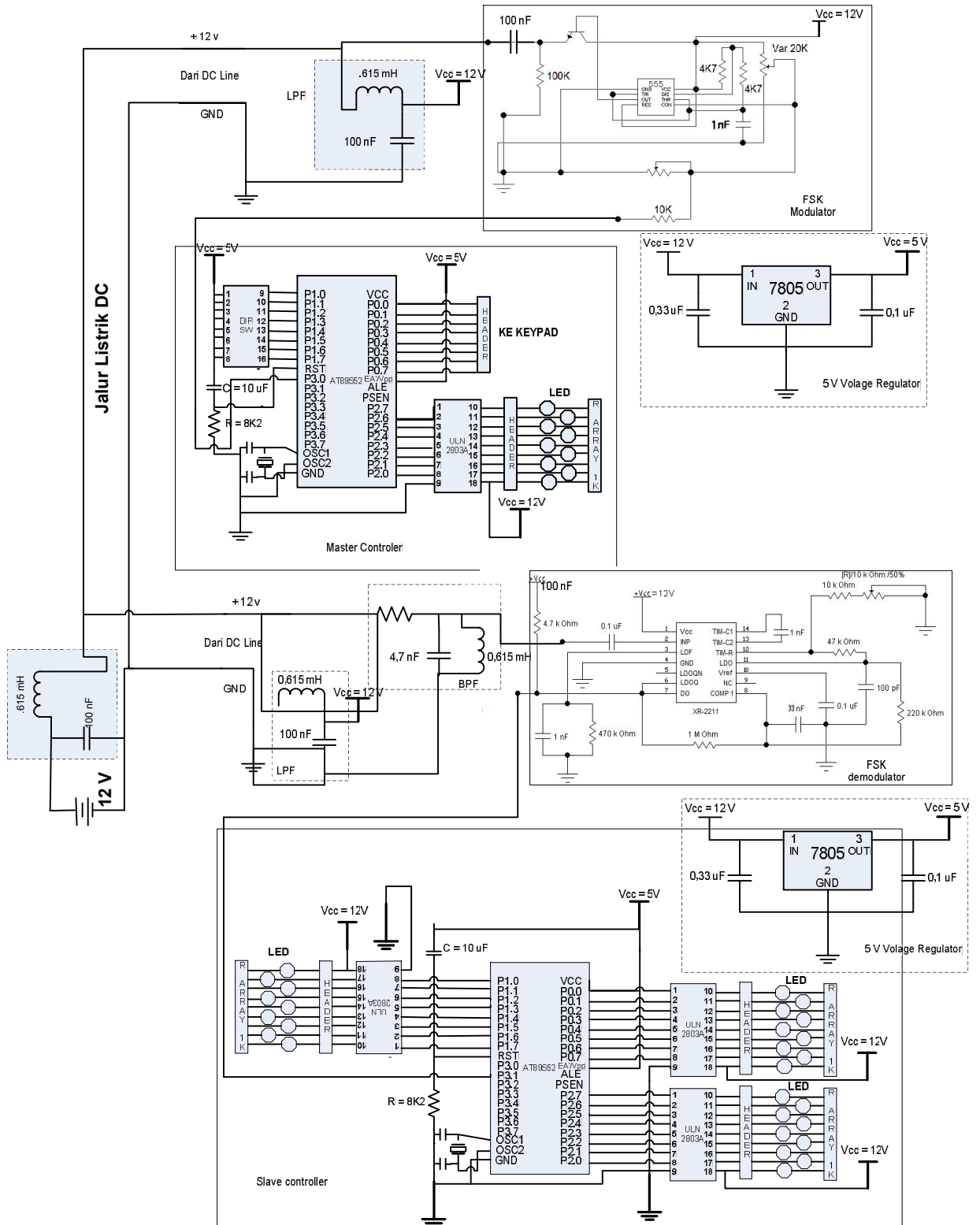
PCB MASTER CONTROLLER

PCB Bottom
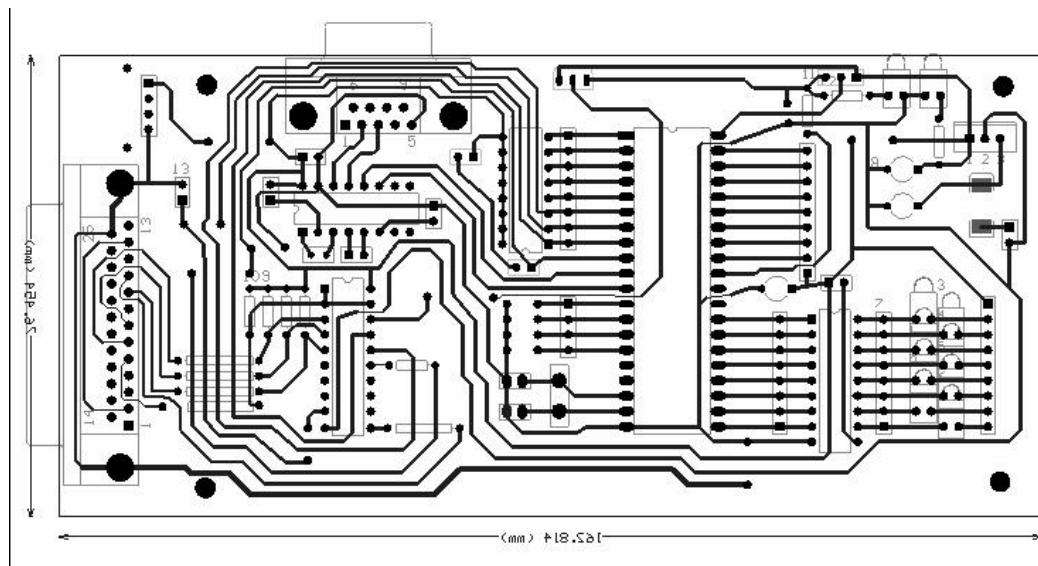
PCB Layout

PCB SLAVE CONTROLLER

PCB Bottom
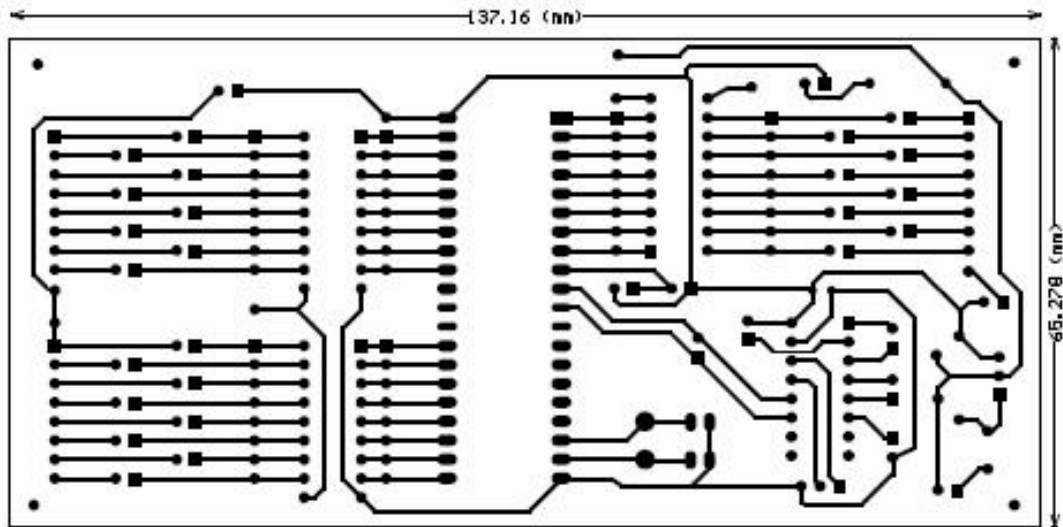
PCB Layout
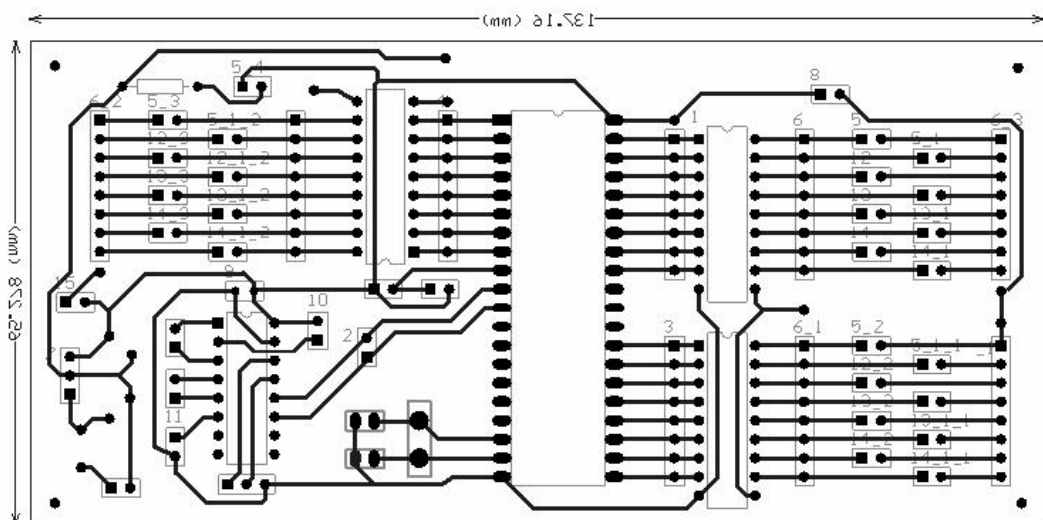
PCB FSK MODULATOR

PCB FSK DEMODULATOR

A -19

EXAR

...the analog plus company^{TM}
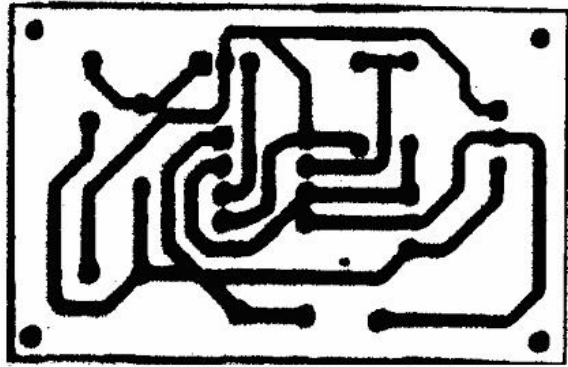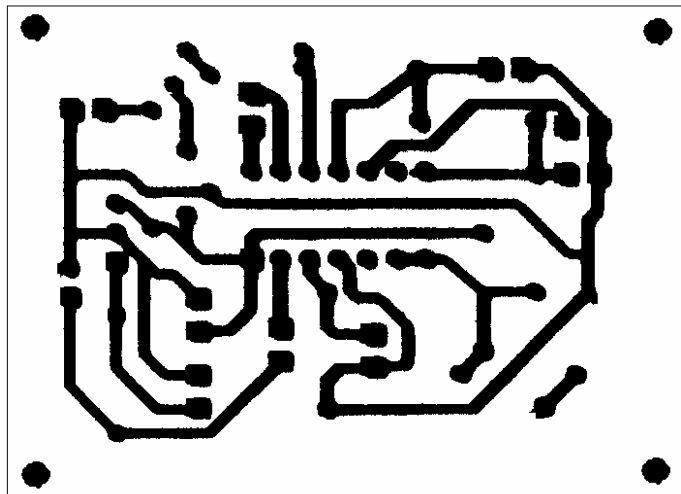
FEATURES

- Wide Frequency Range, 0.01Hz to 300kHz
- Wide Supply Voltage Range, 4.5V to 20V
- HCMOS/TTL/Logic Compatibility
- FSK Demodulation, with Carrier Detection
- Wide Dynamic Range, 10mV to 3V rms
- Adjustable Tracking Range, $\pm$1% to 80%
- Excellent Temp. Stability, $\pm$50ppm/$^{\circ}$C, max.

APPLICATIONS

- Caller Identification Delivery
- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications applications. It is particularly suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 10mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a

quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply is provided at an output pin.

The XR-2211 is available in 14 pin packages specified for military and industrial temperature ranges.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2211M	14 Pin CDIP (0.300")	-55°C to +125°C
XR-2211N	14 Pin CDIP (0.300")	-40°C to +85°C
XR-2211P	14 Pin PDIP (0.300")	-40°C to +85°C
XR-2211ID	14 Lead SOIC (Jedec, 0.150")	-40°C to +85°C

Rev. 3.01

©1992
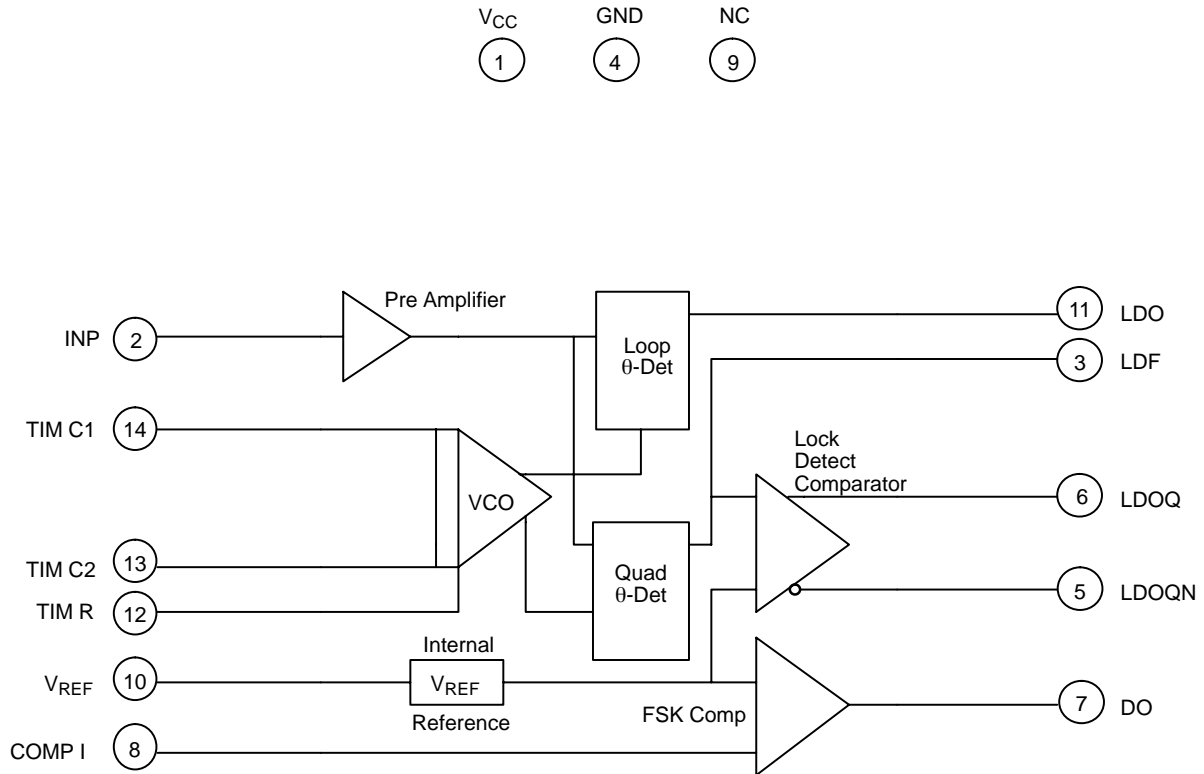
BLOCK DIAGRAM

Figure 1. XR-2211 Block Diagram

EXAR

PIN CONFIGURATION

V_CC	1	•	14	TIM C1
INP	2		13	TIM C2
LDF	3		12	TIM R
GND	4		11	LDO
LDOQN	5		10	V_REF
LDOQ	6		9	NC
DO	7		8	COMP I

14 Lead CDIP, PDIP (0.300")

V_CC	1	14	TIM C1
INP	2	13	TIM C2
LDF	3	12	TIM R
GND	4	11	LDO
LDOQN	5	10	V_REF
LDOQ	6	9	NC
DO	7	8	COMP I
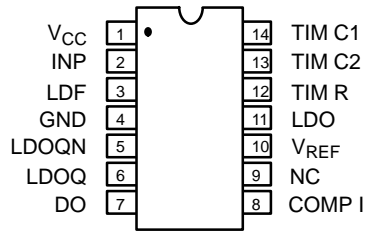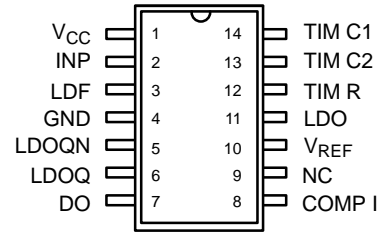
14 Lead SOIC (Jedec, 0.150")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	V_{CC}		**Positive Power Supply.**
2	INP	I	**Receive Analog Input.**
3	LDF	O	**Lock Detect Filter.**
4	GND		**Ground Pin.**
5	LDOQN	O	**Lock Detect Output Not.** This output will be low if the VCO is in the capture range.
6	LDOQ	O	**Lock Detect Output.** This output will be high if the VCO is in the capture range.
7	DO	O	**Data Output.** Decoded FSK output.
8	COMP I	I	**FSK Comparator Input.**
9	NC		**Not Connected.**
10	V_{REF}	O	**Internal Voltage Reference.** The value of V_{REF} is $V_{CC}/2$ - 650mV.
11	LDO	O	**Loop Detect Output.** This output provides the result of the quadrature phase detection.
12	TIM R	I	**Timing Resistor Input.** This pin connects to the timing resistor of the VCO.
13	TIM C2	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 14.
14	TIM C1	I	**Timing Capacitor Input.** The timing capacitor connects between this pin and pin 13.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 12V, T_A = +25°C, R_O = 30KΩ, C_O = 0.033μF, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
General					
Supply Voltage	**4.5**		**20**	V	
Supply Current		4	**7**	mA	$R_0 \geq$ 10KΩ. See *Figure 4.*
Oscillator Section					
Frequency Accuracy		±1	**±3**	%	Deviation from f_O = $1/R_0 C_0$
Frequency Stability					
Temperature		±20	±50	ppm/°C	See *Figure 8.*
Power Supply		0.05	**0.5**	%/V	V_{CC} = 12 ±1V. See *Figure 7.*
		0.2		%/V	V_{CC} = ± 5V. See *Figure 7.*
Upper Frequency Limit	**100**	300		kHz	R_0 = 8.2KΩ, C_0 = 400pF
Lowest Practical Operating Frequency			0.01	Hz	R_0 = 2MΩ, C_0 = 50μF
Timing Resistor, R_0 - See *Figure 5*					
Operating Range	**5**		2000	KΩ	
Recommended Range	5			KΩ	See *Figure 7* and *Figure 8.*
Loop Phase Dectector Section					
Peak Output Current	**±150**	±200	**±300**	μA	Measured at Pin 11
Output Offset Current		1		μA	
Output Impedance		1		MΩ	
Maximum Swing	**±4**	± 5		V	Referenced to Pin 10
Quadrature Phase Detector				Measured at Pin 3	
Peak Output Current	**100**	300		μA	
Output Impedance		1		MΩ	
Maximum Swing		11		V_{PP}	
Input Preampt Section				Measured at Pin 2	
Input Impedance		20		KΩ	
Input Signal					
Voltage Required to Cause Limiting		2	10	mV rms	

Notes
Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.
Bold face parameters *are covered by production test and guaranteed over operating temperature range.*

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $V_{CC} = 12V$, $T_A = +25°C$, $R_O = 30K\Omega$, $C_O = 0.033\mu F$, unless otherwise specified.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Voltage Comparator Section					
Input Impedance		2		MΩ	Measured at Pins 3 and 8
Input Bias Current		100		nA	
Voltage Gain	55	70		dB	$R_L = 5.1K\Omega$
Output Voltage Low		300	**500**	mV	$I_C = 3mA$
Output Leakage Current		0.01	**10**	μA	$V_O = 20V$
Internal Reference					
Voltage Level	**4.9**	5.3	**5.7**	V	Measured at Pin 10
Output Impedance		100		Ω	AC Small Signal
Maximum Source Current		80		μA	

Notes
Parameters are guaranteed over the recommended operating conditions, but are not 100% tested in production.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 20V
Input Signal Level . . . . 3V rms
Power Dissipation 900mW

Package Power Dissipation Ratings
CDIP 750mW
   Derate Above $T_A = 25°C$ . . . . 8mW/°C
PDIP 800mW
   Derate Above $T_A = 25°C$ . . . . 60mW/°C
SOIC 390mW
   Derate Above $T_A = 25°C$ . . . . 5mW/°C

SYSTEM DESCRIPTION

The main PLL within the XR-2211 is constructed from an input preamplifier, analog multiplier used as a phase detector and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that input signals above typically 10mV rms are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (unfiltered) produces sum and difference frequencies of the input and the VCO output. The VCO is actually a current controlled oscillator with its normal input current (f_O) set by a resistor (R_0) to ground and its driving current with a resistor (R_1) from the phase detector.

The output of the phase detector produces sum and difference of the input and the VCO frequencies (internally connected). When in lock, these frequencies are $f_{IN}+ f_{VCO}$ (2 times f_{IN} when in lock) and $f_{IN} - f_{VCO}$ (0Hz when lock). By adding a capacitor to the phase detector output, the 2 times f_{IN} component is reduced, leaving a DC voltage that represents the phase difference between the two frequencies. This closes the loop and allows the VCO to track the input frequency.

The FSK comparator is used to determine if the VCO is driven above or below the center frequency (FSK comparator). This will produce both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is AC coupled to this terminal. The internal impedance at pin 2 is 20KΩ. Recommended input signal level is in the range of 10mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see *Figure 3*) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, pin 3 can be left open.

Lock Detect Output, Q (Pin 6): The output at pin 6 is at "low" state when the PLL is out of lock and goes to "high" state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V_{CC} for proper operation. At "low" state, it can sink up to 5mA of load current.

Lock Detect Complement, (Pin 5): The output at pin 5 is the logic complement of the lock detect output at pin 6. This output is also an open collector type stage which can sink 5mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V_{CC} for proper operation. It can sink 5mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (pin 11). This data filter is formed by R_F and C_F (see *Figure 3*.) The threshold voltage of the comparator is set by the internal reference voltage, V_{REF}, available at pin 10.

Reference Voltage, V_{REF} (Pin 10): This pin is internally biased at the reference voltage level, V_{REF}: $V_{REF} = V_{CC}/2$ - 650mV. The DC voltage level at this pin forms an internal reference for the voltage levels at pins 5, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to pin 11 (see *Figure 3*.) With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_{REF}. The peak to peak voltage swing available at the phase detector output is equal to 2 x V_{REF}.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_O, is:

$$f_O = \frac{1}{R_0 \cdot C_0} \ Hz$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10KΩ to 100KΩ (see *Figure 9*.)

This terminal is a low impedance point, and is internally biased at a DC level equal to V_{REF}. The maximum timing current drawn from pin 12 must be limited to $\leq$ 3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see *Figure 6*.) C_0 must be non-polar, and in the range of 200pF to 10μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at pin 12 (see *Figure 10*.)

VCO Free-Running Frequency, f_O: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. For set-up or adjustment purposes, the VCO free-running frequency can be tuned by using the generalized circuit in *Figure 3*, and applying an alternating bit pattern of O's and 1's at the known mark and space frequencies. By adjusting R_0, the VCO can then be tuned to obtain a 50% duty cycle on the FSK output (pin 7). This will ensure that the VCO f_O value is accurately referenced to the mark and space frequencies.
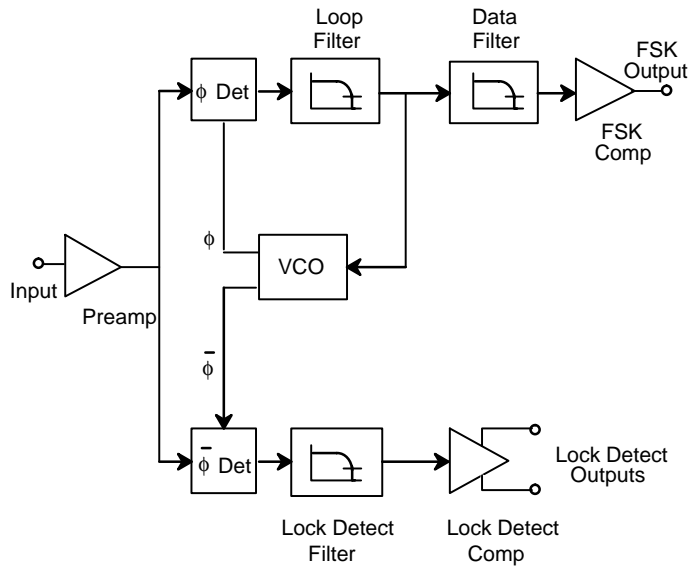
EXAR

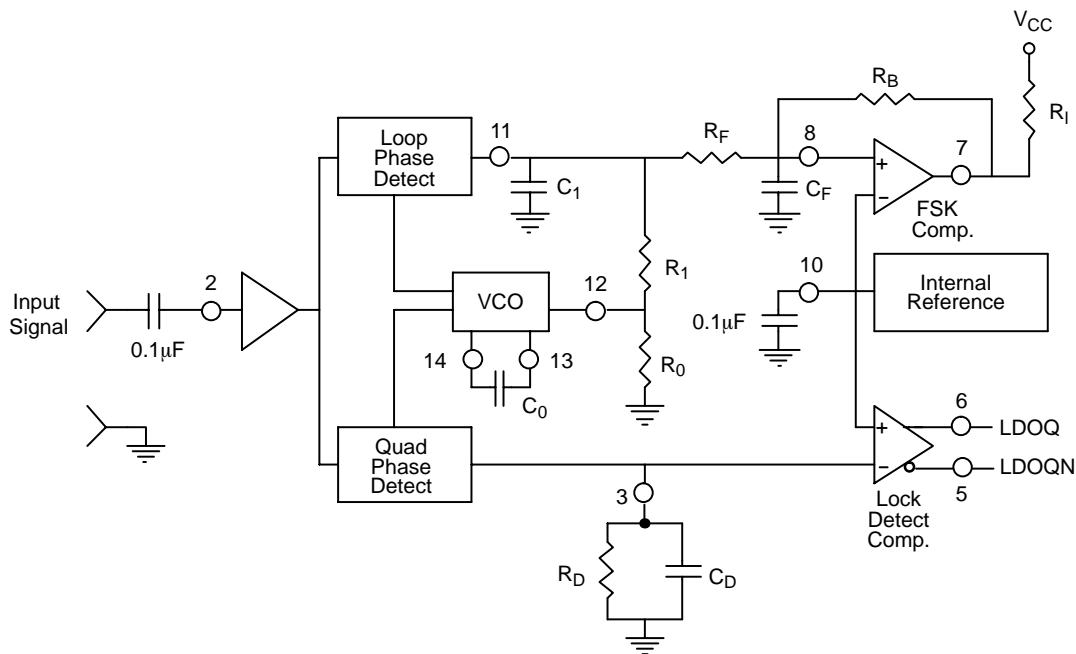**Figure 2. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211**

Figure 3. Generalized Circuit Connection for FSK and Tone Detection

DESIGN EQUATIONS

(All resistance in Ω, all frequency in Hz and all capacitance in farads, unless otherwise specified)

(See *Figure 3* for definition of components)

1. VCO Center Frequency, f_O:

$$f_O = \frac{1}{R_0 \cdot C_0}$$

2. Internal Reference Voltage, V_{REF} (measured at pin 10):

$$V_{REF} = \left(\frac{V_{CC}}{2}\right) - 650mV \ \text{in volts}$$

3. Loop Low-Pass Filter Time Constant, τ:

$$\tau = C_1 \cdot R_{PP} \ (\text{seconds})$$

where:

$$R_{PP} = \left(\frac{R_1 \cdot R_F}{R_1 + R_F}\right)$$

if R_F is ∞ or C_F reactance is ∞, then $R_{PP} = R1$

4. Loop Damping, ς:

$$\zeta = \sqrt{\left(\frac{1250 \cdot C_0}{R_1 \cdot C_1}\right)}$$

Note: *For derivation/explanation of this equation, please see TAN-011.*

5. Loop-tracking

bandwidth, $\pm = \dfrac{\varDelta f}{f_0}$

$\dfrac{\varDelta f}{f_0} = \dfrac{R_0}{R_1}$
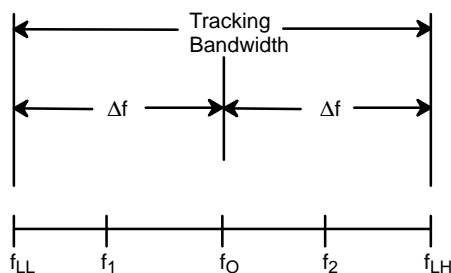
6. FSK Data filter time constant, tF:

$$\tau_F = \frac{R_B \cdot R_F}{(R_B + R_F)} \cdot C_F \ (seconds)$$

7. Loop phase detector conversion gain, Kd: (Kd is the differential DC voltage across pin 10 and pin11, per unit of phase error at phase detector input):

$$K_d = \frac{V_{REF} \cdot R_1}{10,000 \cdot \pi} \left[\frac{volt}{radian} \right]$$

Note: *For derivation/explanation of this equation, please see TAN-011.*

8. VCO conversion gain, Ko: (Ko is the amount of change in VCO frequency, per unit of DC voltage change at pin 11):

$$K_0 = \frac{-2\pi}{V_{REF} \cdot C_0 \cdot R_1} = \left(\frac{radian/second}{volt} \right)$$

9. The filter transfer function:

$$F(s) = \frac{1}{1 + SR_1 \cdot C_1} \ at \ 0 \ Hz. \qquad S = J\omega \ and \ \omega = 0$$

10. Total loop gain. K$_T$:

$$K_T = K_O \cdot K_d \cdot F(s) = \left(\frac{R_F}{5,000 \cdot C_0 \cdot (R_1 + R_F)} \right) \left[\frac{1}{seconds} \right]$$

11. Peak detector current I$_A$:

$$I_A = \frac{V_{REF}}{20,000} \ (V_{REF} \ in \ volts \ and \ I_A \ in \ amps)$$

Note: *For derivation/explanation of this equation, please see TAN-011.*

APPLICATIONS INFORMATION

FSK Decoding

Figure 10 shows the basic circuit connection for FSK decoding. With reference to *Figure 3* and *Figure 10*, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B from pin 7 to pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Design Instructions:

The circuit of *Figure 10* can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_O and f_1, these parameters can be calculated as follows:

(All resistance in Ω's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

a) Calculate PLL center frequency, f_O:

$$f_O = \sqrt{F_1 \cdot F_2}$$

b) Choose value of timing resistor R_0, to be in the range of 10KΩ to 100KΩ. This choice is arbitrary. The recommended value is $R_0 = 20$KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

$$R_O = R_O + \frac{R_X}{2}$$

c) Calculate value of C0 from design equation (1) or from *Figure 7*:

$$C_O = \frac{1}{R_0 \cdot f_0}$$

d) Calculate R1 to give the desired tracking bandwidth (See design equation 5).

$$R_1 = \frac{R_0 \cdot f_0}{(f_1 - f_2)} \cdot 2$$

e) Calculate C1 to set loop damping. (See design equation 4):

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \varsigma^2}$$

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f) The input to the XR-2211 may sometimes be too sensitive to noise conditions on the input line. *Figure 4* illustrates a method of de-sensitizing the XR-2211 from such noisy line conditions by the use of a resistor, Rx, connected from pin 2 to ground. The value of Rx is chosen by the equation and the desired minimum signal threshold level.

$$V_{IN} \ minimum \ (peak) = \ V_a\!-\!V_b = \varDelta V \pm 2.8mV \ offset = \ V_{REF}\frac{20,000}{(20,000 + R_x)} \ or \ R_x = 20,000\left(\frac{V_{REF}}{\varDelta V}\!-\!1\right)$$

V_{IN} minimum (peak) input voltage must exceed this value to be detected (equivalent to adjusting V threshold)
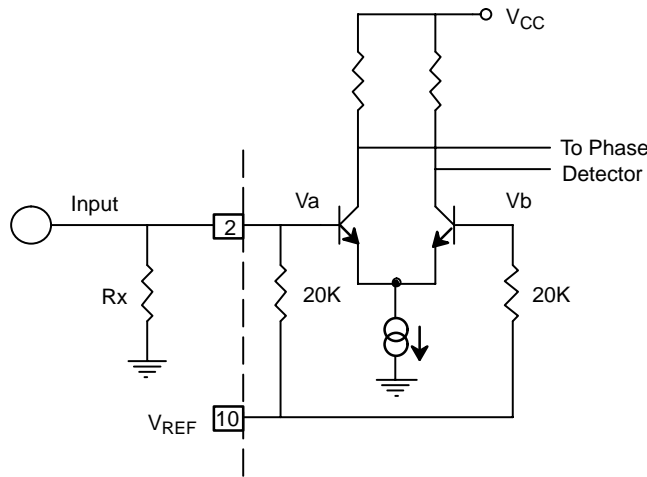
Figure 4. Desensitizing Input Stage

g) Calculate Data Filter Capacitance, C_F:

$$R_{sum} = \frac{(R_F + R_1)\cdot R_B}{(R_1 + R_F + R_B)}$$

$$C_F = \frac{0.25}{(R_{sum}\cdot Baud \ Rate)} \qquad Baud \ rate \ in \ \frac{1}{seconds}$$

Note: *All values except R_0 can be rounded to nearest standard value.*
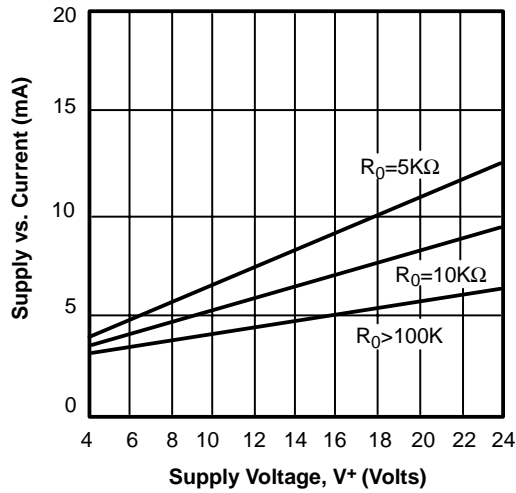
Figure 5. Typical Supply Current vs. V+ (Logic Outputs Open Circuited)
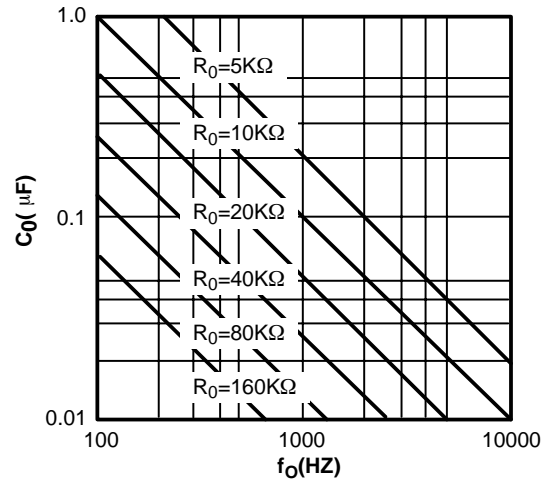
Figure 6. VCO Frequency vs. Timing Resistor
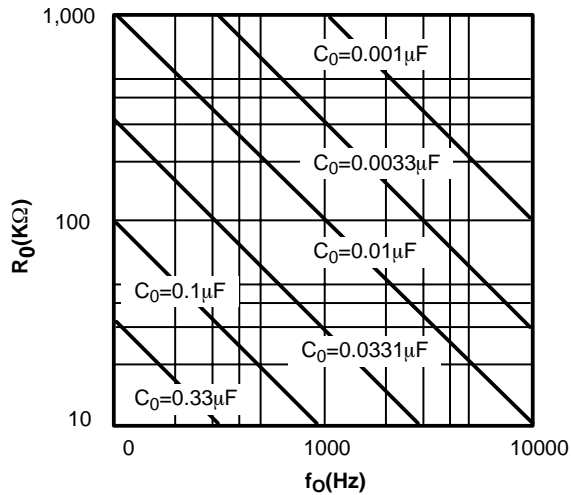
Figure 7. VCO Frequency vs. Timing Capacitor
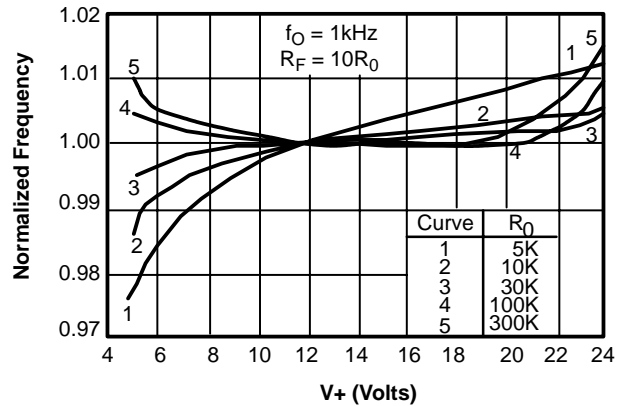
Figure 8. Typical f_O vs. Power Supply Characteristics
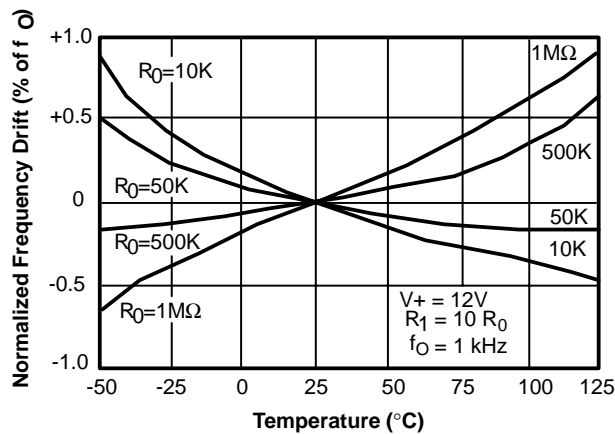
Figure 9. Typical Center Frequency Drift vs. Temperature

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Design Example:

1200 Baud FSK demodulator with mark and space frequencies of 1200/2200.

Step 1: Calculate f_O: from design instructions

(*a*) $f_O = \sqrt{1200 \cdot 2200} = 1624$

Step 2: Calculate R_0 : $R_0 = 10K$ with a potentiometer of 10K. (See design instructions (b))

(*b*) $R_T = 10 + \left(\dfrac{10}{2}\right) = 15K$

Step 3: Calculate C_0 from design instructions

(*c*) $C_O = \dfrac{1}{15000 \cdot 1624} = 39nF$

Step 4: Calculate R_1 : from design instructions

(*d*) $R_1 = \dfrac{20000 \cdot 1624 \cdot 2}{(2200 - 1200)} = 51,000$

Step 5: Calculate C_1 : from design instructions

(*e*) $C_1 = \dfrac{1250 \cdot 39nF}{51000 \cdot 0.5^2} = 3.9nF$

Step 6: Calculate R_F : R_F should be at least five times R_1, $R_F = 51,000 \cdot 5 = 255$ KΩ

Step 7: Calculate R_B : R_B should be at least five times R_F, $R_B = 255,000 \cdot 5 = 1.2$ MΩ

Step 8: Calculate R_{SUM} :

$$R_{SUM} = \frac{(R_F + R_1) \cdot R_B}{(R_F + R_1 + R_B)} = 240K\Omega$$

Step 9: Calculate C_F :

$$C_F = \frac{0.25}{(R_{SUM} \cdot Baud\ Rate)} = 1nF$$

Note: *All values except R_0 can be rounded to nearest standard value.*
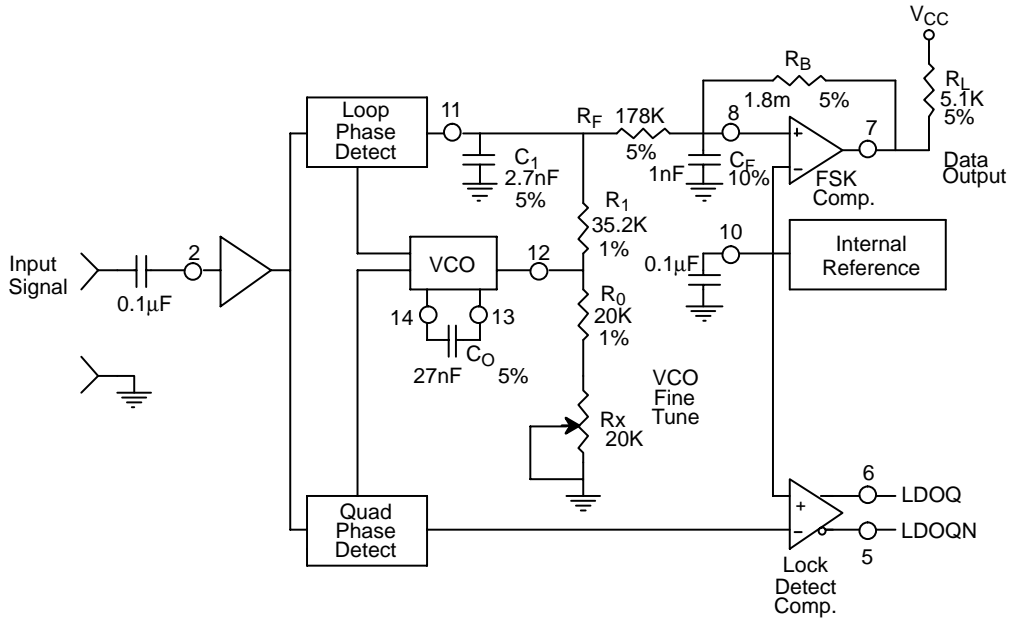
Figure 10. Circuit Connection for FSK Decoding of Caller Identification Signals (Bell 202 Format)
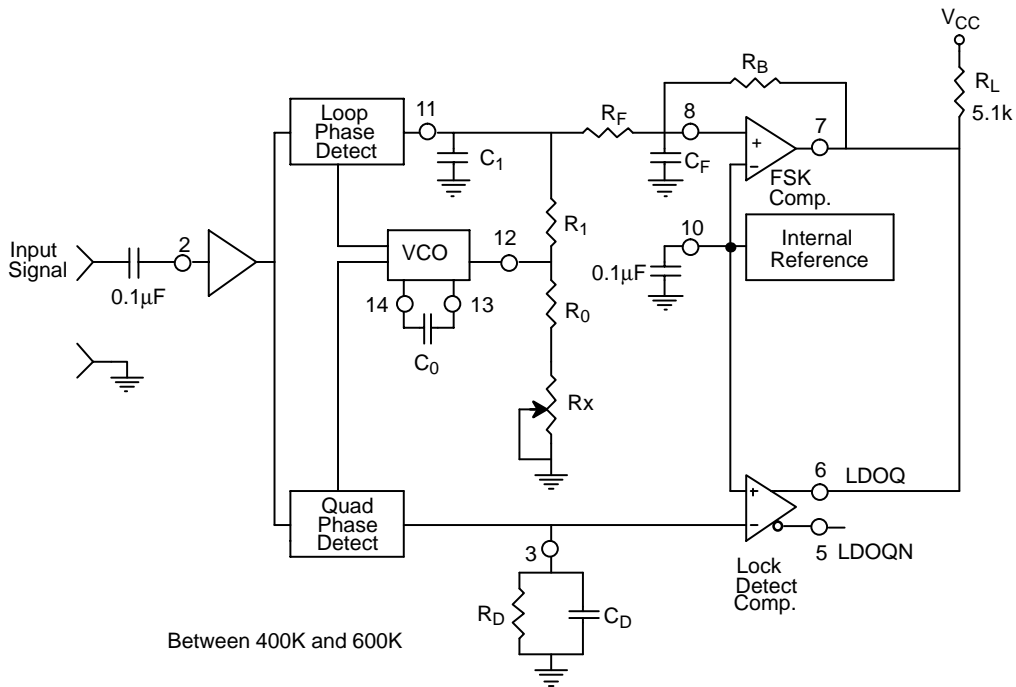
Figure 11. External Connectors for FSK Demodulation with Carrier Detect Capability

EXAR
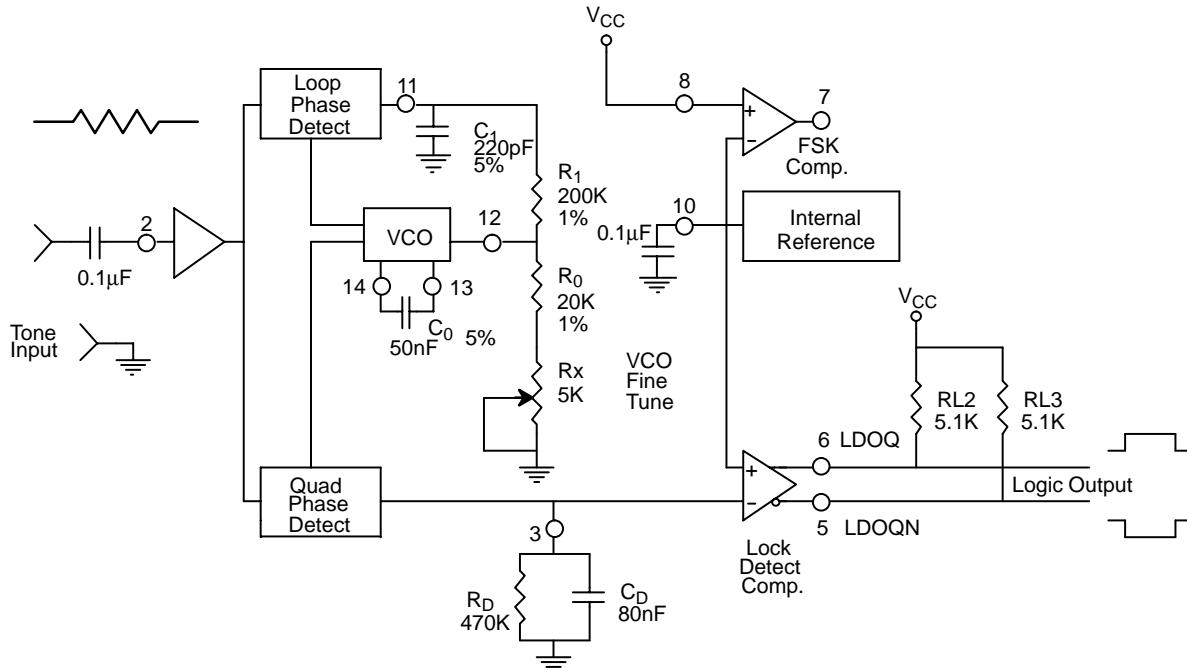
Figure 12. Circuit Connection for Tone Detection

FSK Decoding with Carrier Detect

The lock detect section of XR-2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in *Figure 11.* The open collector lock detect output, pin 6, is shorted to data output (pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL and the pin 6 output goes "high" to enable the data output.

Note: *Data Output is "Low" When No Carrier is Present.*

The minimum value of the lock detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta fc$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta fc > \Delta f/2$. For $R_D = 470K\Omega$, the approximate minimum value of C_D can be determined by:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F \text{ and } f \text{ in Hz.}$$

C in μF and f in Hz.

With values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output. For Caller I.D. applications choose $C_D = 0.1\mu F$.

Tone Detection

Figure 12 shows the generalized circuit connection for tone detection. The logic outputs, LDOQN and LDOQ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both outputs at pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L2} and R_{L3}, as shown in *Figure 12.*

With reference to *Figure 3* and *Figure 12*, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor.

Design Instructions:

The circuit of *Figure 12* can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

(All resistance in Ω's, all frequency in Hz and all capacitance in farads, unless otherwise specified)

a) Choose value of timing resistor R_0 to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is $R_0 = 20$KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

b) Calculate value of C_0 from design equation (1) or from *Figure 7* $f_S = f_O$:

$$C_O = \frac{1}{R_0 \cdot fs}$$

c) Calculate R_1 to set the bandwidth $\pm\Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_0 \cdot 2}{\Delta f}$$

Note: *The total detection bandwidth covers the frequency range of $f_O \pm \Delta f$*

d) Calculate value of C_1 for a given loop damping factor:

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \varsigma^2}$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of the filter capacitor C_D. To avoid chatter at the logic output, with $R_D = 470$KΩ, C_D must be:

$$C_D > \frac{16}{\Delta f} \quad C \text{ in } \mu F$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of $\pm$ 100Hz:

a) Choose value of timing resistor R_0 to be in the range of 10KΩ to 50KΩ. This choice is dictated by the max./min. current that the internal voltage reference can deliver. The recommended value is $R_0 = 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

b) Calculate value of C_0 from design equation (1) or from *Figure 6* $f_S = f_O$:

$$C_0 = \frac{1}{R_0 \cdot f_S} = \frac{1}{20,000 \cdot 1,000} = 50nF$$

EXAR

c) Calculate R_1 to set the bandwidth $\pm\Delta f$ (See design equation 5):

$$R_1 = \frac{R_0 \cdot f_O \cdot 2}{\Delta f} = \frac{20,000 \cdot 1,000 \cdot 2}{100} = 400K$$

Note: *The total detection bandwidth covers the frequency range of $f_O \pm\Delta f$*

d) Calculate value of C_0 for a given loop damping factor:

Normally, $\varsigma = 0.5$ is recommended.

$$C_1 = \frac{1250 \cdot C_0}{R_1 \cdot \varsigma^2} = \frac{1250 \cdot 50 \cdot 10^{-9}}{400,000 \cdot 0.5^2} = 6.25pF$$

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of the filter capacitor C_D . To avoid chatter at the logic output, with $R_D = 470K\Omega$, C_D must be:

$$C_D = \frac{16}{\Delta f} \geq \frac{16}{200} \geq 80nF$$

Increasing C_D slows down the logic output response time.

f) Fine tune center frequency with 5KΩ potentiometer, R_X.
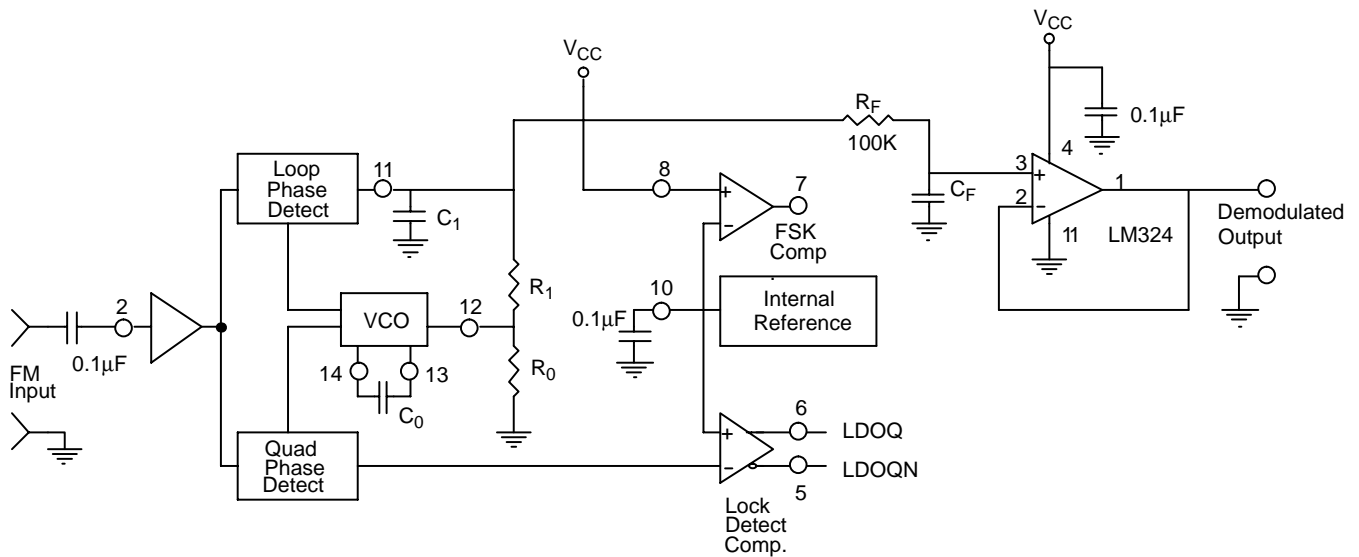
Figure 13. Linear FM Detector Using XR-2211 and an External Op Amp.
(See Section on Design Equation for Component Values.)

TOM™

Linear FM Detection

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in *Figure 13.* The demodulated output is taken from the loop phase detector output (pin 11), through a post-detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in *Figure 13.*

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{OUT} = \frac{R_1 \cdot V_{REF}}{100 \cdot R_0}$$

where VR is the internal reference voltage ($V_{REF} = V_{CC}/2 - 650mV$). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see the section on design equations.
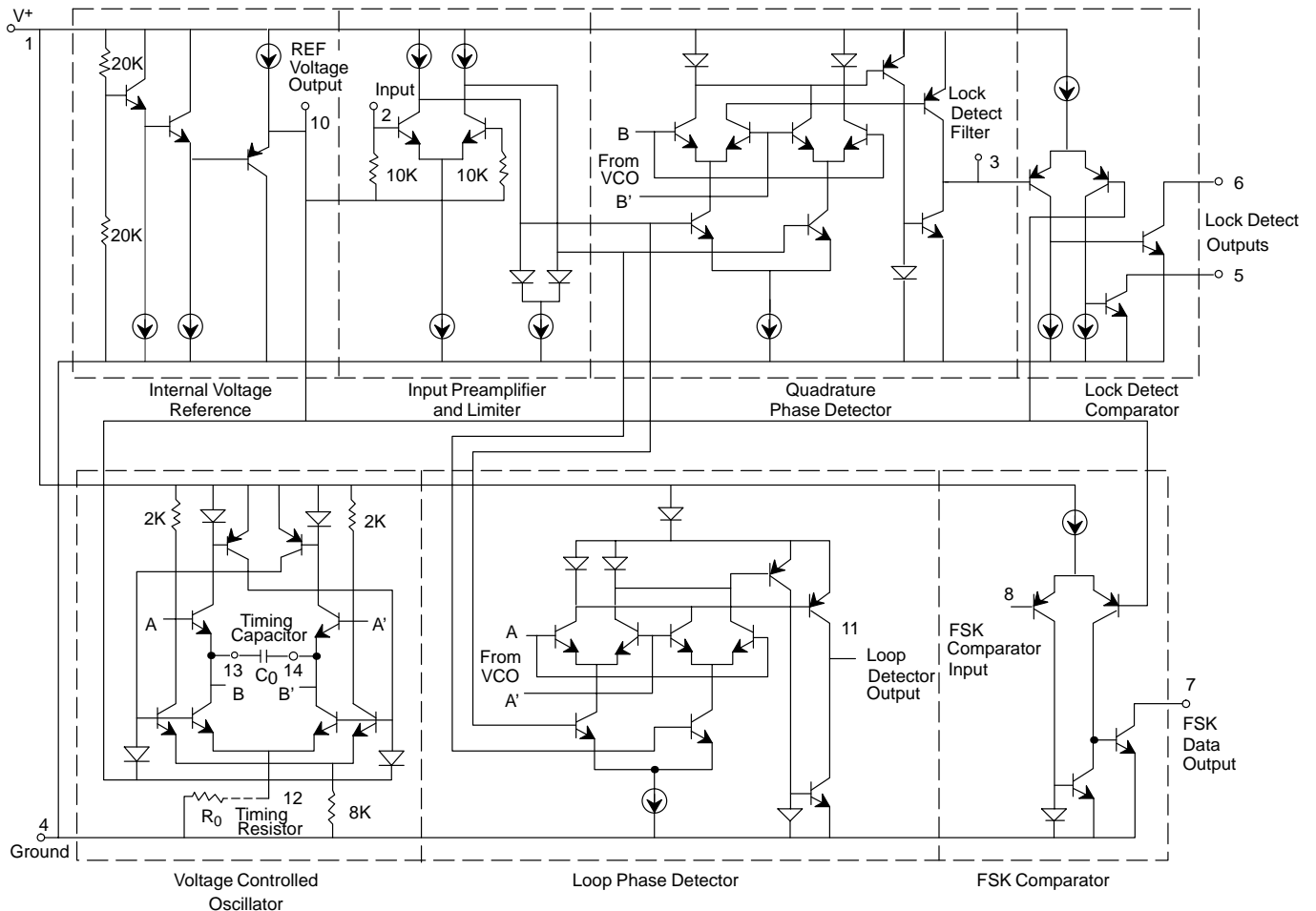
Figure 14. Equivalent Schematic Diagram

EXAR

14 LEAD CERAMIC DUAL-IN-LINE
(300 MIL CDIP)

Rev. 1.00

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.685	0.785	17.40	19.94
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

14 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)

Rev. 1.00
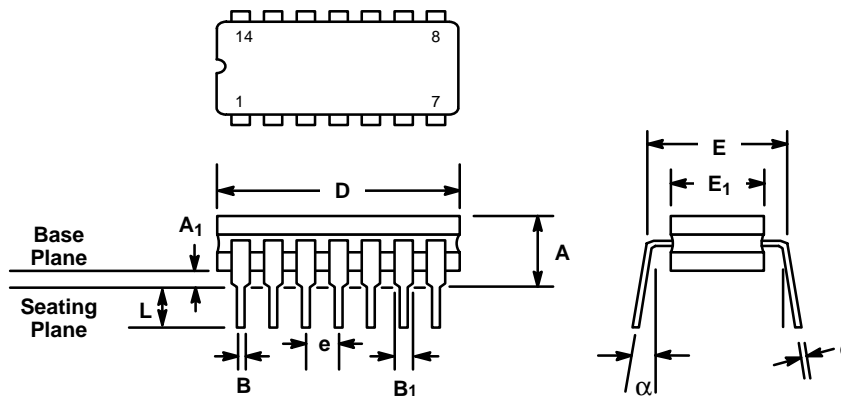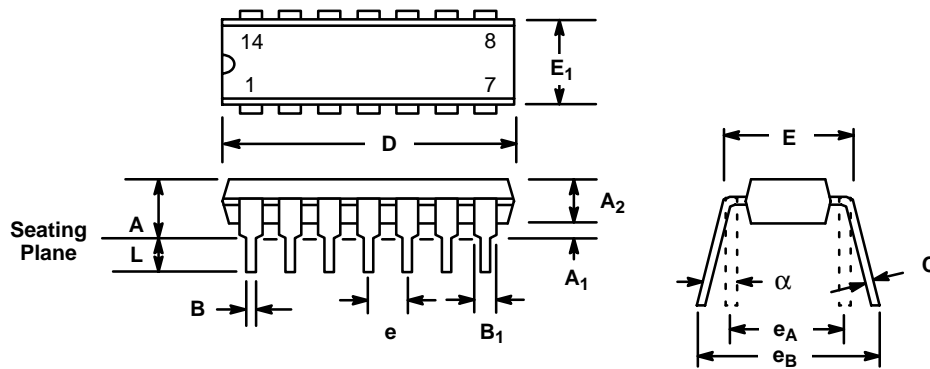
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A$_1$	0.015	0.070	0.38	1.78
A$_2$	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B$_1$	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.725	0.795	18.42	20.19
E	0.300	0.325	7.62	8.26
E$_1$	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e$_A$	0.300 BSC		7.62 BSC	
e$_B$	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

EXAR

14 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)

Rev. 1.00

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

NOTICE

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$\mathcal{N}$ a t i o n a l *S e m i c o n d u c t o r*

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per ˚C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram
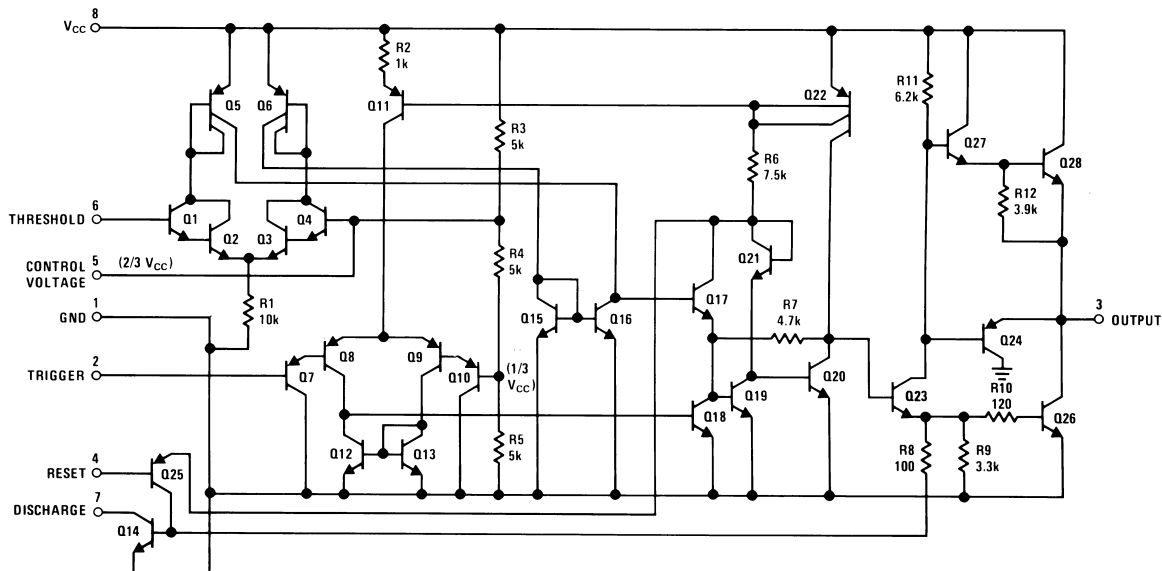
DS007851-1

Connection Diagram

**Dual-In-Line, Small Outline
and Molded Mini Small Outline Packages**

DS007851-3

Top View
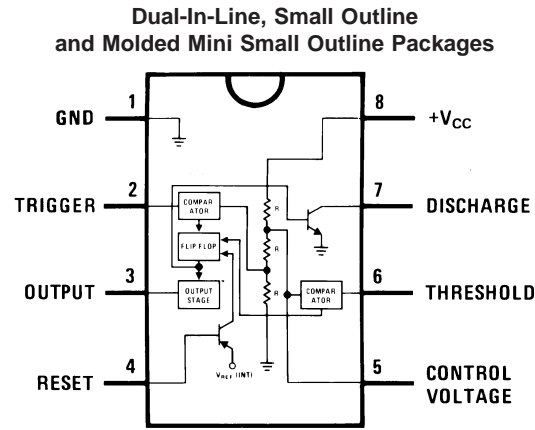
Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package		
Soldering (10 Seconds)		260°C
Small Outline Packages		
(SOIC and MSOP)		
Vapor Phase (60 Seconds)		215°C
Infrared (15 Seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_{CC} = +5V to +15V, unless otehwise specified)

Parameter	Conditions	Limits LM555C			Units
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	
	V_{CC} = 15V, R_L = ∞		10	15	mA
	(Low State) (Note 4)				
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ,		50		ppm/°C
	C = 0.1μF, (Note 5)				
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ,		150		ppm/°C
	C = 0.1μF, (Note 5)				
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25˚C based on a +150˚C maximum junction temperature and a thermal resistance of 106˚C/W (DIP), 170˚C/W (S0-8), and 204˚C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 6: This will determine the maximum value of R_A + R_B for 15V operation. The maximum total (R_A + R_B) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics

**Minimuim Pulse Width
Required for Triggering**

DS007851-4
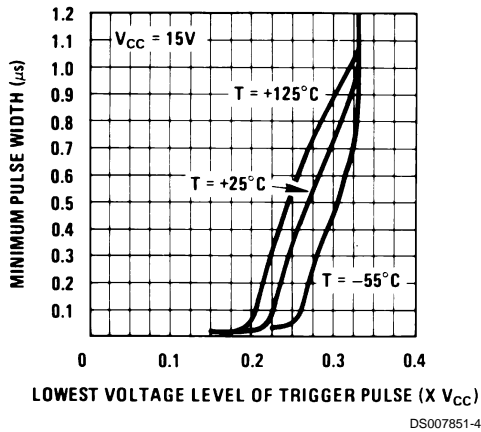
**Supply Current vs.
Supply Voltage**

DS007851-19
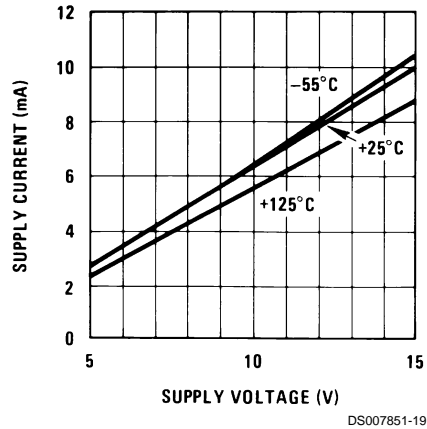
**High Output Voltage vs.
Output Source Current**
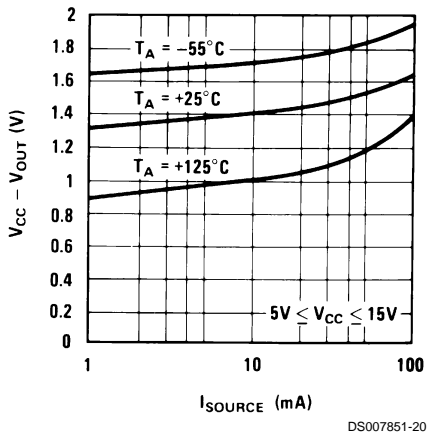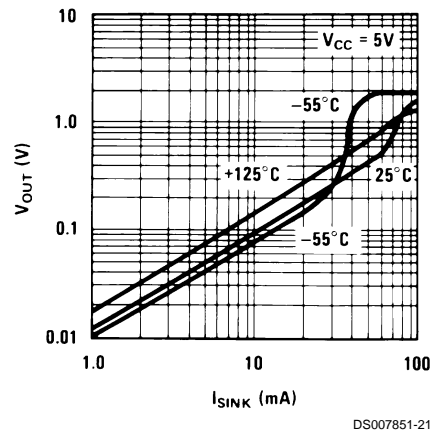
DS007851-20

**Low Output Voltage vs.
Output Sink Current**

DS007851-21

**Low Output Voltage vs.
Output Sink Current**

DS007851-22
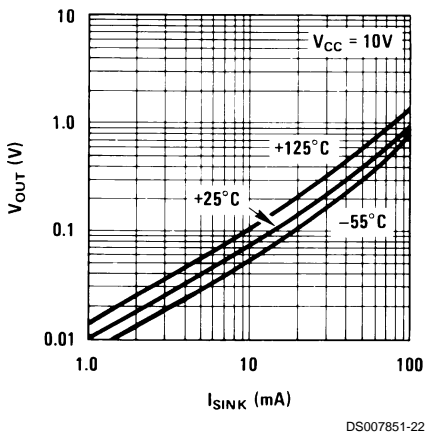
**Low Output Voltage vs.
Output Sink Current**
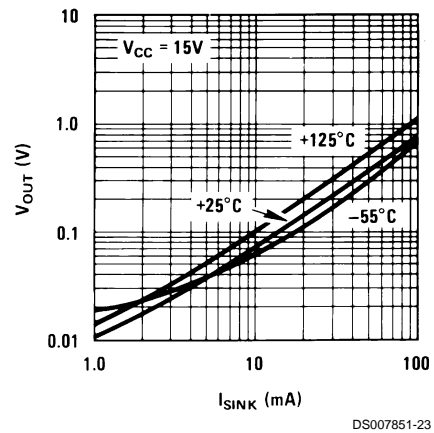
DS007851-23

Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse
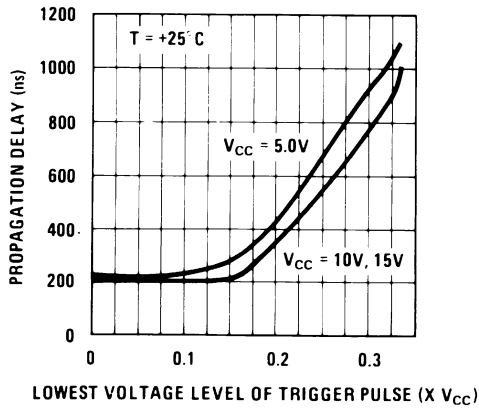
DS007851-24

Output Propagation Delay vs. Voltage Level of Trigger Pulse
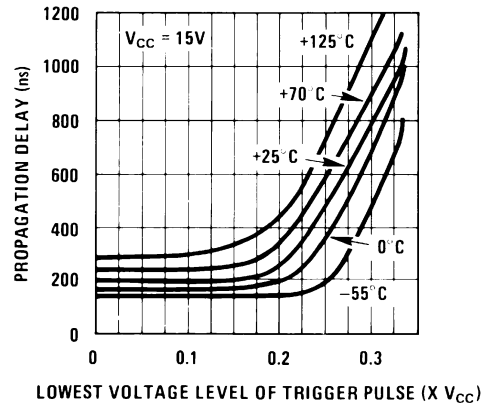
DS007851-25

Discharge Transistor (Pin 7) Voltage vs. Sink Current
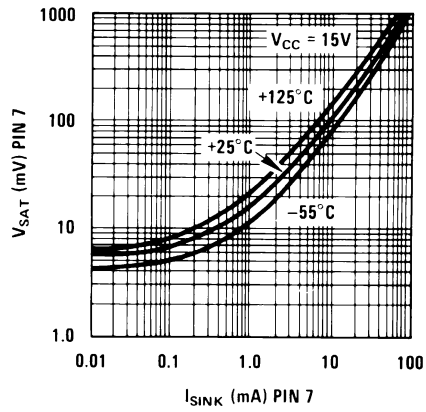
DS007851-26

Discharge Transistor (Pin 7) Voltage vs. Sink Current
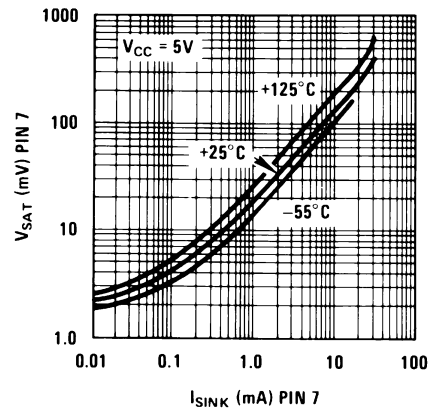
DS007851-27

Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.
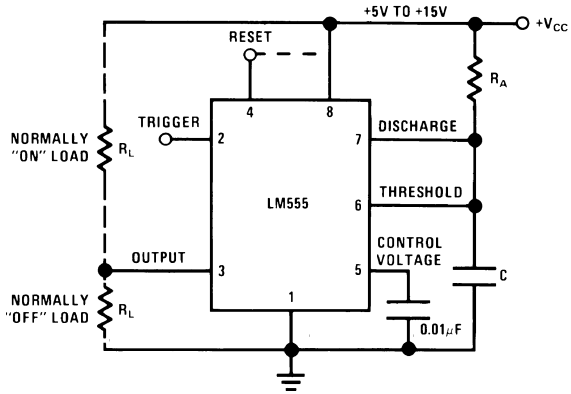
FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.
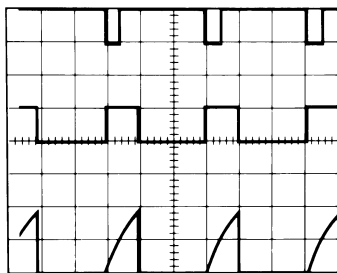
V_{CC} = 5V   Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV.   Middle Trace: Output 5V/Div.
R_A = 9.1kΩ   Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01µF

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10µs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

**NOTE:** In monostable operation, the trigger should be driven high before the end of timing cycle.
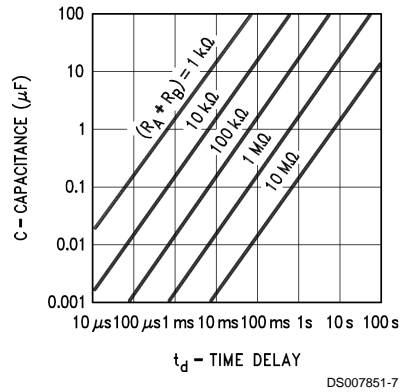
FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.
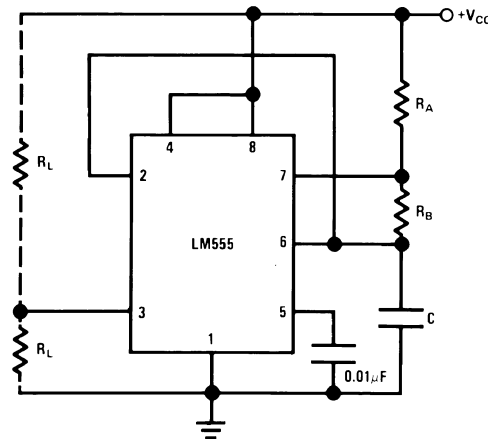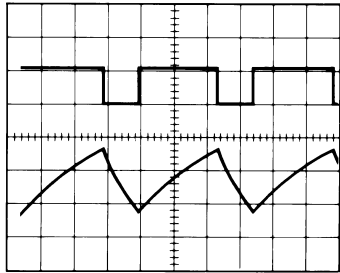

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.

V_{CC} = 5V   Top Trace: Output 5V/Div.
TIME = 20µs/DIV.   Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2 R_B) C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$
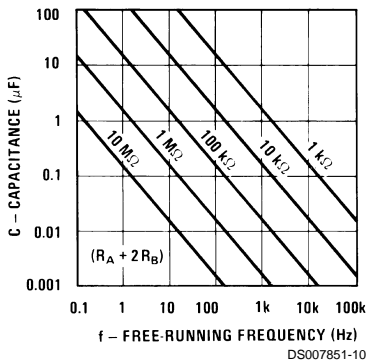
FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.
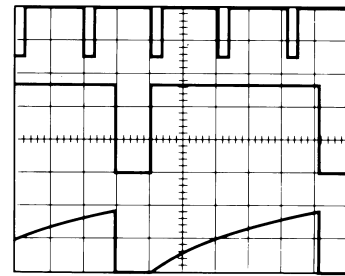

V_{CC} = 5V   Top Trace: Input 4V/Div.
TIME = 20µs/DIV.   Middle Trace: Output 2V/Div.
R_A = 9.1kΩ   Bottom Trace: Capacitor 2V/Div.
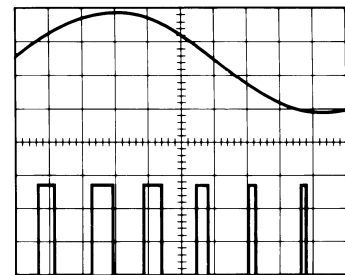C = 0.01µF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.
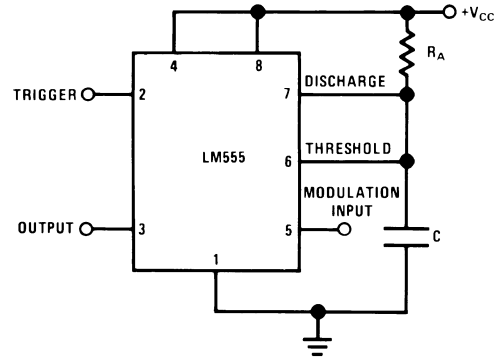
FIGURE 8. Pulse Width Modulator

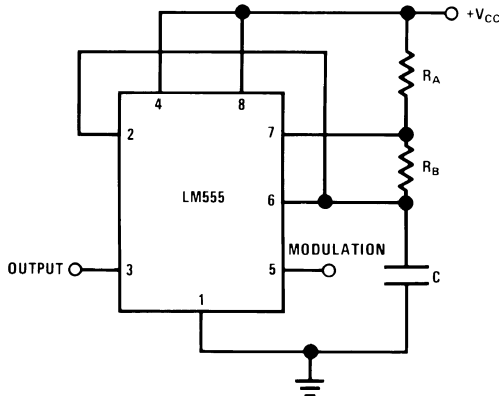V_{CC} = 5V   Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV.   Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

Applications Information (Continued)

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

DS007851-14

**FIGURE 10. Pulse Position Modulator**
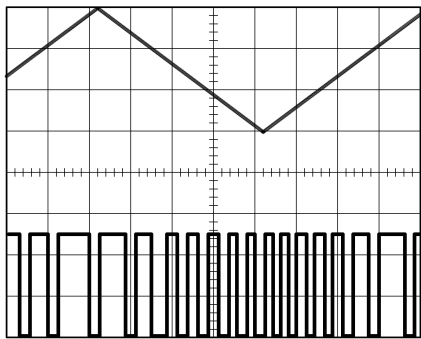
DS007851-15

V_{CC} = 5V   Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV.   Bottom Trace: Output 2V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.
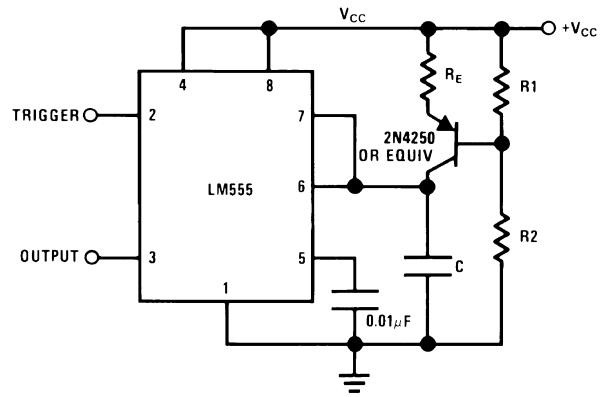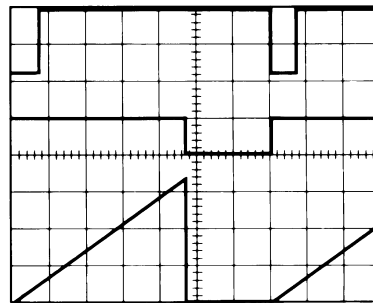

DS007851-16

FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3 \, V_{CC} \, R_E \, (R_1 + R_2) \, C}{R_1 \, V_{CC} - V_{BE} \, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \cong 0.6V$$

DS007851-17

V_{CC} = 5V   Top Trace: Input 3V/Div.
TIME = 20µs/DIV.   Middle Trace: Output 5V/Div.
R_1 = 47kΩ   Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

FIGURE 13. Linear Ramp
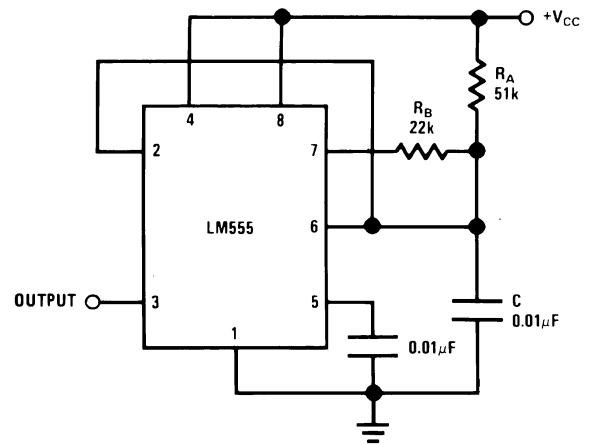
Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$\left[(R_A\ R_B)/(R_A + R_B) \right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A} \right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

DS007851-18

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.
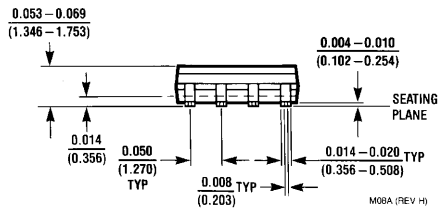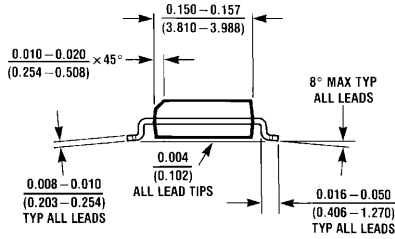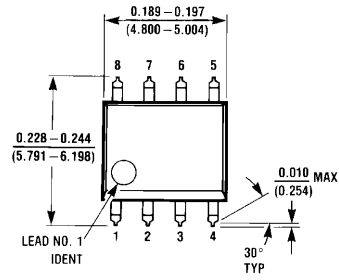
ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.
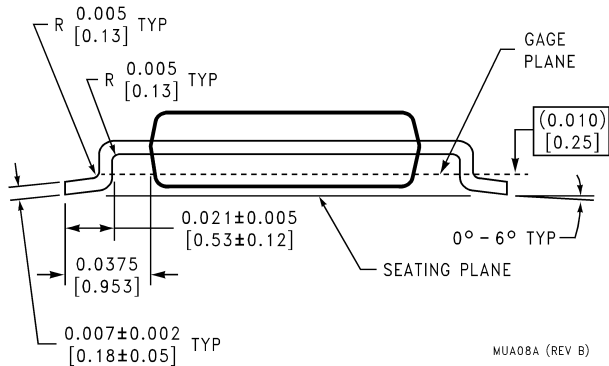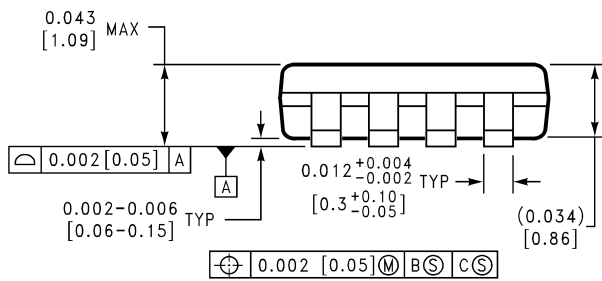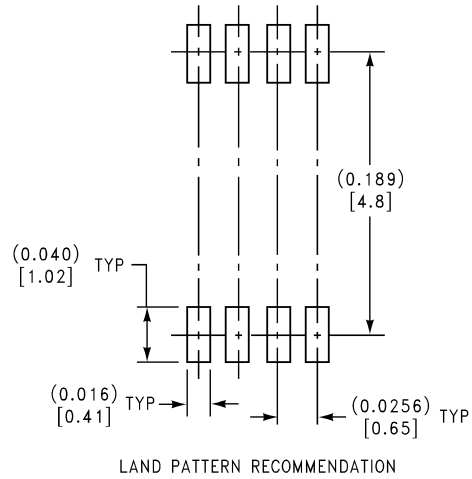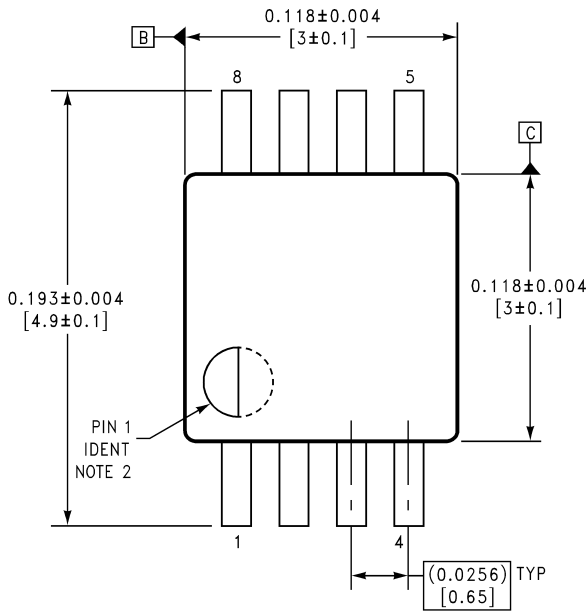
Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

0.189 − 0.197
(4.800 − 5.004)

8 7 6 5

0.228 − 0.244
(5.791 − 6.198)

0.010 MAX
(0.254)

LEAD NO. 1
IDENT

1 2 3 4

30°
TYP

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020 × 45°
(0.254 − 0.508)

8° MAX TYP
ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M08A (REV H)

Small Outline Package (M)
NS Package Number M08A

0.118±0.004
[3±0.1]

B

8   5

C

0.193±0.004
[4.9±0.1]

0.118±0.004
[3±0.1]

PIN 1
IDENT
NOTE 2

1   4

(0.0256) TYP
[0.65]

(0.189)
[4.8]

(0.040)
[1.02] TYP

(0.016) TYP
[0.41]

(0.0256) TYP
[0.65]

LAND PATTERN RECOMMENDATION

0.043
[1.09] MAX

0.002 [0.05] A

A

0.002 − 0.006 TYP
[0.06 − 0.15]

0.012 +0.004 −0.002 TYP
[0.3 +0.10 −0.05]

(0.034)
[0.86]

0.002 [0.05] M B S C S

R 0.005 TYP
[0.13]

R 0.005 TYP
[0.13]

GAGE
PLANE

(0.010)
[0.25]

0.021±0.005
[0.53±0.12]

0.0375
[0.953]

0.007±0.002 TYP
[0.18±0.05]

0° − 6° TYP

SEATING PLANE

MUA08A (REV B)

8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.373 − 0.400
(9.474 − 10.16)

0.090
(2.286)

0.092
(2.337) DIA

PIN NO. 1 IDENT

OPTION 1

0.250 ± 0.005
(6.35 ± 0.127)

0.032 ± 0.005
(0.813 ± 0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

0.280
(7.112) MIN

0.030
(0.762) MAX

0.300 − 0.320
(7.62 − 8.128)

0.040
(1.016) TYP

0.039
(0.991)

0.145 − 0.200
(3.683 − 5.080)

20° ± 1°

0.130 ± 0.005
(3.302 ± 0.127)

95° ± 5°

0.125 − 0.140
(3.175 − 3.556)

0.020
(0.508)
MIN

0.009 − 0.015
(0.229 − 0.381)

0.125
(3.175)
DIA
NOM

0.065
(1.651)

90° ± 4°
TYP

$0.325 \begin{smallmatrix} +0.040 \\ -0.015 \end{smallmatrix}$
$\left(8.255 \begin{smallmatrix} +1.016 \\ -0.381 \end{smallmatrix}\right)$

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

0.045 ± 0.015
(1.143 ± 0.381)

0.060
(1.524)

0.050
(1.270)

N08E (REV F)

Molded Dual-In-Line Package (N)
NS Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.