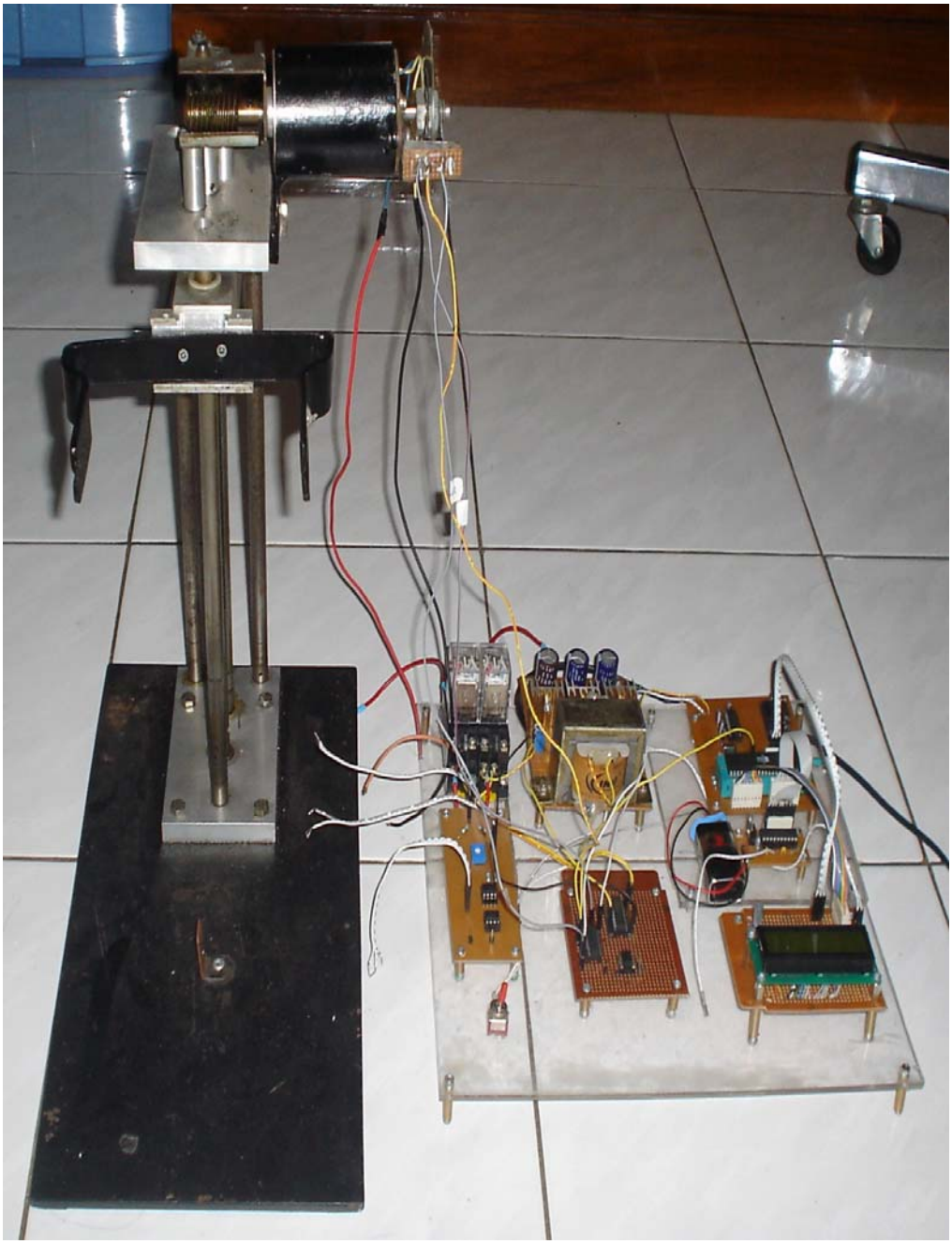
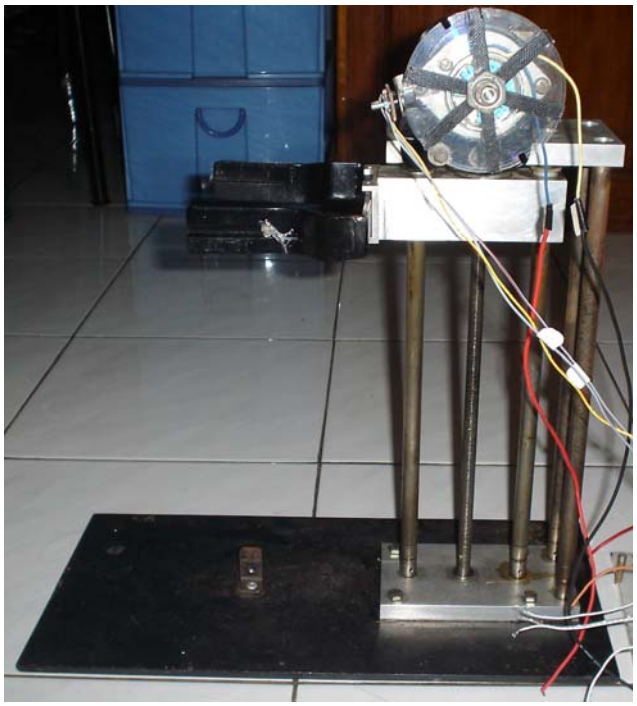
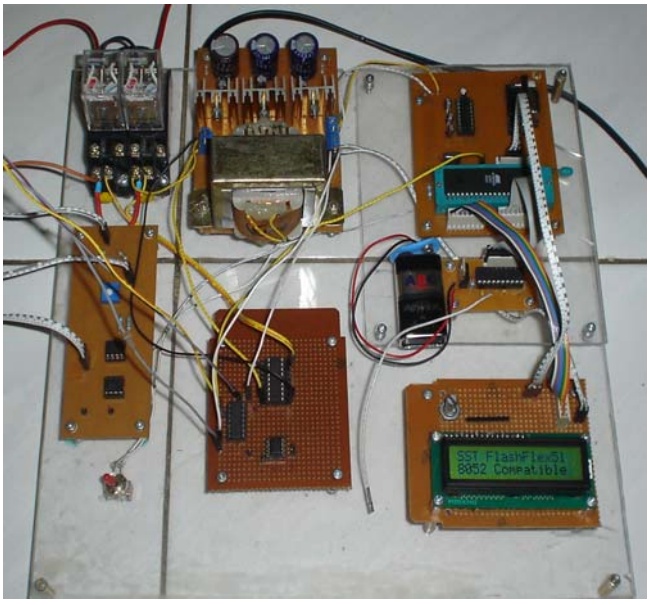
LAMPIRAN A : FOTO ALAT






SST FlashFlex51
8052 Compatible

Natural V 100

Thermacell

LAMPIRAN B :
LISTING PROGRAM MIKROKONTROLER DAN BORLAND DELPHI

LISTING PROGRAM MIKROKONTROLER

```
org 0h9
 data1      equ  051
 data2      equ  052
 read       equ  p2.5
 write      equ  p2.6
 int        equ  p2.7
 int1       equ  80
 koreksi    EQU 19H
 awal    :  ljmp utama
            inc r7
            reti

UTAMA : NOP
 org 10h
 mov ie,#int1
 mov r7,#00
 mov p1,#00h
 mov p2,#00h
 mov p0,#00h
 mov dptr,#00h
 mov a,#00h
 mov r0,#00h
 mov r1,#00h
 mov r2,#00h
 mov r3,#00h
 mov r4,#00h
 mov r5,#00h
 mov r6,#00h
 mov r7,#00h
 mov p0,#0ffh
 call init
 call delay
 nop
 call delay

sch : nop
      call inchar
      cjne a,#20h,sch
      call delay
      setb p1.1
      mov b,#00h
      call lg
      clr p1.1
      call hit
      mov a,r0
      call tulis
      call delay
```

```
        mov a,r1
        call tulis
        call delay
        mov a,r7
        call delay
        call tulis
        call delay
        nop
        sjmp awal

lg      : mov a,r5
          call adc
          nop
          cjne a,b,satu
          sjmp lg
satu    : jc kecil
          sjmp besar
besar   : mov b,a
          sjmp lg

kecil   : mov r5,a
          mov r6,b
          mov b,r5
          mov a,r6
          subb a,b
          mov b,#koreksi
          cjne a,b,dua
          sjmp habis
dua     : jc lg
          sjmp habis
habis   : ret


ADC     : mov P0, #00h
          setb P2.5
          clr  P2.6
          setb P2.6
WAIT    : jb P2.7,WAIT
          clr P2.5
          mov A, P0
          ret

init    : mov  tmod,#20h
          mov  TH1,#data2
          setb TR1
          mov  scon,#data1
          ret
```

```
inchar  : nop
          jnb ri,inchar
          mov a,sbuf
          ret

 tulis  : call outchr
          call delay
          ret

outchr  : nop
          jnb ti,outchr
          mov sbuf,a
          ret

hit     : mov r5,a
          anl a,#11110000b
          rl a
          rl a
          rl a
          rl a
          mov b,#16
          mul ab
          mov r6,a

          mov a,r5
          anl a,#00001111b
          mov b,a
          mov a,r6
          add a,b
          mov b,#5
          div ab
          mov r5,a
          mov r6,b
          mov a,r5
          mov b,#10
          div ab
          mov r0,a
          mov r1,b
          ret

delay :   mov r1,#39
dly0  :   mov r2,#39
dly1  :   mov r3,#39
dly2  :   djnz r3,dly2
          djnz r2,dly1
          djnz r1,dly0
          ret
```

LISTING PROGRAM BORLAND DELPHI

```
unit U_hendry4;

interface

uses
  Windows, Messages, SysUtils, Variants, Classes, Graphics, Controls, Forms,
  Dialogs, StdCtrls, ExtCtrls, AfPortControls, AfDataDispatcher, AfComPort,
  AfViewers, AfDataTerminal, Grids;

type
  TForm1 = class(TForm)
    AfComPort1: TAfComPort;
    AfPortRadioGroup1: TAfPortRadioGroup;
    Label1       : TLabel;
    GroupBox1: TGroupBox;
    Panel1       : TPanel;
    Label2       : TLabel;
    GroupBox2: TGroupBox;
    Panel2       : TPanel;
    Button1      : TButton;
    Label3       : TLabel;
    Label7       : TLabel;
    Edit4        : TEdit;
    Edit5        : TEdit;
    Label8       : TLabel;
    Label9       : TLabel;
    Button2      : TButton;
    Label5       : TLabel;
    Label10      : TLabel;
    Button3      : TButton;
    Image1       : TImage;
    Edit2        : TEdit;
    Timer1       : TTimer;
    StringGrid1: TStringGrid;
    GroupBox3: TGroupBox;
    Label6       : TLabel;
    Button4      : TButton;
    procedure Button1Click(Sender: TObject);
    procedure AfComPort1DataRecived(Sender: TObject; Count: Integer);
    procedure Button3Click(Sender: TObject);
    procedure Timer1Timer(Sender: TObject);
    procedure Button2Click(Sender: TObject);
    procedure Button4Click(Sender: TObject);
    procedure AfComPort1CTSChanged(Sender: TObject);
```

```
object Form1: TForm1
  Left        = 192
  Top         = 107
  Width     = 544
  Height    = 375
  Caption  = 'Form1'
  Color      = clBtnFace
  Font.Charset       = DEFAULT_CHARSET
  Font.Color         = clWindowText
  Font.Height        = -11
  Font.Name         = 'MS Sans Serif'
  Font.Style          = []
  OldCreateOrder = False
  OnCreate           = FormCreate
  PixelsPerInch     = 96
  TextHeight         = 13
  object AfComPort1: TAfComPort
  OnCTSChanged = AfComPort1CTSChanged
   Left = 128
   Top = 152
  end
  end
  private
    { Private declarations }
  public
    { Public declarations }
  end;

var
Form1: TForm1;

implementation

{$R *.dfm}
var
l0,l1 : integer   ;
x1 : real = 11 ;
x : array [1..35] of  char ;
y : array [1..15] of integer;
a : integer =0 ;
procedure TForm1.Button1Click(Sender: TObject);
var
tensil,my,l1,f,v,c,d,e : real ;
K1,K2,K3,K4,K5,k6 : integer;
begin
k1 := strtoint(x[1]);
 k2 :=  strtoint(x[2]);
 c   := k1 +(k2/10);
```

```
 k3 := strtoint(x[3]);
 k4 :=  strtoint(x[4]);
 d   := k3 +(k4/10);
 l1  := round(d/6);
 e :=  l1*0.04 ;
if( x1 =11) then
begin
edit4.Text := 'Tdk bisa';
edit5.Text := 'Tdk bisa';
end  ;

if(x1<>11) then
begin
v := c;
f := ((1.73*v*v)+(5.67*v)+0.25);
tensile := ((f*10000/(0.25))/1000000);
my :=(tensil/l1/0.1);
edit4.Text := floattostr(tensil);
edit5.Text := floattostr(my);
end;
end;

procedure TForm1.AfComPort1DataRecived(Sender: TObject; Count: Integer);
begin
x[a] := form1.AfComPort1.ReadChar ;
inc(a);
form1.GroupBox3.Visible := true;
form1.AfComPort1.PurgeRX;
timer1.Enable  :=  False ;
end;

procedure TForm1.Button3Click(Sender: TObject);
var
u : integer;
begin
u := $20;
form1.AfComPort1.WriteData(u,1);
x := 0;
end;

var
b : integer =0;

procedure TForm1.Button2Click(Sender: TObject);
begin
edit2.Clear;
edit4.Clear;
edit5.Clear;
end;
```

```
procedure TForm1.Button4Click(Sender: TObject);
begin
form1.GroupBox3.Visible := false;
end;
end.
```

LISTING PROGRAM SERIAL

```
unit AfComPort;

{$I PVDEFINE.INC}

interface

uses
  Windows, Messages, SysUtils, Classes, Graphics, Controls, Forms, Dialogs,
  AfComPortCore, AfSafeSync, AfDataDispatcher;

type
  TAfBaudrate = (br110, br300, br600, br1200, br2400, br4800, br9600, br14400,
   br19200, br38400, br56000, br57600, br115200, br128000, br256000, brUser);
  TAfParity = (paNone, paOdd, paEven, paMark, paSpace);
  TAfDatabits = (db4, db5, db6, db7, db8);
  TAfStopbits = (sbOne, sbOneAndHalf, sbTwo);
  TAfFlowControl = (fwNone, fwXOnXOff, fwRtsCts, fwDtrDsr);

  TAfComOption = (coParityCheck, coDsrSensitivity, coIgnoreXOff, coErrorChar,
  coStripNull);
  TAfComOptions = set of TAfComOption;

  EAfComPortError = class(Exception);

  TAfComPortEventKind = TAfCoreEvent;

  TAfComPortEventData = DWORD;

  TAfCPTCoreEvent = procedure(Sender: TObject; EventKind: TAfComPortEventKind;
  Data: TAfComPortEventData) of object;
  TAfCPTErrorEvent = procedure(Sender: TObject; Errors: DWORD) of object;
  TAfCPTDataReceivedEvent = procedure(Sender: TObject; Count: Integer) of object;

  TAfCustomSerialPort = class(TAfDataDispConnComponent)
  private
    FAutoOpen: Boolean;
    FBaudRate: TAfBaudrate;
    FClosing: Boolean;
    FCoreComPort: TAfComPortCore;
    FDatabits: TAfDatabits;
    FDCB: TDCB;
    FDTR: Boolean;
    FEventThreadPriority: TThreadPriority;
    FFlowControl: TAfFlowControl;
```

```
    FInBufSize: Integer;
    FOptions: TAfComOptions;
    FOutBufSize: Integer;
    FParity: TAfParity;
    FRTS: Boolean;
    FStopbits: TAfStopbits;
    FSyncID: TAfSyncSlotID;
    FUserBaudRate: Integer;
    FXOnChar, FXOffChar: Char;
    FXOnLim, FXOffLim: Word;
    FOnCTSChanged: TNotifyEvent;
    FOnDataRecived: TAfCPTDataReceivedEvent;
    FOnDSRChanged: TNotifyEvent;
    FOnRLSDChanged: TNotifyEvent;
    FOnRINGDetected: TNotifyEvent;
    FOnLineError: TAfCPTErrorEvent;
    FOnOutBufFree: TNotifyEvent;
    FOnNonSyncEvent: TAfCPTCoreEvent;
    FOnPortClose: TNotifyEvent;
    FOnPortOpen: TNotifyEvent;
    FOnSyncEvent: TAfCPTCoreEvent;
    Sync_Event: TAfComPortEventKind;
    Sync_Data: TAfComPortEventData;
    FWriteThreadPriority: TThreadPriority;
    procedure CheckClose;
    procedure CoreComPortEvent(Sender: TAfComPortCore; EventKind: TAfCoreEvent;
Data: DWORD);
    function GetActive: Boolean;
    function GetComStat (Index: Integer): Boolean;
    function GetHandle: THandle;
    function GetModemStatus(Index: Integer): Boolean;
    function IsUserBaudRateStored: Boolean;
    procedure SafeSyncEvent(ID: TAfSyncSlotID);
    procedure Set_DTR(const Value: Boolean);
    procedure Set_RTS(const Value: Boolean);
    procedure SetActive(const Value: Boolean);
    procedure SetBaudRate(const Value: TAfBaudrate);
    procedure SetDCB(const Value: TDCB);
    procedure SetDatabits(const Value: TAfDatabits);
    procedure SetEventThreadPriority(const Value: TThreadPriority);
    procedure SetFlowControl(const Value: TAfFlowControl);
    procedure SetInBufSize(const Value: Integer);
    procedure SetStopbits(const Value: TAfStopbits);
    procedure SetOptions(const Value: TAfComOptions);
    procedure SetOutBufSize(const Value: Integer);
    procedure SetParity(const Value: TAfParity);
```

```
 procedure SetUserBaudRate(const Value: Integer);
    procedure SetWriteThreadPriority(const Value: TThreadPriority);
    procedure SetXOnChar(const Value: Char);
    procedure SetXOnLim(const Value: Word);
    procedure SetXOffChar(const Value: Char);
    procedure SetXOffLim(const Value: Word);
    procedure UpdateDCB;
    procedure UpdateOnOffLimit;
  protected
    procedure DispatchComEvent(EventKind: TAfComPortEventKind; Data:
TAfComPortEventData);
    procedure DoOutBufFree;
    procedure DoPortData(Count: Integer);
    procedure DoPortEvent(Event: DWORD);
    procedure DoPortClose;
    procedure DoPortOpen;
    function GetNumericBaudrate: Integer;
    procedure InternalOpen; dynamic; abstract;
    procedure Loaded; override;
    procedure RaiseError(const ErrorMsg: String); dynamic;
    property AutoOpen: Boolean read FAutoOpen write FAutoOpen default False;
    property BaudRate: TAfBaudrate read FBaudRate write SetBaudRate default
br115200;
    property Core: TAfComPortCore read FCoreComPort;
    property Databits: TAfDatabits read FDatabits write SetDatabits default db8;
    property DTR: Boolean read FDTR write Set_DTR default True;
    property EventThreadPriority: TThreadPriority read FEventThreadPriority write
SetEventThreadPriority default tpNormal;
    property FlowControl: TAfFlowControl read FFlowControl write SetFlowControl
default fwNone;
    property InBufSize: Integer read FInBufSize write SetInBufSize default 4096;
    property Options: TAfComOptions read FOptions write SetOptions default [];
    property OutBufSize: Integer read FOutBufSize write SetOutBufSize default 2048;
    property Parity: TAfParity read FParity write SetParity default paNone;
    property RTS: Boolean read FRTS write Set_RTS default True;
    property Stopbits: TAfStopbits read FStopbits write SetStopbits default sbOne;
    property UserBaudRate: Integer read FUserBaudRate write SetUserBaudRate stored
IsUserBaudRateStored;
    property WriteThreadPriority: TThreadPriority read FWriteThreadPriority write
SetWriteThreadPriority default tpHighest;
    property XOnChar: Char read FXOnChar write SetXOnChar default #17;
    property XOffChar: Char read FXOffChar write SetXOffChar default #19;
    property XOnLim: Word read FXOnLim write SetXOnLim default 0;
    property XOffLim: Word read FXOffLim write SetXOffLim default 0;
    property OnCTSChanged: TNotifyEvent read FOnCTSChanged write
FOnCTSChanged;
```

```
property OnDataRecived: TAfCPTDataReceivedEvent read FOnDataRecived write
FOnDataRecived;
   property OnDSRChanged: TNotifyEvent read FOnDSRChanged write
FOnDSRChanged;
   property OnRLSDChanged: TNotifyEvent read FOnRLSDChanged write
FOnRLSDChanged;
   property OnRINGDetected: TNotifyEvent read FOnRINGDetected write
FOnRINGDetected;
   property OnLineError: TAfCPTErrorEvent read FOnLineError write FOnLineError;
   property OnNonSyncEvent: TAfCPTCoreEvent read FOnNonSyncEvent write
FOnNonSyncEvent;
   property OnOutBufFree: TNotifyEvent read FOnOutBufFree write FOnOutBufFree;
   property OnPortClose: TNotifyEvent read FOnPortClose write FOnPortClose;
   property OnPortOpen: TNotifyEvent read FOnPortOpen write FOnPortOpen;
   property OnSyncEvent: TAfCPTCoreEvent read FOnSyncEvent write FOnSyncEvent;
   public
   procedure Close; override;
   constructor Create(AOwner: TComponent); override;
   destructor Destroy; override;
   function ExecuteConfigDialog: Boolean; dynamic; abstract;
   function InBufUsed: Integer;
   procedure Open; override;
   function OutBufFree: Integer;
   function OutBufUsed: Integer;
   procedure PurgeRX;
   procedure PurgeTX;
   function ReadChar: Char;
   procedure ReadData(var Buf; Size: Integer);
   function ReadString: String;
   function SynchronizeEvent(EventKind: TAfComPortEventKind; Data:
TAfComPortEventData; Timeout: Integer): Boolean;
   procedure WriteChar(C: Char);
   procedure WriteData(const Data; Size: Integer); override;
   procedure WriteString(const S: String);
   property Active: Boolean read GetActive write SetActive;
   property DCB: TDCB read FDCB write SetDCB;
   property Handle: THandle read GetHandle;
   property CTSHold: Boolean index 1 read GetComStat;
   property DSRHold: Boolean index 2 read GetComStat;
   property RLSDHold: Boolean index 3 read GetComStat;
   property XOffHold: Boolean index 4 read GetComStat;
   property XOffSent: Boolean index 5 read GetComStat;
   property CTS: Boolean index 1 read GetModemStatus;
   property DSR: Boolean index 2 read GetModemStatus;
   property RING: Boolean index 3 read GetModemStatus;
   property RLSD: Boolean index 4 read GetModemStatus;
```

```
end;

TAfCustomComPort = class(TAfCustomSerialPort)
private
  FComNumber: Word;
  procedure SetComNumber(const Value: Word);
protected
  property ComNumber: Word read FComNumber write SetComNumber default 0;
  procedure InternalOpen; override;
  function GetDeviceName: String;
public
  function ExecuteConfigDialog: Boolean; override;
  procedure SetDefaultParameters;
  function SettingsStr: String;
end;

TAfComPort = class(TAfCustomComPort)
public
  property Core;
published
  property AutoOpen;
  property BaudRate;
  property ComNumber;
  property Databits;
  property DTR;
  property EventThreadPriority;
  property FlowControl;
  property InBufSize;
  property Options;
  property OutBufSize;
  property Parity;
  property RTS;
  property Stopbits;
  property UserBaudRate;
  property WriteThreadPriority;
  property XOnChar;
  property XOffChar;
  property XOnLim;
  property XOffLim;
  property OnCTSChanged;
  property OnDataRecived;
  property OnDSRChanged;
  property OnLineError;
  property OnNonSyncEvent;
  property OnOutBufFree;
  property OnPortClose;
```

```
property OnPortOpen;
    property OnRINGDetected;
    property OnRLSDChanged;
    property OnSyncEvent;
  end;

implementation

resourcestring
  sErrorSetDCB = 'Error setting parameters from DCB';
  sPortIsNotClosed = 'Port is not closed';
  sReadError = 'Read data error';
  sWriteError = 'Write data error [requested: %d, free: %d]';

const
  DCB_BaudRates: array[TAfBaudRate] of DWORD =
    (CBR_110, CBR_300, CBR_600, CBR_1200, CBR_2400, CBR_4800, CBR_9600,
     CBR_14400, CBR_19200, CBR_38400, CBR_56000, CBR_57600, CBR_115200,
     CBR_128000, CBR_256000, 0);
  DCB_DataBits: array[TAfDatabits] of DWORD =
    (4, 5, 6, 7, 8);
  DCB_Parity: array[TAfParity] of DWORD =
    (NOPARITY, ODDPARITY, EVENPARITY, MARKPARITY, SPACEPARITY);
  DCB_StopBits: array[TAfStopbits] of DWORD =
    (ONESTOPBIT, ONE5STOPBITS, TWOSTOPBITS);
  DCB_FlowControl: array[TAfFlowControl] of DWORD =
    (0,
     fOutX or fInX,
     fOutxCtsFlow or fRtsControlHandshake,
     fOutxDsrFlow or fDtrControlHandshake);
  DCB_ComOptions: array[TAfComOption] of LongInt =
    (fParity, fDsrSensitivity, fTXContinueOnXoff, fErrorChar, fNull);

{ TAfCustomSerialPort }

procedure TAfCustomSerialPort.CheckClose;
begin
  if Active then
    RaiseError(sPortIsNotClosed);
end;

procedure TAfCustomSerialPort.Close;
begin
  FClosing := True;
  inherited Close;
  if not (csDesigning in ComponentState) then
```

```
begin
    AfEnableSyncSlot(FSyncID, False);
    FCoreComPort.CloseComPort;
    DoPortClose;
  end;
  FClosing := False;
end;

procedure TAfCustomSerialPort.CoreComPortEvent(Sender: TAfComPortCore;
  EventKind: TAfCoreEvent; Data: DWORD);
var
  P: Pointer;
  Count: Integer;
  NeedCallSyncEvents: Boolean;
begin
  if FClosing or (csDestroying in ComponentState) then Exit;
  NeedCallSyncEvents := True;
  if EventKind = ceException then
    SynchronizeEvent(EventKind, Data, AfSynchronizeTimeout)
  else
  begin
    if Assigned(FDispatcher) then
      case TAfComPortEventKind(EventKind) of
        ceLineEvent:
          if Data and EV_RXCHAR <> 0 then
          begin
            if Data and (not EV_RXCHAR) = 0 then
              NeedCallSyncEvents := False; // there aren't any other events to dispatch
            Count := InBufUsed;
            GetMem(P, Count);
            try
              ReadData(P^, Count);
              FDispatcher.Dispatcher_WriteTo(P^, Count);
            finally
              FreeMem(P);
            end;
          end;
        ceNeedReadData:
          begin
            NeedCallSyncEvents := False;
            Count := Data;
            GetMem(P, Count);
            try
              ReadData(P^, Count);
              FDispatcher.Dispatcher_WriteTo(P^, Count);
            finally
```

```
    FreeMem(P);
          end;
        end;
      ceOutFree:
        begin
          NeedCallSyncEvents := Assigned(FOnOutBufFree); // some kind of optimization
          FDispatcher.Dispatcher_WriteBufFree;
        end;
    end;
    if Assigned(FOnNonSyncEvent) then
     FOnNonSyncEvent(Self, EventKind, Data)
    else
     if NeedCallSyncEvents then SynchronizeEvent(EventKind, Data,
AfSynchronizeTimeout);
  end;
end;

constructor TAfCustomSerialPort.Create(AOwner: TComponent);
begin
  inherited Create(AOwner);
  FBaudRate := br115200;
  FDatabits := db8;
  FDTR := True;
  FEventThreadPriority := tpNormal;
  FFlowControl := fwNone;
  FInBufSize := 4096;
  FOptions := [];
  FOutBufSize := 2048;
  FParity := paNone;
  FRTS := True;
  FStopbits := sbOne;
  FWriteThreadPriority := tpHighest;
  FXOnChar := #17;
  FXOffChar := #19;
  if not (csDesigning in ComponentState) then
  begin
    FSyncID := AfNewSyncSlot(SafeSyncEvent);
    FCoreComPort := TAfComPortCore.Create;
    FCoreComPort.OnPortEvent := CoreComPortEvent;
    UpdateDCB;
  end;
end;

destructor TAfCustomSerialPort.Destroy;
begin
  if not (csDesigning in ComponentState) then
```

```
    begin
   AfReleaseSyncSlot(FSyncID);
   FCoreComPort.Free;
   FCoreComPort := nil;
  end;
  inherited Destroy;
end;

procedure TAfCustomSerialPort.DispatchComEvent(EventKind:
TAfComPortEventKind; Data: TAfComPortEventData);
begin
  if FClosing or (csDestroying in ComponentState) then Exit;
  if Assigned(FOnSyncEvent) then FOnSyncEvent(Self, EventKind, Data);
  case EventKind of
    ceLineEvent:
      begin
        if Data and EV_RXCHAR <> 0 then
DoPortData(FCoreComPort.ComStatus.cbInQue);
        DoPortEvent(Data);
      end;
    ceOutFree:
      DoOutBufFree;
    ceNeedReadData:
      DoPortData(Data);
    ceException:
      raise Exception(Data);
  end;
end;

procedure TAfCustomSerialPort.DoOutBufFree;
begin
  if Assigned(FOnOutBufFree) then FOnOutBufFree(Self);
end;

procedure TAfCustomSerialPort.DoPortClose;
begin
  if Assigned(FOnPortClose) then FOnPortClose(Self);
end;

procedure TAfCustomSerialPort.DoPortData(Count: Integer);
begin
  if Assigned(FOnDataRecived) then FOnDataRecived(Self, Count);
end;

procedure TAfCustomSerialPort.DoPortEvent(Event: DWORD);
var
```

```
  LastError: DWORD;
begin
  LastError := FCoreComPort.ComError;
  if (Event and EV_ERR <> 0) {or (LastError <> 0)} then
  begin
    if Assigned(FOnLineError) then FOnLineError(Self, LastError);
  end;
  if (Event and EV_CTS <> 0) and Assigned(FOnCTSChanged) then
    FOnCTSChanged(Self);
  if (Event and EV_DSR <> 0) and Assigned(FOnDSRChanged) then
    FOnDSRChanged(Self);
  if (Event and EV_RING <> 0) and Assigned(FOnRINGDetected) then
    FOnRINGDetected(Self);
  if (Event and EV_RLSD <> 0) and Assigned(FOnRLSDChanged) then
    FOnRLSDChanged(Self);
end;

procedure TAfCustomSerialPort.DoPortOpen;
begin
  if Assigned(FOnPortOpen) then FOnPortOpen(Self);
end;

function TAfCustomSerialPort.GetActive: Boolean;
begin
  Result := Assigned(FCoreComPort) and FCoreComPort.IsOpen;
end;

function TAfCustomSerialPort.GetComStat(Index: Integer): Boolean;
begin
  Result := TComStateFlag(Index - 1) in FCoreComPort.ComStatus.Flags
end;

function TAfCustomSerialPort.GetHandle: THandle;
begin
  Result := FCoreComPort.Handle;
end;

function TAfCustomSerialPort.GetModemStatus(Index: Integer): Boolean;
const
  Mask: array[1..4] of DWORD = (MS_CTS_ON, MS_DSR_ON, MS_RING_ON,
MS_RLSD_ON);
begin
  Result := FCoreComPort.ModemStatus and Mask[Index] <> 0;
end;

function TAfCustomSerialPort.GetNumericBaudrate: Integer;
```

```
    begin
  if FBaudRate = brUser then
    Result := FUserBaudRate
  else
    Result := DCB_BaudRates[FBaudRate];
end;

function TAfCustomSerialPort.InBufUsed: Integer;
begin
  Result := FCoreComPort.ComStatus.cbInQue;
end;

function TAfCustomSerialPort.IsUserBaudRateStored: Boolean;
begin
  Result := FBaudRate = brUser;
end;

procedure TAfCustomSerialPort.Loaded;
begin
  inherited Loaded;
  if FAutoOpen then Open else UpdateDCB;
end;

procedure TAfCustomSerialPort.Open;
begin
  if not ((csDesigning in ComponentState) or FCoreComPort.IsOpen) then
  begin
    AfEnableSyncSlot(FSyncID, True);
    FCoreComPort.DCB := FDCB;
    FCoreComPort.InBuffSize := FInBufSize;
    FCoreComPort.OutBuffSize := FOutBufSize;
    FCoreComPort.EventThreadPriority := FEventThreadPriority;
    FCoreComPort.WriteThreadPriority := FWriteThreadPriority;
    FClosing := False;
    InternalOpen;
    DoPortOpen;
  end;
  inherited Open;
end;

function TAfCustomSerialPort.OutBufFree: Integer;
begin
  Result := FCoreComPort.OutBuffFree;
end;

function TAfCustomSerialPort.OutBufUsed: Integer;
```

```
    begin
  Result := FCoreComPort.OutBuffUsed;
end;

procedure TAfCustomSerialPort.PurgeRX;
begin
  if not FClosing then FCoreComPort.PurgeRX;
end;

procedure TAfCustomSerialPort.PurgeTX;
begin
  if not FClosing then FCoreComPort.PurgeTX;
end;

procedure TAfCustomSerialPort.RaiseError(const ErrorMsg: String);
begin
  raise EAfComPortError.CreateFmt('%s - %s ', [ErrorMsg, Name]);
end;

function TAfCustomSerialPort.ReadChar: Char;
begin
  ReadData(Result, Sizeof(Result));
end;

procedure TAfCustomSerialPort.ReadData(var Buf; Size: Integer);
begin
  if FClosing then Exit;
  if FCoreComPort.ReadData(Buf, Size) <> Size then
    RaiseError(sReadError);
end;

function TAfCustomSerialPort.ReadString: String;
var
  Size: Integer;
begin
  if FClosing then
    Result := ''
  else
  begin
    Size := FCoreComPort.ComStatus.cbInQue;
    SetLength(Result, Size);
    FCoreComPort.ReadData(Pointer(Result)^, Size);
  end;
end;

procedure TAfCustomSerialPort.SafeSyncEvent(ID: TAfSyncSlotID);
```

```
begin
  if not FClosing {Active} then DispatchComEvent(Sync_Event, Sync_Data);
end;

procedure TAfCustomSerialPort.SetActive(const Value: Boolean);
begin
  if Value then Open else Close;
end;

procedure TAfCustomSerialPort.SetBaudRate(const Value: TAfBaudrate);
begin
  if FBaudRate <> Value then
  begin;
    FBaudRate := Value;
    if FBaudRate <> brUser then FUserBaudRate := 0;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.SetDatabits(const Value: TAfDatabits);
begin
  if FDatabits <> Value then
  begin
    FDatabits := Value;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.SetDCB(const Value: TDCB);
var
  QBaudRate: TAfBaudrate;
  QDataBits: TAfDatabits;
  QParity: TAfParity;
  QStopBits: TAfStopbits;
  QFlowControl: TAfFlowControl;
  QOptions: TAfComOption;
  Found: Boolean;
begin
  if Value.DCBlength <> Sizeof(TDCB) then
    RaiseError(sErrorSetDCB);
  FDCB := Value;
  Found := False;
  for QBaudRate := Low(QBaudRate) to High(QBaudRate) do
    if FDCB.BaudRate = DCB_BaudRates[QBaudRate] then
    begin
      Found := True;
```

```
  FBaudRate := QBaudRate;
     Break;
   end;
  if not Found then
  begin
   FBaudRate := brUser;
   FUserBaudRate := FDCB.BaudRate;
  end;

  Found := False;
  for QDataBits := Low(QDataBits) to High(QDataBits) do
   if FDCB.ByteSize = DCB_DataBits[QDataBits] then
   begin
     Found := True;
     FDatabits := QDataBits;
     Break;
   end;
  if not Found then FDatabits := db8;

  Found := False;
  for QParity := Low(QParity) to High(QParity) do
   if FDCB.Parity = DCB_Parity[QParity] then
   begin
     Found := True;
     FParity := QParity;
     Break;
   end;
  if not Found then FParity := paNone;

  Found := False;
  for QStopBits := Low(QStopBits) to High(QStopBits) do
   if FDCB.StopBits = DCB_StopBits[QStopBits] then
   begin
     Found := True;
     FStopbits := QStopBits;
     Break;
   end;
  if not Found then FStopbits := sbOne;

  Found := False;
  for QFlowControl := High(QFlowControl) downto Low(QFlowControl) do
    if FDCB.Flags and DCB_FlowControl[QFlowControl] =
DCB_FlowControl[QFlowControl] then
    begin
      Found := True;
      FFlowControl := QFlowControl;
```

```
      Break;
    end;
  if not Found then FFlowControl := fwNone;

  FOptions := [];
  for QOptions := Low(QOptions) to High(QOptions) do
    if FDCB.Flags and DCB_ComOptions[QOptions] <> 0 then
      Include(FOptions, QOptions);
  FXOnChar := FDCB.XonChar;
  FXOffChar := FDCB.XoffChar;
  FXOnLim := FDCB.XonLim;
  FXOffLim := FDCB.XoffLim;

  UpdateDCB;
end;

procedure TAfCustomSerialPort.Set_DTR(const Value: Boolean);
const
  ESC_DTR: array[Boolean] of DWORD = (CLRDTR, SETDTR);
begin
  if FDTR <> Value then
  begin
    if Assigned(FCoreComPort) then FCoreComPort.EscapeComm(ESC_DTR[Value]);
    FDTR := Value;
  end;
end;

procedure TAfCustomSerialPort.SetEventThreadPriority(const Value: TThreadPriority);
begin
  if FEventThreadPriority <> Value then
  begin
    FEventThreadPriority := Value;
  end;
end;

procedure TAfCustomSerialPort.SetFlowControl(const Value: TAfFlowControl);
begin
  if (FFlowControl <> Value) then
  begin
    FFlowControl := Value;
    UpdateOnOffLimit;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.SetInBufSize(const Value: Integer);
```

```
    begin
  if FInBufSize <> Value then
  begin
    CheckClose;
    FInBufSize := Value;
    UpdateOnOffLimit;
  end;
end;

procedure TAfCustomSerialPort.SetOptions(const Value: TAfComOptions);
begin
  if FOptions <> Value then
  begin
    FOptions := Value;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.SetOutBufSize(const Value: Integer);
begin
  if FOutBufSize <> Value then
  begin
    CheckClose;
    FOutBufSize := Value;
  end;
end;

procedure TAfCustomSerialPort.SetParity(const Value: TAfParity);
begin
  if FParity <> Value then
  begin
    FParity := Value;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.Set_RTS(const Value: Boolean);
const
  ESC_RTS: array[Boolean] of DWORD = (CLRRTS, SETRTS);
begin
  if (FRTS <> Value) then
  begin
    if Assigned(FCoreComPort) then FCoreComPort.EscapeComm(ESC_RTS[Value]);
    FRTS := Value;
  end;
end;
```

```
  procedure TAfCustomSerialPort.SetStopbits(const Value: TAfStopbits);
begin
  if FStopbits <> Value then
  begin
    FStopbits := Value;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.SetUserBaudRate(const Value: Integer);
begin
  if FUserBaudRate <> Value then
  begin
    FUserBaudRate := Value;
    FBaudRate := brUser;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.SetWriteThreadPriority(const Value: TThreadPriority);
begin
  if FWriteThreadPriority <> Value then
  begin
    FWriteThreadPriority := Value;
  end;
end;

procedure TAfCustomSerialPort.SetXOffChar(const Value: Char);
begin
  if FXOffChar <> Value then
  begin
    FXOffChar := Value;
    UpdateDCB;
  end;
end;

procedure TAfCustomSerialPort.SetXOnChar(const Value: Char);
begin
  if FXOnChar <> Value then
  begin
    FXOnChar := Value;
    UpdateDCB;
  end;
end;
```

```
  p procedure TAfCustomSerialPort.SetXOffLim(const Value: Word);
begin
  if FXOffLim <> Value then
  begin
    FXOffLim := Value;
    FXOnLim := FInBufSize - Value;
  end;
end;

procedure TAfCustomSerialPort.SetXOnLim(const Value: Word);
begin
  if FXOnLim <> Value then
  begin
    FXOnLim := Value;
    FXOffLim := FInBufSize - Value;
  end;
end;

function TAfCustomSerialPort.SynchronizeEvent(EventKind: TAfComPortEventKind;
  Data: TAfComPortEventData; Timeout: Integer): Boolean;
begin
  Sync_Event := EventKind;
  Sync_Data := Data;
  Result := AfSyncEvent(FSyncID, Timeout);
  if (not Result) then
    Abort; // object was destroyed during sync event, get out from here
end;

procedure TAfCustomSerialPort.UpdateDCB;
var
  ComOpt: TAfComOption;
begin
  if not (csDesigning in ComponentState) then
  begin
    ZeroMemory(@FDCB, Sizeof(FDCB));
    with FDCB do
    begin
      DCBlength := Sizeof(TDCB);
      if FBaudRate = brUser then
        BaudRate := FUserBaudRate
      else
        BaudRate := DCB_BaudRates[FBaudRate];
      ByteSize := DCB_Databits[FDatabits];
      Parity := DCB_Parity[FParity];
      Stopbits := DCB_Stopbits[FStopbits];
      XonChar := FXOnChar;
```

```
  XoffChar := FXOffChar;
     XonLim := FXOnLim;
     XoffLim := FXOffLim;
     Flags := DCB_FlowControl[FFlowControl] or fBinary;
     for ComOpt := Low(TAfComOption) to High(TAfComOption) do
       if ComOpt in FOptions then Flags := Flags or DCB_ComOptions[ComOpt];
     if FDTR and (FFlowControl <> fwDtrDsr) then
       Flags := Flags or fDtrControlEnable;
     if FRTS and (FFlowControl <> fwRtsCts) then
       Flags := Flags or fRtsControlEnable;
    end;
    if Active then
    try
      FCoreComPort.DCB := FDCB;
    except
      FDCB := FCoreComPort.DCB;
      raise;
    end;
  end;
end;

procedure TAfCustomSerialPort.UpdateOnOffLimit;
begin
  if FFlowControl = fwNone then
  begin
    FXOnLim := 0;
    FXOffLim := 0;
  end else
  begin
    FXOnLim := FInBufSize div 4;
    FXOffLim := FInBufSize - FXOnLim;
  end;
end;

procedure TAfCustomSerialPort.WriteChar(C: Char);
begin
  WriteData(C, 1);
end;

procedure TAfCustomSerialPort.WriteData(const Data; Size: Integer);
begin
  if (not FClosing) and not FCoreComPort.WriteData(Data, Size) then
    RaiseError(Format(sWriteError, [Size, OutBufFree]));
end;

procedure TAfCustomSerialPort.WriteString(const S: String);
```

```
 begin
  if Length(S) > 0 then WriteData(Pointer(S)^, Length(S));
end;

{ TAfCustomComPort }

function TAfCustomComPort.ExecuteConfigDialog: Boolean;
var
  CommConfig: TCommConfig;
  BufSize: DWORD;
  Res: Boolean;
begin
  Result := False;
  ZeroMemory(@CommConfig, Sizeof(CommConfig));
  if Active then
    Res := GetCommConfig(Handle, CommConfig, BufSize) else
      Res := GetDefaultCommConfig(PChar(GetDeviceName), CommConfig, BufSize);
  CommConfig.dcb := FDCB;
  CommConfig.dwSize := Sizeof(CommConfig);
  if Res then
    Result := CommConfigDialog(PChar(GetDeviceName), Application.Handle,
CommConfig);
  if Result then
    SetDCB(CommConfig.dcb);
end;

function TAfCustomComPort.GetDeviceName: String;
begin
  Result := Format('COM%d', [FComNumber]);
end;

procedure TAfCustomComPort.InternalOpen;
begin
  Screen.Cursor := crHourGlass;
  try
    FCoreComPort.OpenComPort(FComNumber);
  finally
    Screen.Cursor := crDefault;
  end;
end;

procedure TAfCustomComPort.SetComNumber(const Value: Word);
begin
  if FComNumber <> Value then
  begin
    if Active then
```

```
  begin
     Close;
     FComNumber := Value;
     Open;
    end else
     FComNumber := Value;
  end;
end;

procedure TAfCustomComPort.SetDefaultParameters;
var
  CommConfig: TCommConfig;
  BufSize: DWORD;
begin
  ZeroMemory(@CommConfig, Sizeof(CommConfig));
  CommConfig.dwSize := Sizeof(CommConfig);
  if GetDefaultCommConfig(PChar(GetDeviceName), CommConfig, BufSize) then
    SetDCB(CommConfig.dcb);
end;

function TAfCustomComPort.SettingsStr: String;
const
  ParityStr: array[TAfParity] of Char = ('N', 'O', 'E', 'M', 'S');
  StopbitStr: array[TAfStopbits] of String = ('1', '1.5', '2');
begin
  Result := Format('COM%d: %d,%s,%s,%s', [FComNumber, GetNumericBaudrate,
    ParityStr[FParity], Chr(Ord(FDatabits) + 4 + 48), StopbitStr[FStopbits]]);
end;

end.
```

LAMPIRAN C : DATASHEET KOMPONEN

Standard Test Method for TENSILE PROPERTIES OF PLASTICS[1]

This standard is issued under the fixed designation D 638; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last approval.

This method has been approved for use by agencies of the Department of Defense and for listing in the DoD Index of Specifications and Standards.

[1] NOTE—Paragraph 5.3 and Figure 1 were editorially corrected in August 1980.

1. Scope

1.1 This method covers the determination of the tensile properties of plastics in the form of standard dumbbell-shaped test specimens when tested under defined conditions of pretreatment, temperature, humidity, and testing machine speed.

1.2 This method can be used for testing materials of any thickness up to 14 mm (0.55 in.). However, for testing specimens in the form of thin sheeting, including film less than 1.0 mm (0.04 in. in thickness) ASTM Method D 882, Test for Tensile Properties of Thin Plastic Sheeting,[2] is the preferred method. Materials with a thickness greater than 14 mm (0.55 in.) must be reduced by machining.

1.3 The values stated in SI units are to be regarded as the standard.

NOTE 1—This method is not intended to cover precise physical procedures. It is recognized that the constant-rate-of-crosshead-movement type of test leaves much to be desired from a theoretical standpoint, that wide differences may exist between rate of crosshead movement and rate of strain between gage marks on the specimen, and that the testing speeds specified disguise important effects characteristic of materials in the plastic state. Further, it is realized that variations in the thicknesses of test specimens, which are permitted by these procedures, produce variations in the surface-volume ratios of such specimens, and that these variations may influence the test results. Hence, where directly comparable results are desired, all samples should be of equal thickness. Special additional tests should be used where more precise physical data are needed.

NOTE 2—This method may be used for testing phenolic molded resin or laminated materials. However, where these materials are used as electrical insulation, such materials should be tested in accordance with ASTM Method D 229, Testing Rigid Sheet and Plate Materials Used for Electrical Insulation,[2] and ASTM Method D 651, Test for Tensile Strength of Molded Electrical Insulating Materials.[3]

2. Applicable Documents

2.1 *ASTM Standards:*

D 618 Conditioning Plastics and Electrical Insulating Materials for Testing[2]

D 883 Definitions of Terms Relating to Plastics[4]

E 4 Load Verification of Testing Machines[5]

E 83 Verification and Classification of Extensometers[6]

3. Significance

3.1 This method is designed to produce tensile property data for the control and specification of plastic materials. These data are also useful for qualitative characterization and for research and development.

3.2 Tensile properties may vary with specimen preparation and with speed and environment of testing. Consequently, where precise comparative results are desired, these factors must be carefully controlled.

3.2.1 It is realized that a material cannot be tested without also testing the method of preparation of that material. Hence, when comparative tests of materials per se are desired, the greatest care must be exercised to ensure that all samples are prepared in exactly the same way, unless the test is to include the

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[1] This method is under the jurisdiction of ASTM Committee D-20 on Plastics and is the direct responsibility of Subcommittee D 20.10 on Mechanical Properties.

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[2] *Annual Book of ASTM Standards*, Part 35.

[3] *Annual Book of ASTM Standards*, Part 39.

[4] *Annual Book of ASTM Standards*, Parts 34, 35, and 36.

[5] *Annual Book of ASTM Standards*, Parts 10, 14, 32, 35, and 41.

[6] *Annual Book of ASTM Standards*, Parts 10 and 41.

effects of sample preparation. Similarly, for referee purposes or comparisons within any given series of specimens, care must be taken to secure the maximum degree of uniformity in details of preparation, treatment, and handling.

3.3 Tensile properties may provide useful data for plastics engineering design purposes. However, because of the high degree of sensitivity exhibited by many plastics to rate of straining and environmental conditions, data obtained by this method cannot be considered valid for applications involving load-time scales or environments widely different from those of this method. In cases of such dissimilarity, no reliable estimation of the limit of usefulness can be made for most plastics. This sensitivity to rate of straining and environment necessitates testing over a broad load-time scale (including impact and creep) and range of environmental conditions if tensile properties are to suffice for engineering design purposes.

NOTE 3—Since the existence of a true elastic limit in plastics (as in many other organic materials and in many metals) is debatable, the propriety of applying the term "elastic modulus" in its quoted generally accepted definition to describe the "stiffness" or "rigidity" of a plastic has been seriously questioned. The exact stress-strain characteristics of plastic materials are highly dependent on such factors as rate of application of stress, temperature, previous history of specimen, etc. However, stress-strain curves for plastics, determined as described in this method, almost always show a linear region at low stresses, and a straight line drawn tangent to this portion of the curve permits calculation of an elastic modulus of the usually defined type. Such a constant is useful if its arbitrary nature and dependence on time, temperature, and similar factors are realized.

4. Definitions

4.1 Definitions of terms applying to this method appear in Definitions D 883 and Annex A1.

5. Apparatus

5.1 *Testing Machine*—A testing machine of the constant-rate-of-crosshead-movement type and comprising essentially the following:

5.1.1 *Fixed Member*—A fixed or essentially stationary member carrying one grip.

5.1.2 *Movable Member*—A movable member carrying a second grip.

5.1.3 *Grips*—Grips for holding the test specimen between the fixed member and the movable member. The grips shall be self-aligning, that is, they shall be attached to the fixed and movable member, respectively, in such a manner that they will move freely into alignment as soon as any load is applied, so that the long axis of the test specimen will coincide with the direction of the applied pull through the center line of the grip assembly. The specimens should be aligned as perfectly as possible with the direction of pull so that no rotary motion that may induce slippage will occur in the grips; there is a limit to the amount of misalignment self-aligning. grips will accommodate.

5.1.3.1 The test specimen shall be held in such a way that slippage relative to the grips is prevented insofar as possible. Grip surfaces that are deeply scored or serrated with a pattern similar to those of a coarse single-cut file, serrations about 2.4 mm (3/32 in.) apart and about 1.6 mm (1/16 in.) deep, have been found satisfactory for most thermoplastics. Finer serrations have been found to be more satisfactory for harder plastics such as the thermosetting materials. The serrations should be kept clean and sharp. Breaking in the grips may occur at times, even when deep serrations or abraded specimen surfaces are used; other techniques must be used in these cases. Other techniques that have been found useful, particularly with smooth-faced grips, are abrading that portion of the surface of the specimen that will be in the grips, and interposing thin pieces of abrasive cloth, abrasive paper, or plastic or rubber-coated fabric, commonly called hospital sheeting, between the specimen and the grip surface. No. 80 double-sided abrasive paper has been found effective in many cases. An open-mesh fabric, in which the threads are coated with abrasive, has also been effective. Reducing the cross-sectional area of the specimen may also be effective. The use of special types of grips is sometimes necessary to eliminate slippage and breakage in the grips.

5.1.4 *Drive Mechanism*—A drive mechanism for imparting to the movable member a uniform, controlled velocity with respect to the stationary member, this velocity to be regulated as specificed in Section 9.

5.1.5 *Load Indicator*—A suitable load-indicating mechanism capable of showing the total tensile load carried by the test specimen

when held by the grips. This mechanism shall be essentially free of inertia lag at the specified rate of testing and shall indicate the load with an accuracy of ±1 % of the indicated value, or better. The accuracy of the testing machine shall be verified in accordance with Method E 4.

NOTE 4 - Experience has shown that many testing machines now in use are incapable of maintaining accuracy for as long as the periods between inspection recommended in Methods E 4. Hence, it is recommended that each machine be studied individually and verified as often as may be found necessary. It frequently will be necessary to perform this function daily.

5.1.6 The fixed member, movable member, drive mechanism, and grips shall be constructed of such materials and in such proportions that the total elastic longitudinal strain of the system constituted by these parts does not exceed 1 % of the total longitudinal strain between the two gage marks on the test specimen at any time during the test and at any load up to the rated capacity of the machine.

5.2 *Extension Indicator* — A suitable instrument for determining the distance between two designated points located within the gage length of the test specimen as the specimen is stretched. It is desirable, but not essential, that this instrument automatically record this distance (or any change in it) as a function of the load on the test specimen or of the elapsed time from the start of the test, or both. If only the latter is obtained, load-time data must also be taken. This instrument shall be essentially free of inertia lag at the specified speed of testing and shall be accurate to ±1 % of strain or better.

NOTE 5—Reference is made to Method E 83.

5.3 *Micrometers*—Suitable micrometers, reading to at least 0.025 ± *0.000 mm* (0.001 ± *0.000 in.*), for measuring the width and thickness of the test specimens. The thickness of nonrigid plastics should be measured with a dial micrometer that exerts a pressure of 24.5 ± 4.5 kPa (3.6 ± 0.7 psi) on the specimen and measures the thickness to within 0.025 mm (0.001 in.). The anvil of the micrometer shall be at least 36 mm (1.4 in.) in diameter and parallel to the face of the contact foot.

6. Test Specimens

6.1 *Sheet, Plate, and Molded Plastics:*

6.1.1 *Rigid and Semirigid Plastics* — The test specimen shall conform to the dimensions shown in Fig. 1. The Type I specimen is the preferred specimen and shall be used where sufficient material having a thickness of 7 mm (0.28 in.) or less is available. The Type II specimen may be used when a material does not break in the narrow section with the preferred Type I specimen. The Type V specimen shall be used where only limited material having a thickness of 7 mm (0.28 in.) or less is available for evaluation, or where a large number of specimens are to be exposed in a limited space (thermal and environmental stability tests, etc.). The Type IV specimen should be used when direct comparisons are required between materials in different rigidity cases (that is, nonrigid and semirigid). The Type III specimen must be used for all materials with a thickness of greater than 7 mm (0.28 in.) but not more than 14 mm (0.55 in.).

6.1.2 *Nonrigid Plastics* — The test specimen shall conform to the dimensions shown in Fig. 1. The Type IV specimen shall be used for testing nonrigid plastics with a thickness of 7 mm (0.28 in.) or less. The Type III specimen must be used for all materials with a thickness greater than 7 mm (0.28 in.) but not more than 14 mm (0.55 in.).

6.1.3 *Preparation* — Test specimens shall be prepared by machining operations, or die cutting, from materials in sheet, plate, slab, or similar form. Materials thicker than 14 mm (0.55 in.) must be machined to 14 mm (0.55 in.) for use as Type III specimens. Specimens can also be prepared by molding the material to be tested.

NOTE 6—Specimens prepared by injection molding may have different tensile properties than specimens prepared by machining or die-cutting because of the orientation induced. This effect may be more pronounced in specimens with narrow sections.

6.2 The test specimen for rigid tubes shall be as shown in Fig. 2. The length, *L*, shall be as shown in the table in Fig. 2. A groove shall be machined around the outside of the specimen at the center of its length so that the wall section after machining shall be 60 % of the original nominal wall thickness. This groove shall consist of a straight section 57.2 mm (2¼ in.) in length with a radius of 76 mm (3) at each end joining it to the outside diam-

eter. Steel or brass plugs having diameters such that they will fit snugly inside the tube and having a length equal to the full jaw length plus 25 mm (1 in.) shall be placed in the ends of the specimens to prevent crushing. They can be located conveniently in the tube by separating and supporting them on a threaded metal rod. Details of plugs and test assembly are shown in Fig. 2.

6.3 The test specimen for rigid rods shall be as shown in Fig. 3. The length, *L*, shall be as shown in the table in Fig. 3. A groove shall be machined around the specimen at the center of its length so that the diameter of the machined portion shall be 60 % of the original nominal diameter. This groove shall consist of a straight section 57.2 mm (2¼ in.) in length with a radius of 76 mm (3 in.) at each end joining it to the outside diameter.

6.4 All surfaces of the specimen shall be free of visible flaws, scratches, or imperfections. Marks left by coarse machining operations shall be carefully removed with a fine file or abrasive, and the filed surfaces shall then be smoothed with abrasive paper (No. 00 or finer). The finishing sanding strokes shall be made in a direction parallel to the long axis of the test specimen. All flash shall be removed from a molded specimen, taking great care not to disturb the molded surfaces. In machining a specimen, undercuts that would exceed the dimensional tolerances shown in Fig. 1 shall be scrupulously avoided. Care shall also be taken to avoid other common machining errors.

6.5 If it is necessary to place gage marks on the specimen, this shall be done with a wax crayon or India ink that will not affect the material being tested. Gage marks shall not be scratched, punched, or impressed on the specimen.

6.6 When testing materials that are suspected of anisotropy, duplicate sets of test specimens shall be prepared, having their long axes respectively parallel with, and normal to, the suspected direction of anisotropy.

7. Conditioning

7.1 *Conditioning*—Condition the test imens at 23 ± 2°C (73.4 ± 3.6°F) and 5 % relative humidity for not less than prior to test in accordance with Procedure A of Methods D 618 for those tests where conditioning is required. In cases of disagreement, the tolerances shall be ±1°C (1.8°F) and ±2 % relative humidity.

7.2 *Test Conditions*—Conduct tests in the Standard Laboratory Atmosphere of 23 ± 2°C (73.4 ± 3.6°F) and 50 ± 5 % relative humidity, unless otherwise specified in the test methods. In cases of disagreements, the tolerances shall be ±1°C (1.8°F) and ±2 % relative humidity.

7.3 The tensile properties of some plastics change rapidly with small changes in temperature. Since heat may be generated as a result of straining the specimen at high rates, conduct tests without forced cooling to ensure uniformity of test conditions. Measure the temperature in the reduced section of the specimen and record it for materials where self-heating is suspected.

8. Number of Test Specimens

8.1 Test at least five specimens for each sample in the case of isotropic materials.

8.2 Test ten specimens, five normal to, and five parallel with the principal axis of anisotropy, for each sample in the case of anisotropic materials.

8.3 Discard specimens that break at some obvious fortuitous flaw, or that do not break between the predetermined gage marks, and make retests, unless such flaws constitute a variable to be studied.

NOTE 7—Before testing, all transparent specimens should be inspected in a polariscope. Those which show atypical or concentrated strain patterns should be rejected, unless the effects of these residual strains constitute a variable to be studied.

9. Speed of Testing

9.1 Speed of testing shall be the relative rate of motion of the grips or test fixtures during the test. Rate of motion of the driven grip or fixture when the testing machine is running idle may be used, if it can be shown that the resulting speed of testing is within the limits of variation allowed.

9.2 Choose the speed of testing from Table 1. Determine this chosen speed of testing by the specification for the material being tested, or by agreement between those concerned. When the speed is not specified, use the lowest speed shown in Table 1 for the specimen

geometry being used, which gives rupture within ½ to 5 min testing time.

9.3 Modulus determinations may be made at the speed selected for the other tensile properties when the recorder response and resolution are adequate.

10. Procedure

10.1 Measure the width and thickness of rigid flat specimens (Fig. 1) with a suitable micrometer to the nearest 0.025 mm (0.001 in.) at several points along their narrow sections. Measure the thickness of nonrigid specimens (produced by a Type IV die) in the same manner with the required dial micrometer. Take the width of this specimen as the distance between the cutting edges of the die in the narrow section. Measure the diameter of rod specimens, and the inside and outside diameters of tube specimens, to the nearest 0.025 mm (0.001 in.) at a minimum of two points 90 deg apart; make these measurements along the groove for specimens so constructed. Use plugs in testing tube specimens, as shown in Fig. 2.

10.2 Place the specimen in the grips of the testing machine, taking care to align the long axis of the specimen and the grips with an imaginary line joining the points of attachment of the grips to the machine. The distance between the ends of the gripping surfaces, when using flat specimens, shall be as indicated in Fig. 1. On tube and rod specimens, the location for the grips shall be as shown in Fig. 2 and 3. Tighten the grips evenly and firmly to the degree necessary to prevent slippage of the specimen during the test, but not to the point where the specimen would be crushed.

10.3 Attach the extension indicator.

10.4 Set the speed of testing at the proper rate as required in Section 9, and start the machine.

10.5 Record the load-extension curve of the specimen.

10.6 Record the load and extension at the yield point (if one exists) and the load and extension at the moment of rupture.

NOTE 8—If it is desired to measure both ... lus and failure properties (yield or break, or it may be necessary, in the case of highly ext materials to run two independent tests. Th magnification extensometer normally used to determine properties up to the yield point may not be suitable for tests involving high extensibility. If allowed to remain attached to the specimen, the extensometer could be permanently damaged. A broad range incremental extensometer or hand rule technique may be needed when such materials are taken to rupture.

11. Calculations

11.1 *Tensile Strength*—Calculate the tensile strength by dividing the maximum load in newtons (or pounds-force) by the original minimum cross-sectional area of the specimen in square metres (or square inches). Express the result in pascals (or pounds-force per square inch) and report it to three significant digures as "Tensile Strength at Yield" or "Tensile Strength at Break," whichever term is applicable. When a nominal yield or break load less than the maximum is present and applicable, it may be desirable also to calculate, in a similar manner, the corresponding" Tensile Stress at Yield" or "Tensile Stress at Break" and report it to three significant figures (Annex Note A1.1).

11.2 *Percent Elongation*—If the specimen gives a yield load that is larger than the load at break, calculate "Percent Elongation at Yield." Otherwise, calculate "Percent Elongation at Break." Do this by reading the extension (change in gage length) at the moment the applicable load is reached. Divide that extension by the original gage length and multiply by 100. Report "Percent Elongation at Yield" or "Percent Elongation at Break" to two significant figures. When a yield or breaking load less than the maximum is present and of interest, it is desirable to calculate and report both "Percent Elongation at Yield" and "Percent Elongation at Break" (Annex Note A1.2).

11.3 *Modulus of Elasticity*—Calculate the modulus of elasticity by extending the initial linear portion of the load-extension curve and dividing the difference in stress corresponding to any segment of section on this straight line by the corresponding difference in strain. All elastic modulus values shall be computed using the average initial cross-sectional area of the test specimens in the calculations. The result shall be expressed in pascals (or pounds-force per square inch) and reported to three significant figures.

11.4 For each series of tests, calculate the arithmetic mean of all values obtained and report it as the "average value" for the particular property in question.

11.5 Calculate the standard deviation (estimated) as follows and report it to two significant figures:

$$S = \sqrt{(\Sigma X^2 - n\bar{X}^2)/(n-1)}$$

where:

S = estimated standard deviation,
X = value of single observation,
n = number of observations, and
$\bar{X}$ = arithmetic mean of the set of observations.

11.6 See Appendix X1 for information on toe compensation.

12. Report

12.1 The report shall include the following:

12.1.1 Complete identifications of the material tested, including type, source, manufacturer's code numbers, form, principal dimensions, previous history, etc.,

12.1.2 Method of preparing test specimens,

12.1.3 Type of test specimen and dimensions,

12.1.4 Conditioning procedure used,

12.1.5 Atmospheric conditions in test room,

12.1.6 Temperature rise in specimen,

12.1.7 Number of specimens tested,

12.1.8 Speed of testing,

12.1.9 Tensile strength at yield or break, average value and standard deviation,

12.1.10 Tensile stress at yield or break, if applicable, average value and standard deviation,

12.1.11 Percentage elongation at yield or break (or both, as applicable), average value and standard deviation,

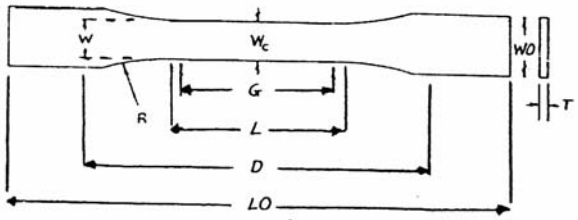
12.1.12 Modulus of elasticity, average value and standard deviation, and

12.1.13 Date of test.

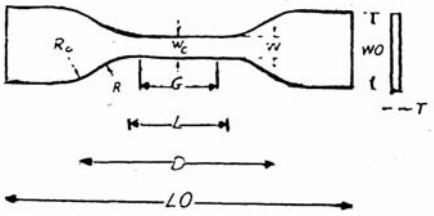
TABLE 1 Designations for Speed of Testing[A]

Classification[B]	Specimen Type	Speed of Testing, mm/min (in./min)	Nominal Strain[C] Rate at Start of Test, mm/mm·min
Rigid and Semirigid	I, II, III, Rods and Tubes	5 (0.2) ± 25 %	0.1
		50 (2) ± 10 %	1
		500 (20) ± 10 %	10
	IV	5 (0.2) ± 25 %	0.15
		50 (2) ± 10 %	1.5
		500 (20) ± 10 %	15
	V	1 (0.05) ± 25 %	0.1
		10 (0.5) ± 25 %	1
		100 (5) ± 25 %	10
Nonrigid	III	50 (2) ± 10 %	1
		500 (20) ± 10 %	10
	IV	50 (2) ± 10 %	1.5
		500 (20) ± 10 %	15

[A] Select the lowest speed that produces rupture in ½ to 5 min for the specimen geometry being used (see 9.2).
[B] See Definitions D 883 for definitions.
[C] The initial rate of straining cannot be calculated exactly for dumbbell-shaped specimens because of extension, both in the reduced section outside the gage length and in the fillets. This initial strain rate can be measured from the initial slope of the tensile strain-versus-time diagram.



TYPES I, II, III & V



TYPE IV

Specimen Dimensions for Thickness, *T*, mm[D]

Dimensions (see drawings)	7 or under		Over 7 to 14 incl.	4 or under		Tolerances
	Type I	Type II	Type III	Type IV[G]	Type V[I]	
W—Width of narrow section[A, B]	13	6	19	6	3.18	±0.5[G, I]
L—Length of narrow section	57	57	57	33	9.53	±0.5[I]
WO—Width over-all, min[E]	19	19	29	19	9.53	±6
LO—Length over-all, min[F]	165	183	246	115	63.5	no max
G—Gage length[C]	50	50	50	...	7.62	±0.25[I]
G—Gage length[C]	...	...	...	25	...	±0.13
D—Distance between grips	115	135	115	64[H]	25.4	±5
R—Radius of fillet	76	76	76	14	12.7	±1[I]
RO—Outer radius (Type IV)	...	...	...	25	...	±1

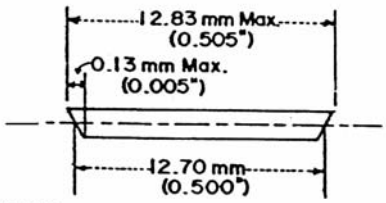
Specimen Dimensions for Thickness, *T*, in.[D]

Dimensions (see drawings)	0.28 or under		Over 0.28 to 0.55 incl.	0.16 or under		Tolerances
	Type I	Type II	Type III	Type IV[G]	Type V[I]	
W—Width of narrow section[A, B]	0.50	0.25	0.75	0.25	0.125	±0.02[G, I]
L—Length of narrow section	2.25	2.25	2.25	1.30	0.375	±0.02[I]
WO—Width over-all, min[E]	0.75	0.75	1.13	0.75	0.375	±0.25
LO—Length over-all, min[F]	6.5	7.2	9.7	4.5	2.5	no max
G—Gage length[C]	2.00	2.00	2.00	...	0.300	±0.010[I]
G—Gage length[C]	...	...	...	1.00	...	±0.005
D—Distance between grips	4.5	5.3	4.5	2.5[H]	1.0	±0.2
R—Radius of fillet	3.00	3.00	3.00	0.56	0.5	±0.04[I]
RO—Outer radius (Type IV)	...	...	...	1.00	...	±0.04

FIG. 1 Tension Test Specimens for Sheet, Plate, and Molded Plastics.

[A] The width at the center W_c shall be plus 0.00 mm, minus 0.10 mm (+0.000 in., −0.004 in.) compared with width *W* at other parts of the reduced section. Any reduction in *W* at the center shall be gradual, equally on each side so that no abrupt changes in dimension result.

[B] For molded specimens, a draft of not over 0.13 mm (0.005 in.) may be allowed for either Type I or II specimens 3.2 mm (0.13 in.) in thickness, and this should be taken into account when calculating width of the specimen. Thus a typical section of a molded Type I specimen, having the maximum allowable draft, could be as follows:



[C] Test marks or initial extensometer span.

[D] Thickness, *T*, shall be 3.2 ± 0.4 mm (0.13 ± 0.02 in.) for all types of molded specimens, and for other Types I and II specimens where possible. If specimens are machined from sheets or plates, thickness, *T*, may be the thickness of the sheet or plate provided this does not exceed the range stated for the intended specimen type. For sheets of nominal thickness greater than 14 mm (0.55 in.) the specimens shall be machined to 14 ± 0.4 mm (0.55 ± 0.02 in.) in thickness, for use with the Type III specimen. For sheets of nominal thickness between 14 and 51 mm (0.55 and 2 in.) approximately equal amounts shall be machined from each surface. For thicker sheets both surfaces of the specimen shall be machined and the location of the specimen with reference to the original thickness of the sheet, shall be noted. Tolerances on thickness less than 14 mm (0.55 in.) shall be those standard for the grade of material tested.

[E] Overall widths greater than the minimum indicated may be desirable for some materials in order to avoid breaking in the grips.

[F] Overall lengths greater than the minimum indicated may be desirable either to avoid breaking in the grips or to satisfy special test requirements.

[G] For the Type IV specimen, the internal width of the narrow section of the die shall be 6.00 ± 0.05 mm (0.250 ± 0.002 in.). The dimensions are essentially those of Die C in ASTM Method D 412, for Rubber Properties in Tension (*Annual Book of ASTM Standards*, Parts 35 and 37).

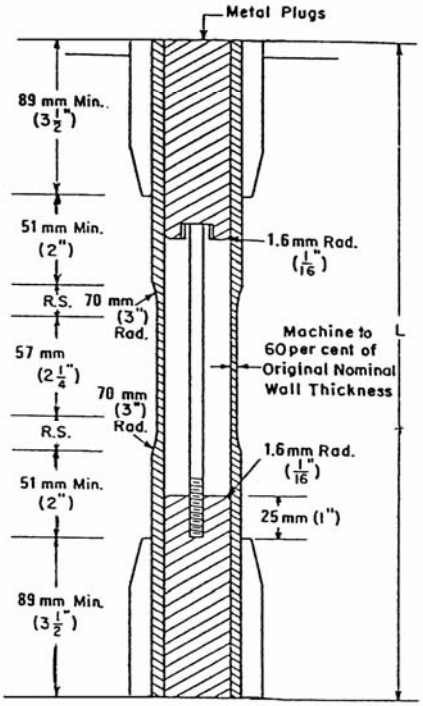
[H] When self-tightening grips are used, for highly extensible polymers, the distance between grips will depend upon the types of grips used and may not be critical if maintained uniform once chosen.

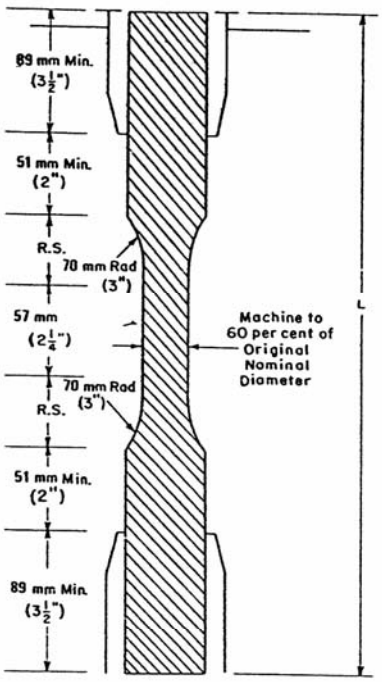
[I] The Type V specimen shall be machined or die cut to the dimensions shown, or molded in a mold whose cavity has these dimensions. The dimensions shall be:

W = 3.18 ± 0.03 mm (0.125 ± 0.001 in.),
L = 9.53 ± 0.08 mm (0.375 ± 0.003 in.),
G = 7.62 ± 0.02 mm (0.300 ± 0.001 in.), and
R = 12.7 ± 0.08 mm (0.500 ± 0.003 in.).

The other tolerances are those in the table. Supporting data on the introduction of the L specimen as the Type V specimen may be obtained from ASTM Headquarters, 1916 Race St., Philadelphia, Pa. 19103, by requesting RR:D-20-1038.

FIG. 1 *Continued.*





DIMENSIONS OF ROD SPECIMENS

Nominal Diameter	Length of Radial Sections, 2R.S.	Total Calculated Minimum Length of Specimen	Standard Length, *L*, of Specimen to be Used for 89-mm (3½-in.) Jaws[A]
mm (in.)	mm (in.)	mm (in.)	mm (in.)
3.2 (⅛)	19.6 (0.773)	356 (14.02)	381 (15)
4.7 (3/16)	24.0 (0.946)	361 (14.20)	381 (15)
6.4 (¼)	27.7 (1.091)	364 (14.34)	381 (15)
9.5 (⅜)	33.9 (1.333)	370 (14.58)	381 (15)
12.7 (½)	39.0 (1.536)	376 (14.79)	400 (15.75)
15.9 (⅝)	43.5 (1.714)	380 (14.96)	400 (15.75)
19.0 (¾)	47.6 (1.873)	384 (15.12)	400 (15.75)
22.2 (⅞)	51.5 (2.019)	388 (15.27)	400 (15.75)
25.4 (1)	54.7 (2.154)	391 (15.40)	419 (16.5)
31.8 (1¼)	60.9 (2.398)	398 (15.65)	419 (16.5)
38.1 (1½)	66.4 (2.615)	403 (15.87)	419 (16.5)
42.5 (1¾)	71.4 (2.812)	408 (16.06)	419 (16.5)
50.8 (2)	76.0 (2.993)	412 (16.24)	432 (17)

[A] For other jaws greater than 89 mm (3½ in.), the standard length shall be increased by twice the length of the jaws minus 178 mm (7 in.). The standard length permits a slippage of approximately 6.4 to 12.7 mm (¼ to ½ in.) in each jaw while maintaining maximum length of jaw grip.

FIG. 3 Diagram Showing Location of Rod Tension Test Specimen in Testing Machine.

DIMENSIONS OF TUBE SPECIMENS

Nominal Wall Thickness	Length of Radial Sections, 2R.S.	Total Calculated Minimum Length of Specimen	Standard Length, *L*, of Specimen to be Used for 89-mm (3½-in.) Jaws[A]
mm(in.)	mm(in.)	mm(in.)	mm(in.)
0.79(1/32)	13.9(0.547)	350(13.80)	381(15)
1.2(3/64)	17.0(0.670)	354(13.92)	381(15)
1.6(1/16)	19.6(0.773)	356(14.02)	381(15)
2.4(3/32)	24.0(0.946)	361(14.20)	381(15)
3.2(⅛)	27.7(1.091)	364(14.34)	381(15)
4.8(3/16)	33.9(1.333)	370(14.58)	381(15)
6.4(¼)	39.0(1.536)	376(14.79)	400(15.75)
7.9(5/16)	43.5(1.714)	380(14.96)	400(15.75)
9.5(⅜)	47.6(1.873)	384(15.12)	400(15.75)
11.1(7/16)	51.3(2.019)	388(15.27)	400(15.75)
12.7(½)	54.7(2.154)	391(15.40)	419(16.5)

[A] For other jaws greater than 89 mm (3½ in.), the standard length shall be increased by twice the length of the jaws minus 178 mm (7 in.). The standard length permits a slippage of approximately 6.4 to 12.7 mm (¼ to ½ in.) in each jaw while maintaining maximum length of jaw grip.

FIG. 2 Diagram Showing Location of Tube Tension Test Specimens in Testing Machine.

Features

- **Compatible with MCS-51™ Products**
- **4K Bytes of In-System Reprogrammable Flash Memory**
  - **Endurance: 1,000 Write/Erase Cycles**
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Three-Level Program Memory Lock**
- **128 x 8-Bit Internal RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial Channel**
- **Low Power Idle and Power Down Modes**

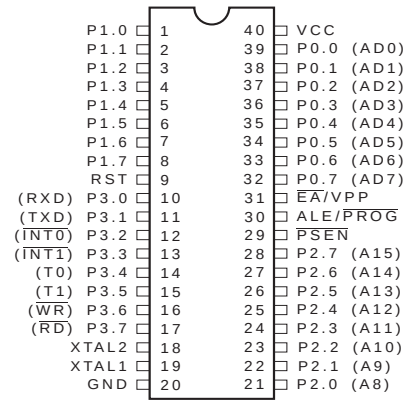
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

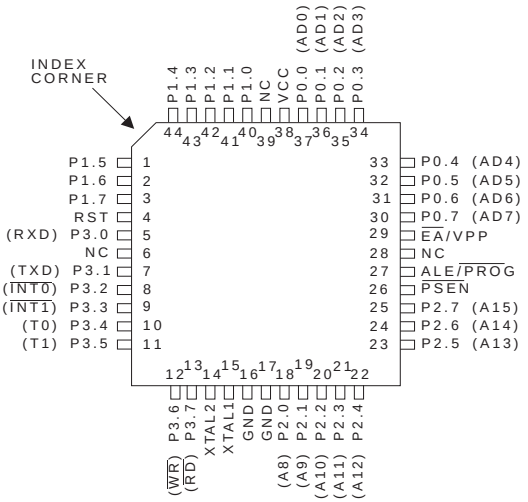
(continued)

Pin Configurations

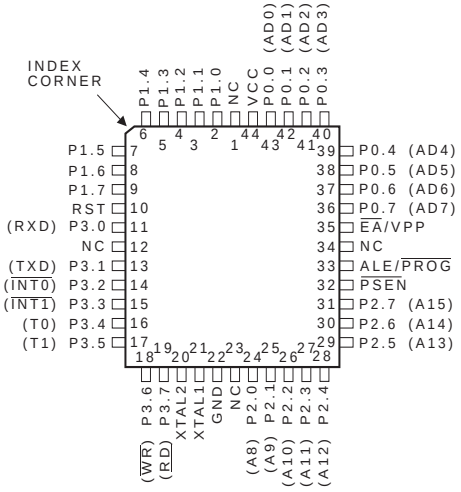
PDIP



PQFP/TQFP



PLCC

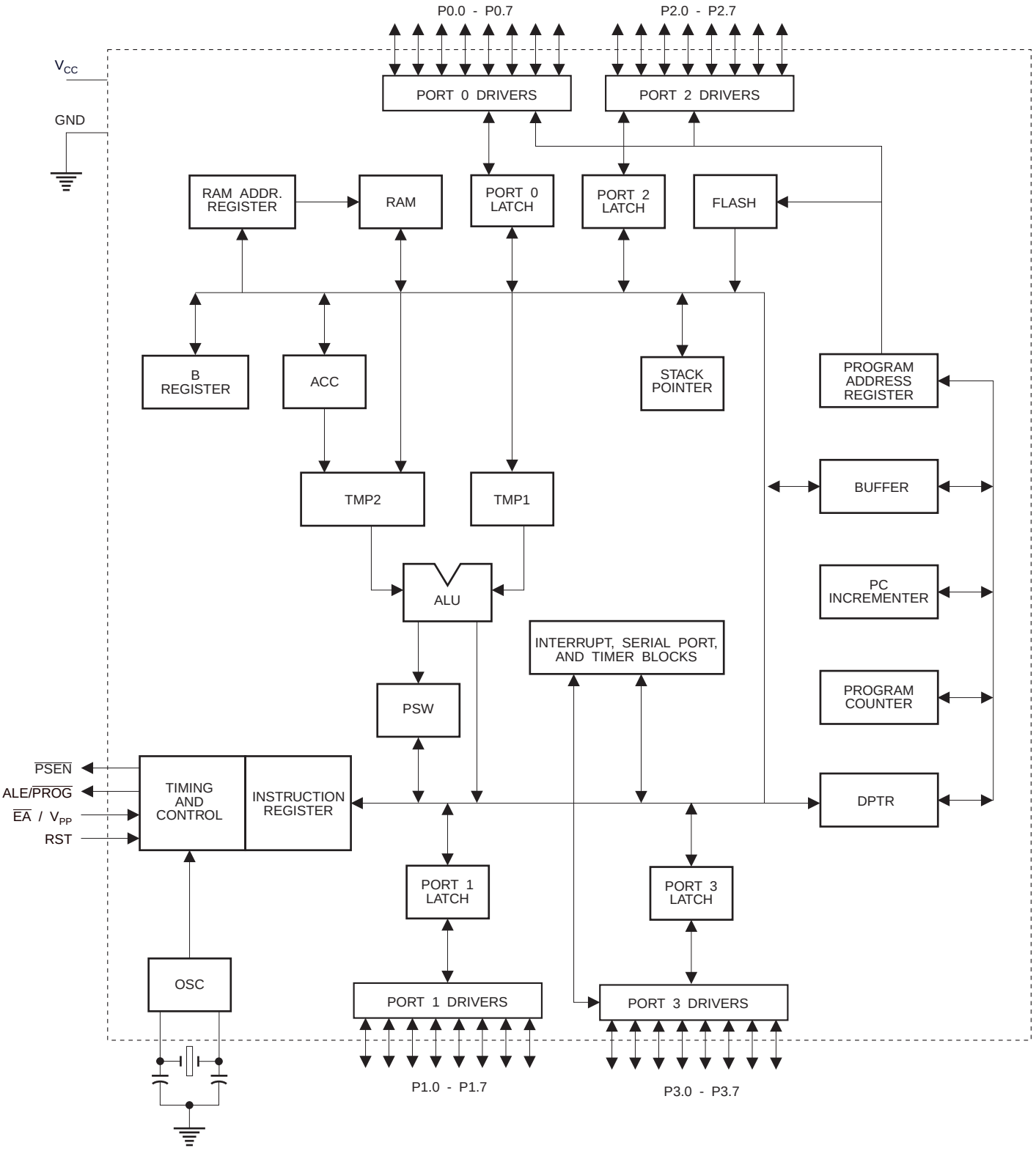


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A–12/97

Block Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}
External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP}.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Oscillator Characteristics

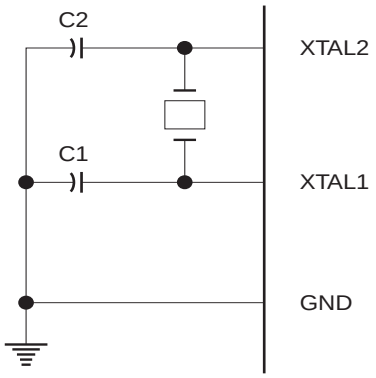
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

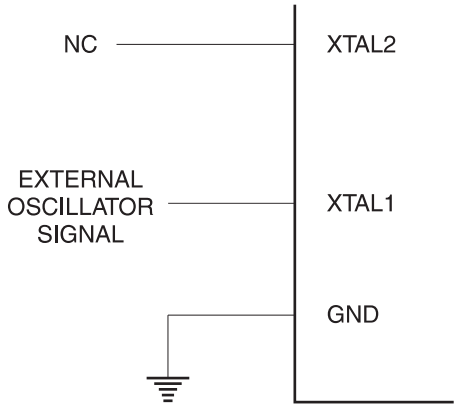
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

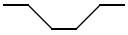
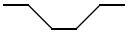
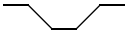
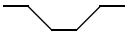
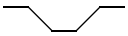
(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms $\overline{PROG}$ pulse.

Figure 3. Programming the Flash

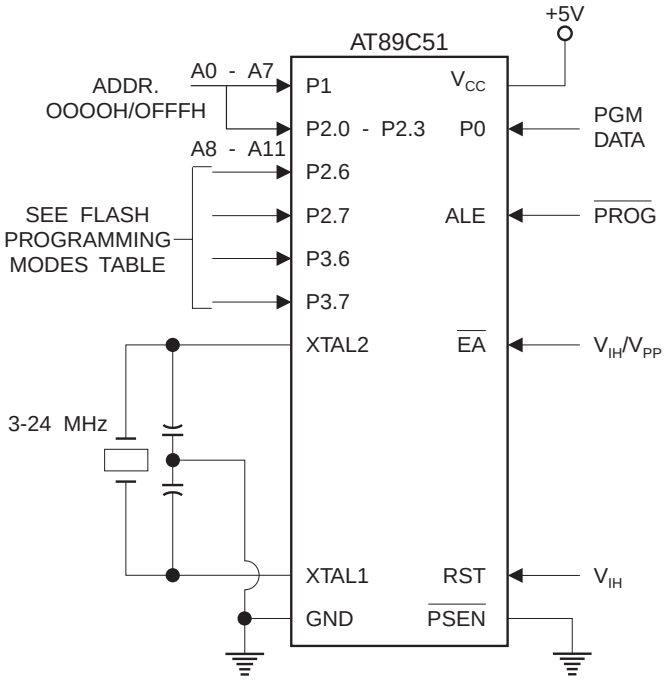
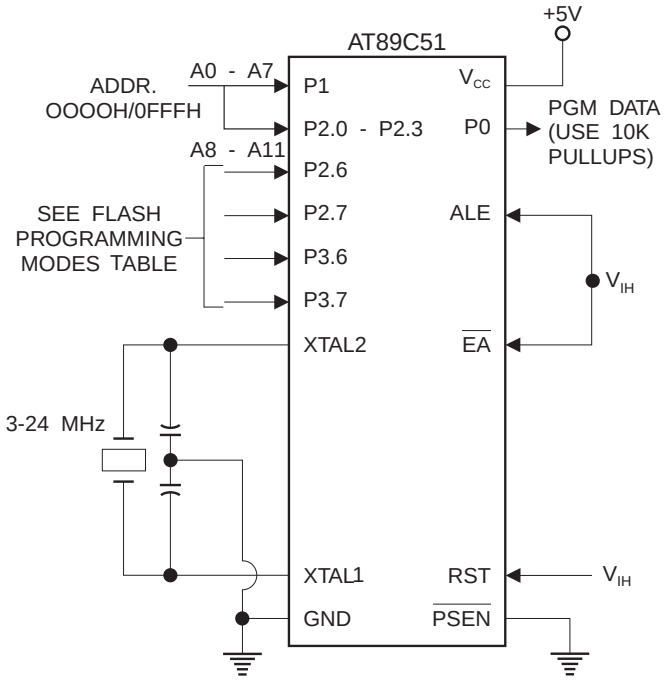


Figure 4. Verifying the Flash



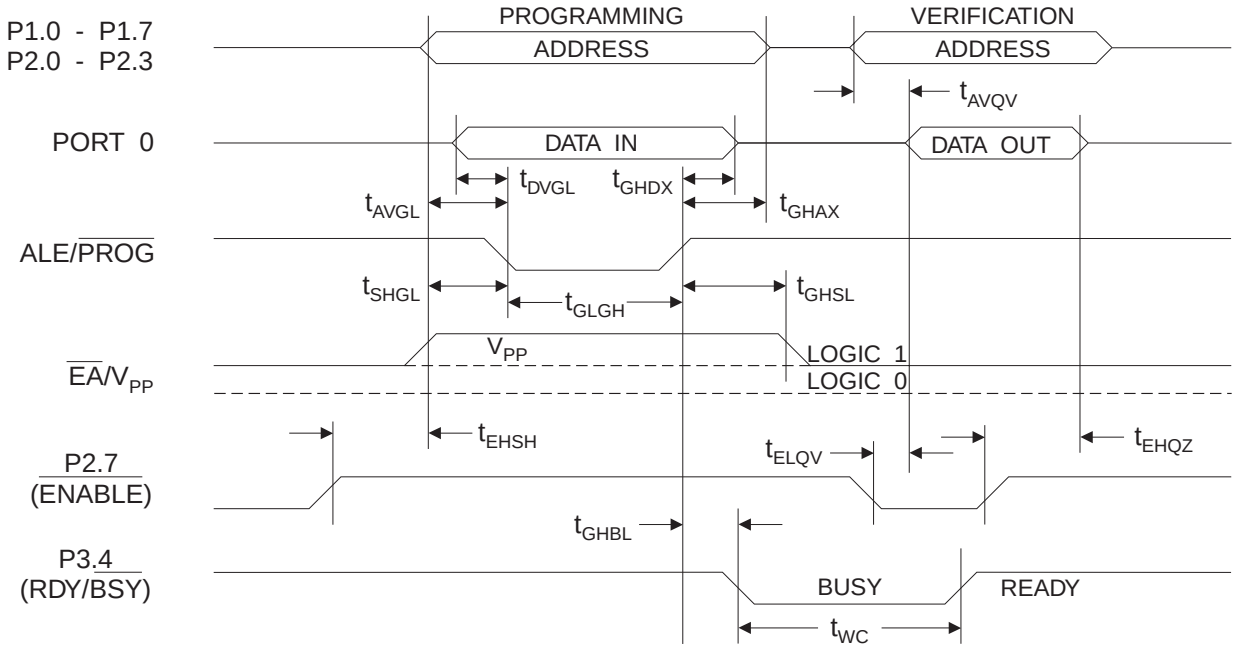
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

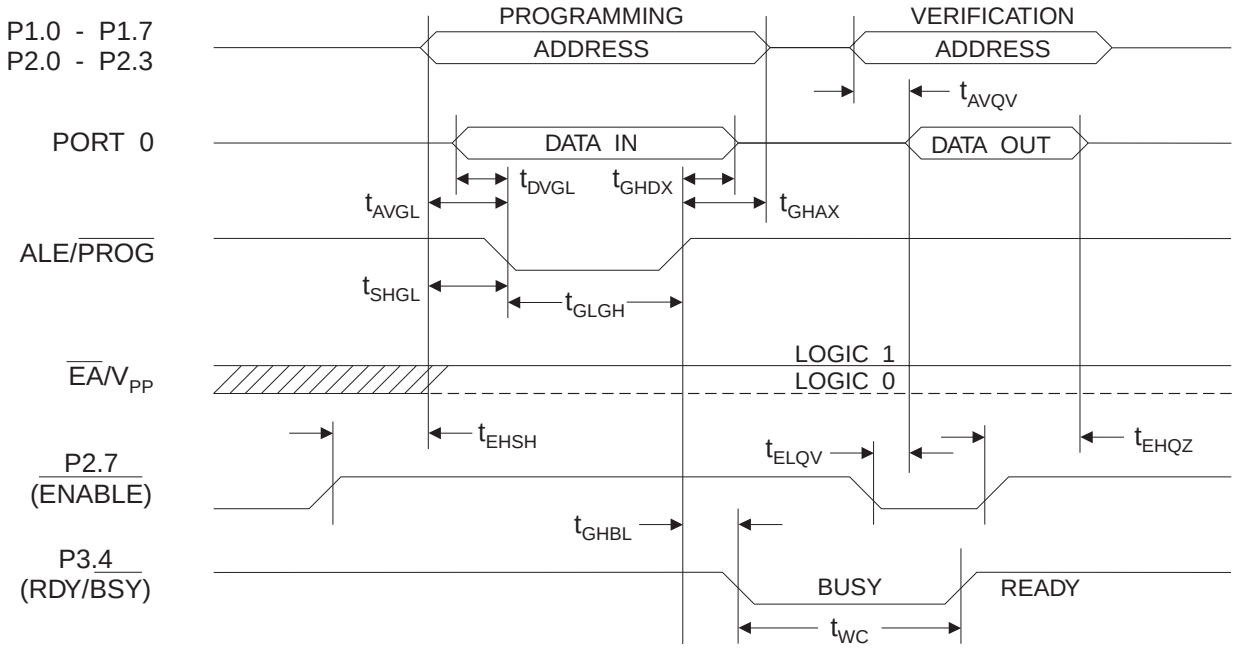
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

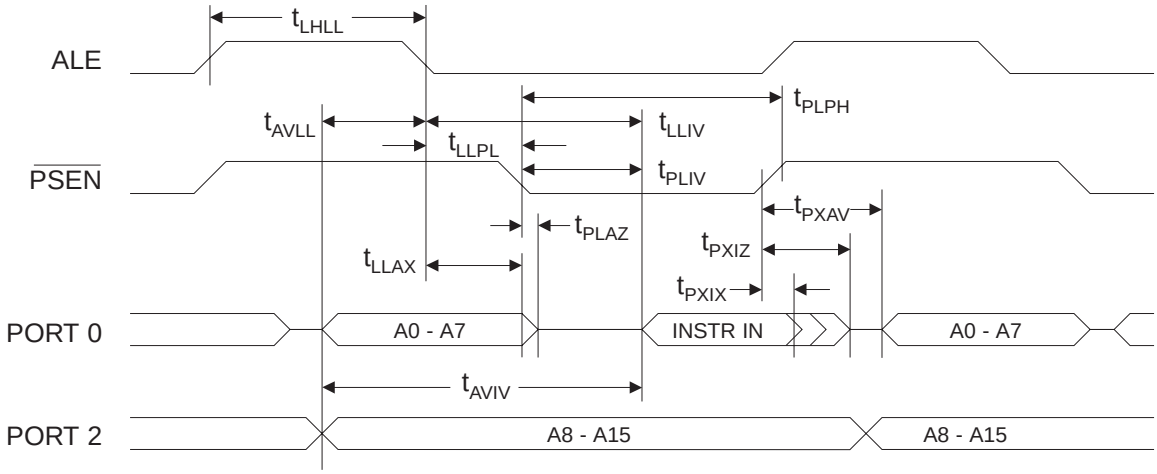
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

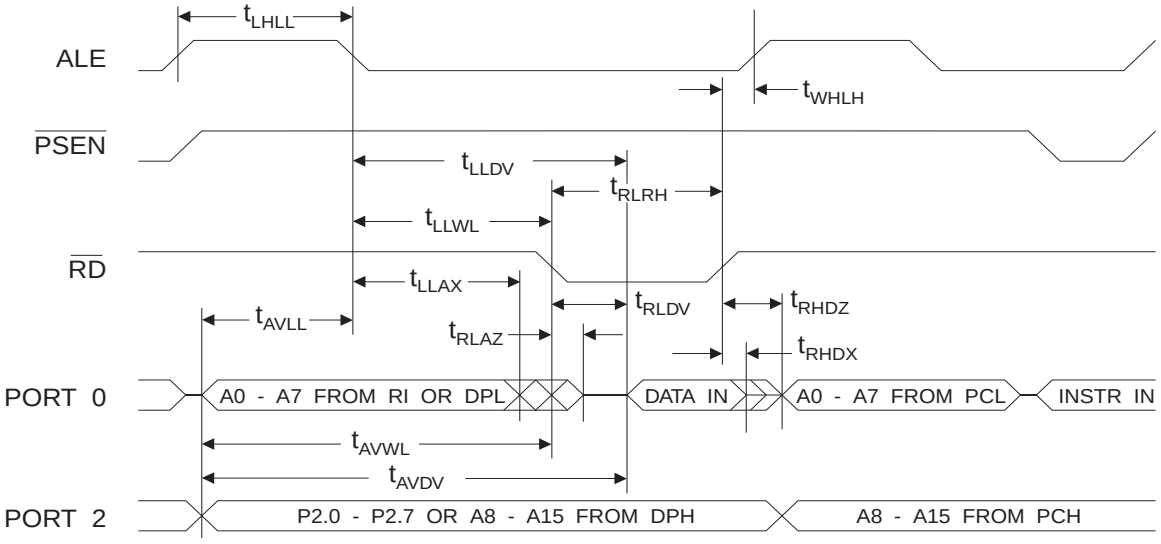
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

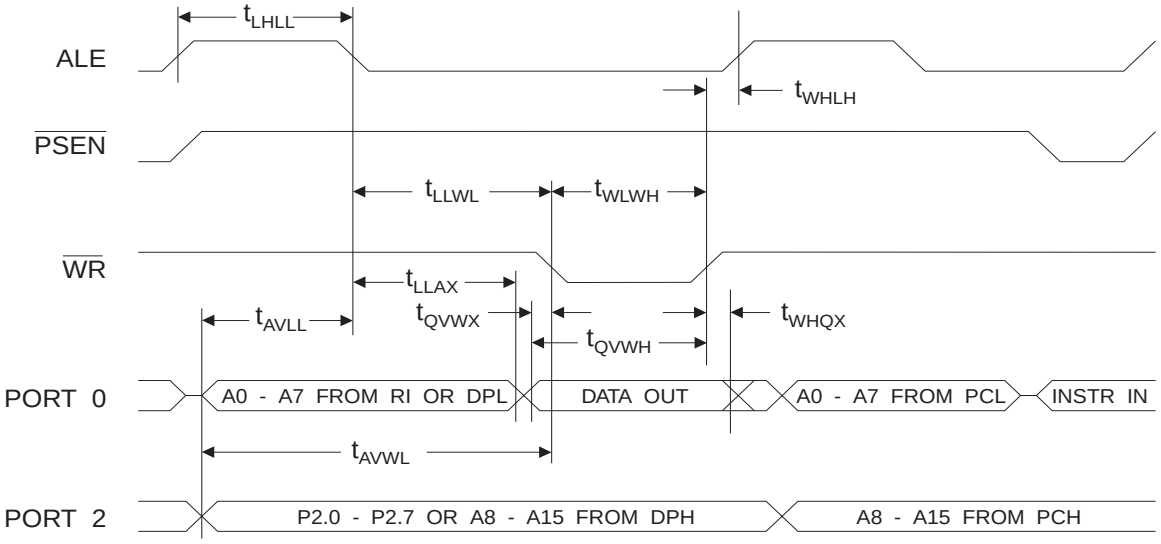
External Program Memory Read Cycle



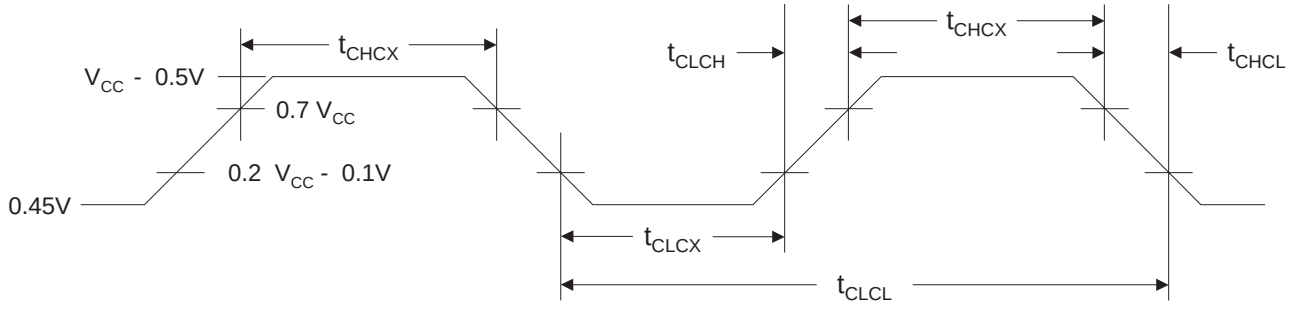
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

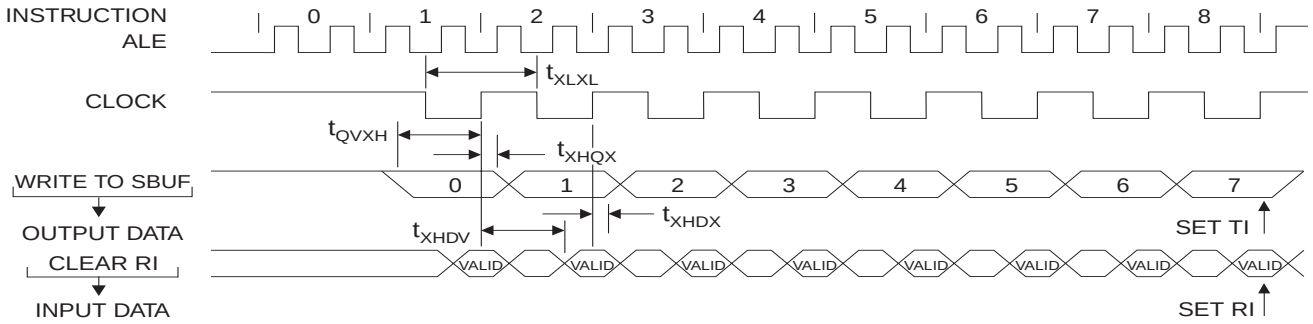
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

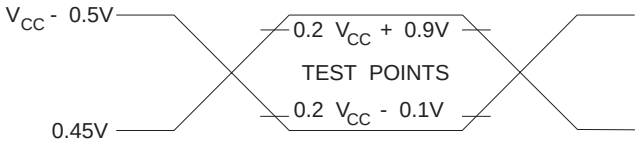
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

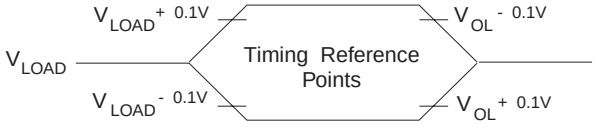


AC Testing Input/Output Waveforms(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

Ultralow Offset Voltage Operational Amplifiers

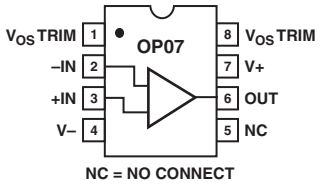
OP07

FEATURES
Low V_{OS}: 75 μV Max
Low V_{OS} Drift: 1.3 μV/°C Max
Ultra-Stable vs. Time: 1.5 μV/Month Max
Low Noise: 0.6 μV p-p Max
Wide Input Voltage Range: ±14 V
Wide Supply Voltage Range: 3 V to 18 V
Fits 725,108A/308A, 741, AD510 Sockets
125°C Temperature-Tested Dice

APPLICATIONS
Wireless Base Station Control Circuits
Optical Network Control Circuits
Instrumentation
Sensors and Controls
Thermocouples
RTDs
Strain Bridges
Shunt Current Measurements
Precision Filters

PIN CONNECTIONS

Epoxy Mini-Dip (P-Suffix)
8-Pin SO (S-Suffix)



GENERAL DESCRIPTION

The OP07 has very low input offset voltage (75 μV max for OP07E) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP07 also features low input bias current (±4 nA for OP07E) and high open-loop gain (200 V/mV for OP07E). The low offsets and high open-loop gain make the OP07 particularly useful for high-gain instrumentation applications.

The wide input voltage range of ±13 V minimum combined with high CMRR of 106 dB (OP07E) and high input impedace provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP07, even at high gain, combined with the freedom from external nulling have made the OP07 an industry standard for instrumentation applications.

The OP07 is available in two standard performance grades. The OP07E is specified for operation over the 0°C to 70°C range, and OP07C over the –40°C to +85°C temperature range.

The OP07 is available in epoxy 8-lead Mini-DIP and 8-lead SOIC. It is a direct replacement for 725,108A, and OP05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. For improved specifications, see the OP177 or OP1177. For ceramic DIP and TO-99 packages and standard micro circuit (SMD) versions, see the OP77.

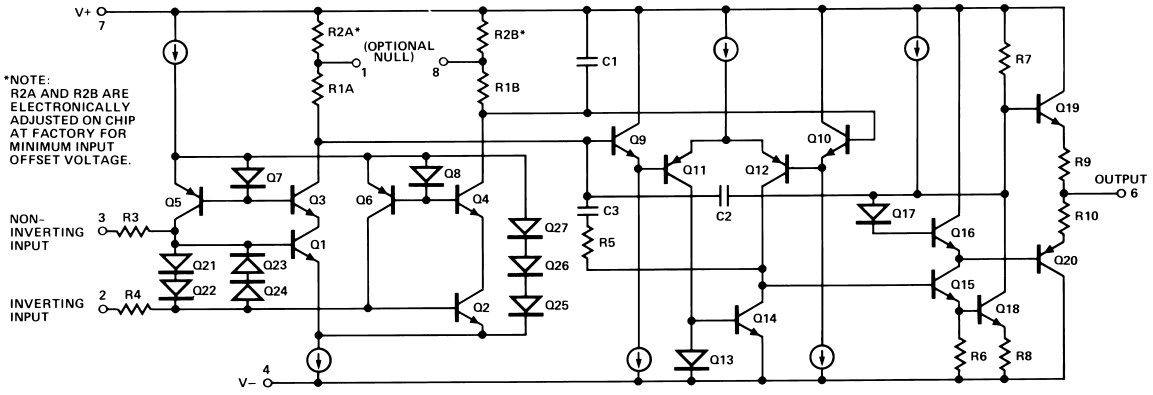


Figure 1. Simplified Schematic

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
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OP07–SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage[1]	V_{OS}			30	75	µV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.3	1.5	µV/Mo
Input Offset Current	I_{OS}			0.5	3.8	nA
Input Bias Current	I_B			±1.2	±4.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		10.3	18.0	nV√Hz
		f_O = 100 Hz[3]		10.0	13.0	nV√Hz
		f_O = 1 kHz		9.6	11.0	nV√Hz
Input Noise Current	I_n p-p			14	30	pA p-p
Input Noise Current Density	I_n	f_O = 10 Hz		0.32	0.80	pA√Hz
		f_O = 100 Hz[3]		0.14	0.23	pA√Hz
		f_O = 1 kHz		0.12	0.17	pA√Hz
Input Resistance—Differential Mode[4]	R_{IN}		15	50		mΩ
Input Resistance—Common-Mode	R_{INCM}			160		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	106	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		5	20	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	200	500		V/mV
		R_L ≥ 500 Ω, V_O = ±0.5 V, V_S = ±3 V[4]	150	400		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12.5	±13.0		V
		R_L ≥ 2 kΩ	±12.0	±12.8		V
		R_L ≥ 1 kΩ	±10.5	±12.0		V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L ≥ 2 kΩ[3]	0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	A_{VOL} = 1[5]	0.4	0.6		MHz
Closed-Loop Output Resistance	R_O	V_O = 0, I_O = 0		60		Ω
Power Consumption	P_d	V_S = ±15 V, No Load		75	120	mW
		V_S = ±13 V, No Load		4	6	mW
Offset Adjustment Range		R_P = 20 kΩ		±4		mV

NOTES

[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

[2]Long-term input offset voltage stability refers to the averaged trend time of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 µV refer to the typical performance curves. Parameter is sample tested.

[3]Sample tested.

[4]Guaranteed by design.

[5]Guaranteed but not tested.

Specifications subject to change without notice.

OP07C ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage[1]	V_{OS}			60	150	µV
Long-Term V_{OS} Stability[2]	V_{OS}/Time			0.4	2.0	µV/Mo
Input Offset Current	I_{OS}			0.8	6.0	nA
Input Bias Current	I_B			±1.8	±7.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.38	0.65	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		10.5	20.0	nV√Hz
		f_O = 100 Hz[3]		10.2	13.5	nV√Hz
		f_O = 1 kHz		9.8	11.5	nV√Hz
Input Noise Current	I_n p-p			15	35	pA p-p
Input Noise Current Density	I_n	f_O = 10 Hz		0.35	0.90	pA√Hz
		f_O = 100 Hz[3]		0.15	0.27	pA√Hz
		f_O = 1 kHz		0.13	0.18	pA√Hz
Input Resistance- Differential Mode[4]	R_{IN}		8	33		mΩ
Input Resistance- Common-Mode	R_{INCM}			120		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		7	32	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	120	400		V/mV
		R_L ≥ 500 Ω, V_O = ±0.5 V, V_S = ±3 V[4]	100	400		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12.0	±13.0		V
		R_L ≥ 2 kΩ	±11.5	±12.8		V
		R_L ≥ 1 kΩ		±12.0		V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L ≥ 2 kΩ[3]	0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	A_{VOL} = 1[5]	0.4	0.6		MHz
Closed-Loop Output Resistance	R_O	V_O = 0, I_O = 0		60		Ω
Power Consumption	P_d	V_S = ±15 V, No Load		80	150	mW
		V_S = ±13 V, No Load		4	8	mW
Offset Adjustment Range		R_P = 20 kΩ		±4		mV

NOTES

[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

[2]Long-term input offset voltage stability refers to the averaged trend time of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 µV refer to the typical performance curves. Parameter is sample tested.

[3]Sample tested.

[4]Guaranteed by design.

[5]Guaranteed but not tested.

Specifications subject to change without notice.

OP07–SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS (V_S = ±15 V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage[1]	V_{OS}			45	130	µV
Voltage Drift without External Trim[2]	TCV_{OS}			0.3	1.3	µV/°C
Voltage Drift with External Trim[3]	TCV_{OSN}	R_P = 20 kΩ		0.3	1.3	µV/°C
Input Offset Current	I_{OS}			0.9	5.3	nA
Input Offset Current Drift	TCI_{OS}			8	35	pA/°C
Input Bias Current	I_B			±1.5	±5.5	nA
Input Bias Current Drift	TCI_B			13	35	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	103	123		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		7	32	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	180	450		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12	±12.6		V

NOTES
[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
[2]Guaranteed by design.
[3]Sample tested.

Specifications subject to change without notice.

OP07C ELECTRICAL CHARACTERISTICS (V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage[1]	V_{OS}			85	250	µV
Voltage Drift without External Trim[2]	TCV_{OS}			0.5	1.8	µV/°C
Voltage Drift with External Trim[3]	TCV_{OSN}	R_P = 20 kΩ		0.4	1.8	µV/°C
Input Offset Current	I_{OS}			1.6	8.0	nA
Input Offset Current Drift	TCI_{OS}			12	50	pA/°C
Input Bias Current	I_B			±2.2	±9.0	nA
Input Bias Current Drift	TCI_B			18	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	97	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		10	51	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	100	400		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±11	±12.6		V

NOTES
[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
[2]Guaranteed by design.
[3]Sample tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S) . . . . . ±22 V
Input Voltage* . . . . . ±22 V
Differential Input Voltage . . . . . ±30 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  S, P Packages . . . . . –65°C to +125°C
Operating Temperature Range
  OP07E . . . . . 0°C to 70°C
  OP07C . . . . . –40°C to +85°C
Junction Temperature Range . . . . . 150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Package Type	θ_{JA}*	θ_{JC}	Units
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SOIC (S)	158	43	°C/W

*θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package, θ_{JA} is specified for device soldered to printed circuit board for SO package.

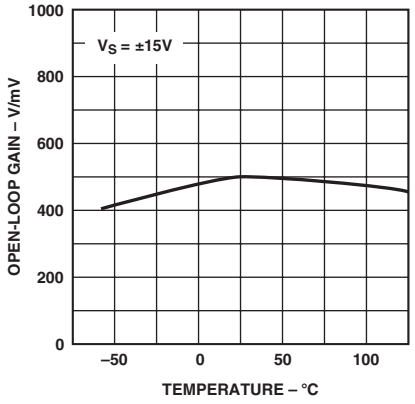
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
OP07EP	0°C to 70°C	8-Lead Epoxy DIP	P-8	
OP07CP	–40°C to 85°C	8-Lead Epoxy DIP	P-8	
OP07CS	–40°C to 85°C	8-Lead SOIC	S-8	

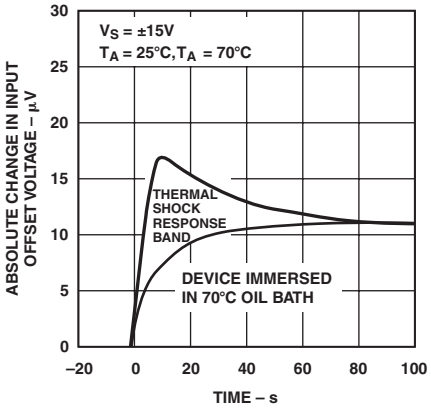
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP07 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

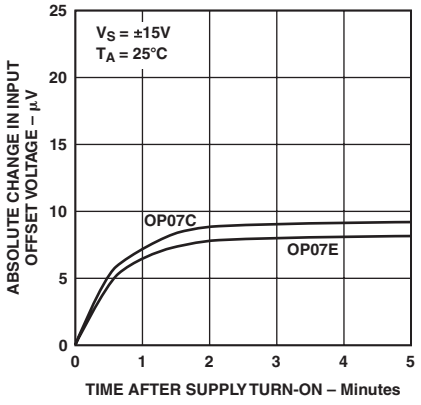
OP07 – Typical Performance Characteristics



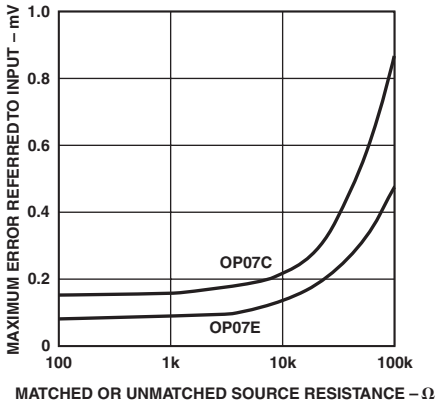
TPC 1. Open-Loop Gain vs. Temperature



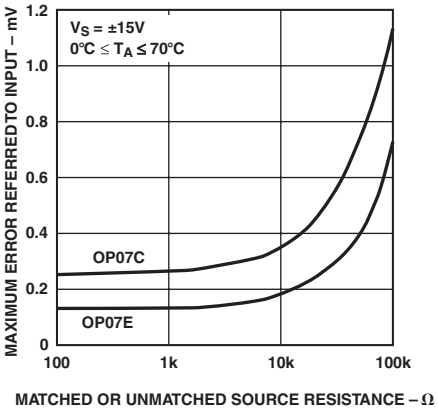
TPC 2. Offset Voltage Change Due to Thermal Shock



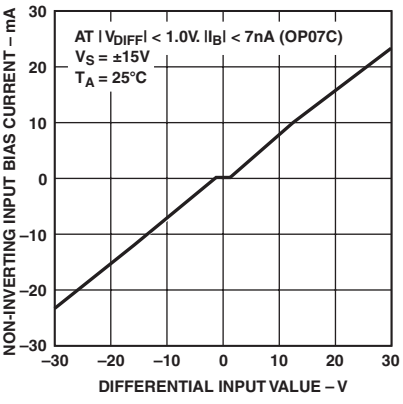
TPC 3. Warm-Up Drift



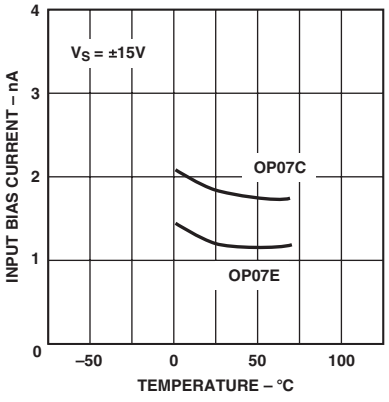
TPC 4. Maximum Error vs. Source Resistance



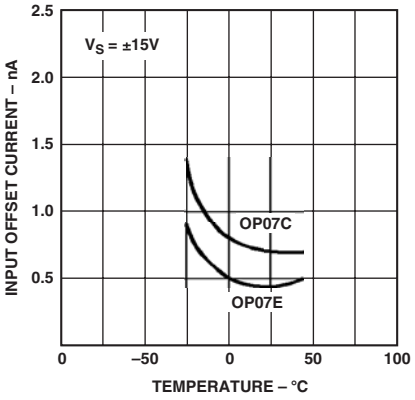
TPC 5. Maximum Error vs. Source Resistance



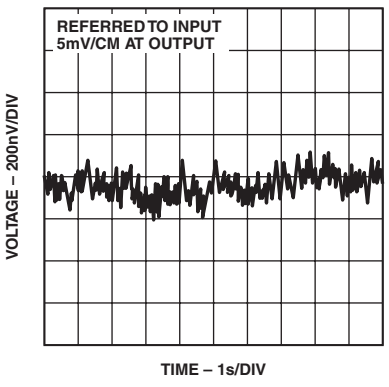
TPC 6. Input Bias Current vs. Differential Input Voltage



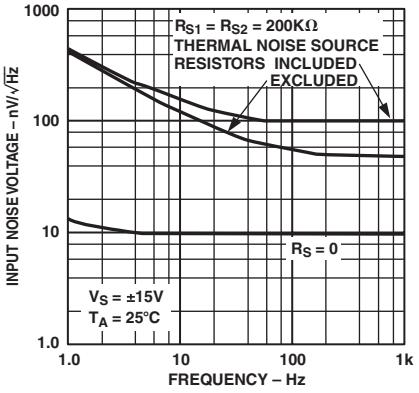
TPC 7. Input Bias Current vs. Temperature



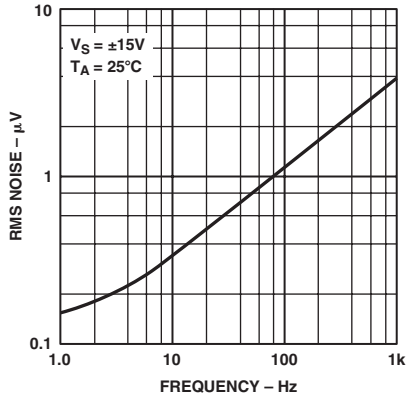
TPC 8. Input Offset Current vs. Temperature



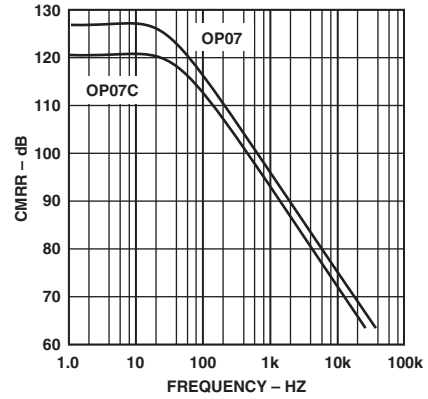
TPC 9. Low Frequency Noise



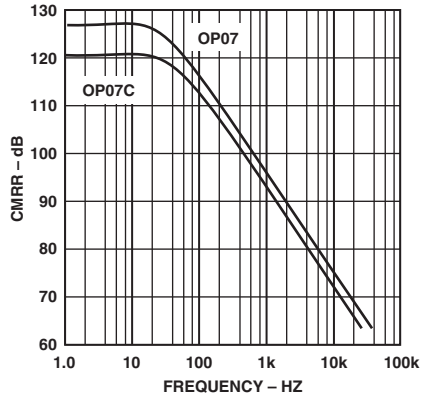
TPC 10. Total Input Noise Voltage vs. Frequency



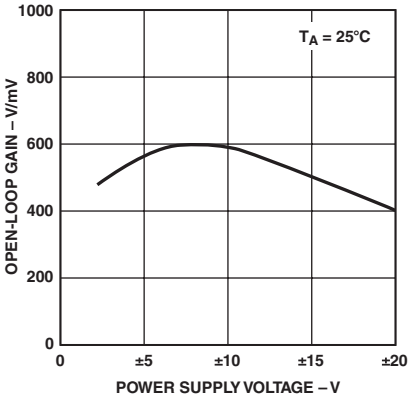
TPC 11. Input Wideband Noise vs Bandwidth (0.1 Hz to Frequency Indicated)



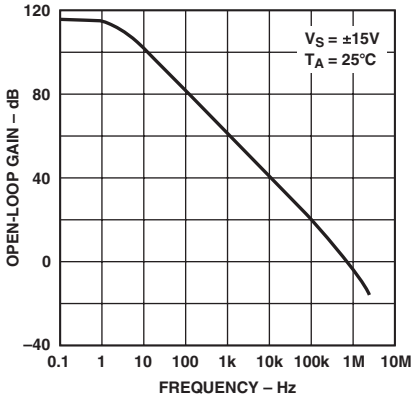
TPC 12. CMRR vs. Frequency



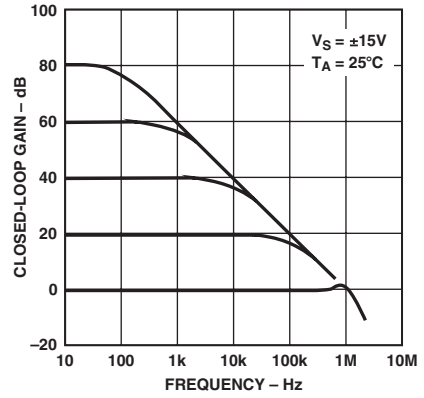
TPC 13. PSRR vs. Frequency



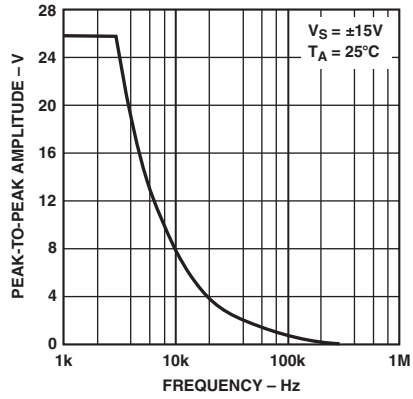
TPC 14. Open-Loop Gain vs Power Supply Voltage



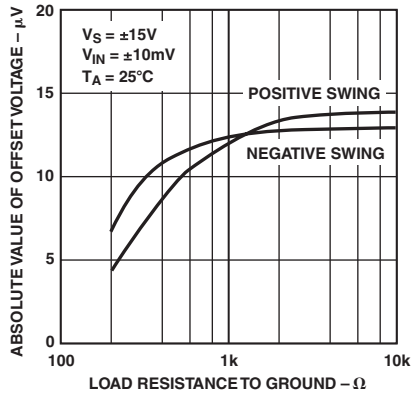
TPC 15. Open-Loop Frequency Response



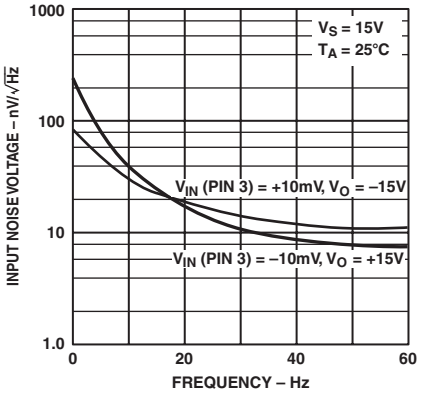
TPC 16. Closed-Loop Response for Various Gain Configurations



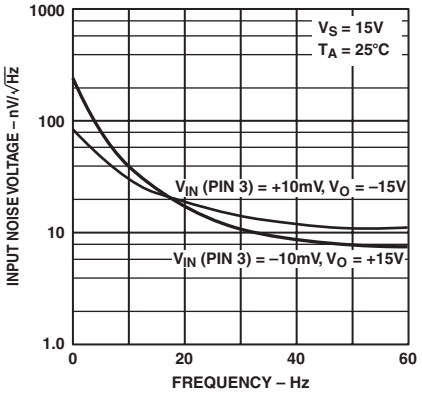
TPC 17. Maximum Output Swing vs. Frequency



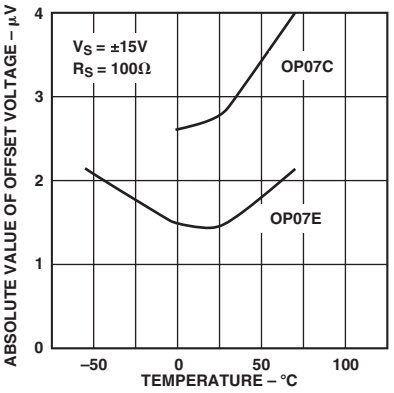
TPC 18. Maximum Output Voltage vs. Load Resistance



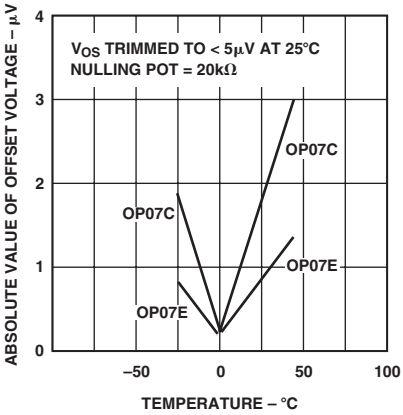
TPC 19. Power Consumption vs. Power Supply



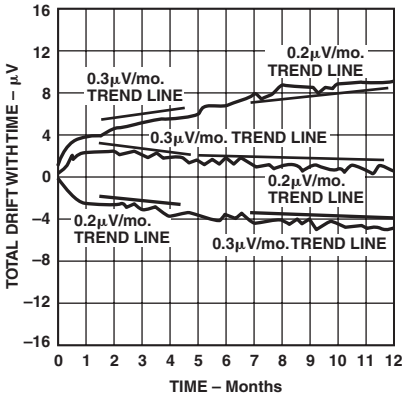
TPC 20. Output Short-Circuit Current vs. Time



TPC 21. Untrimmed Offset Voltage vs. Temperature



TPC 22. Trimmed Offset Voltage vs. Temperature



TPC 23. Offset Voltage Stability vs. Time

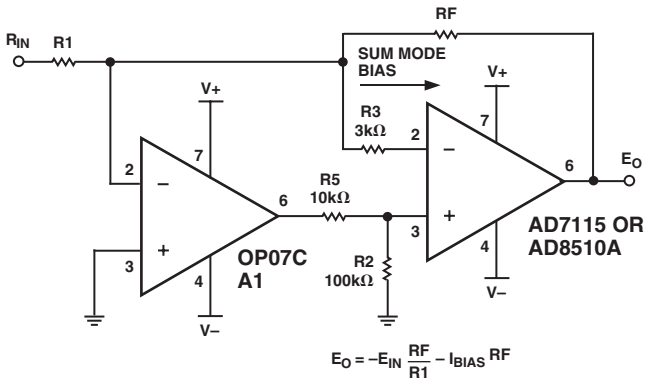


Figure 2. Typical Offset Voltage Test Circuit

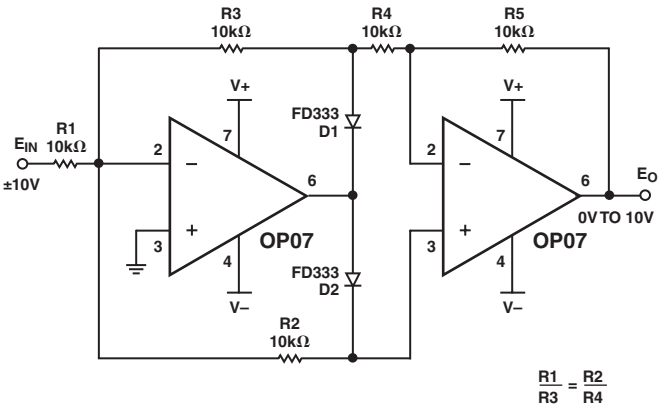


Figure 5. Burn-In circuit

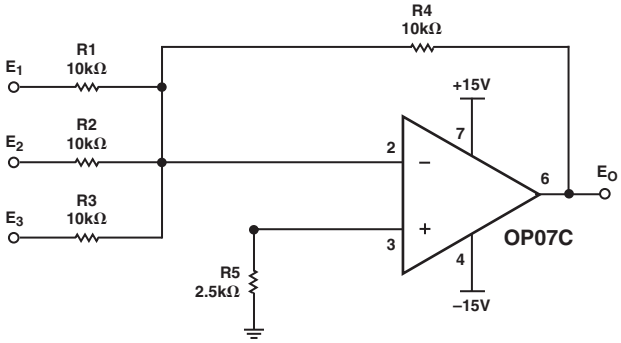
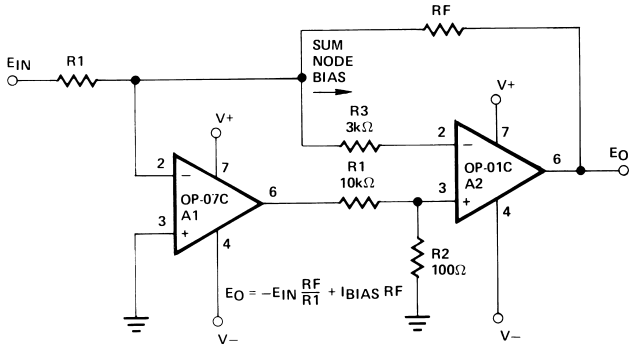


Figure 3. Typical Low-Frequency Noise Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 6. High-Speed, Low VOS Composite Amplifier

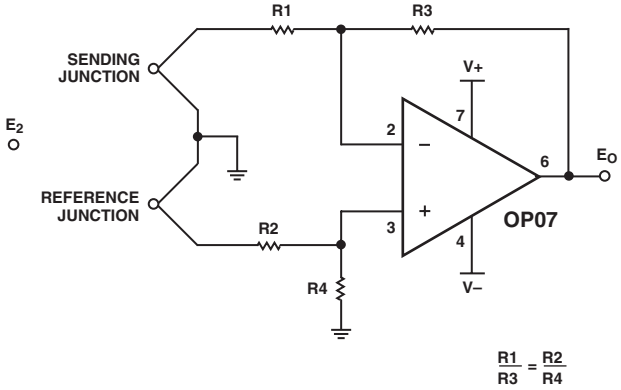
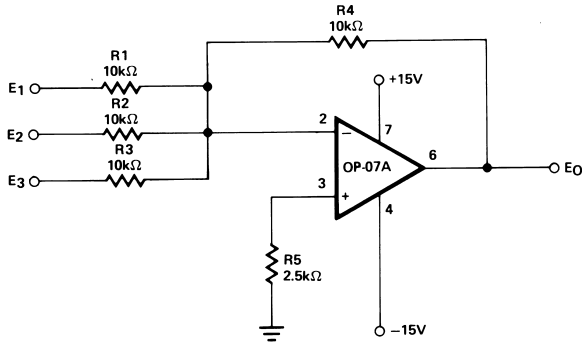


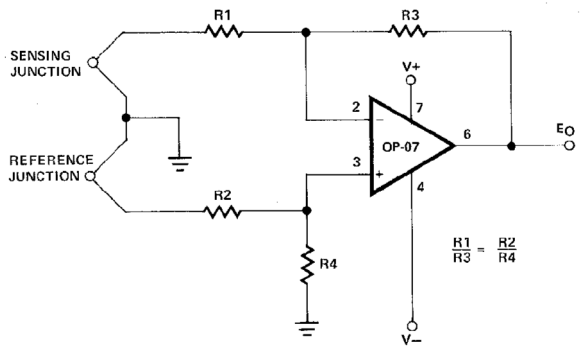
Figure 4. Optional Offset Nulling Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

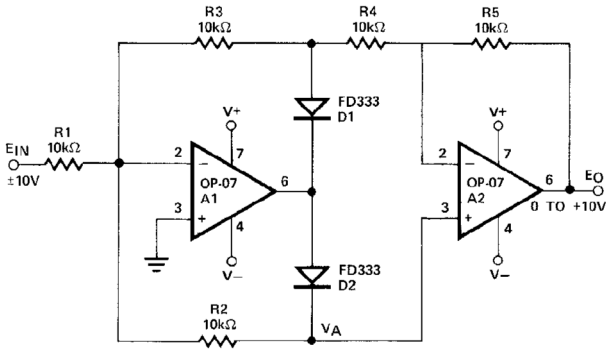
Figure 7. Adjustment-Free Precision Summing Amplifier

TYPICAL APPLICATIONS



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 8. High-Stability Thermocouple Amplifier



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 9. Precision Absolute-Value Circuit

APPLICATIONS INFORMATION

OP07 series units may be substituted directly into 725, 108A/308A* and OP05 sockets with or without removal of external compensation or nulling components. Additionally, the OP07 may be used in unnulled 741 type sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP07 operation. OP07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

PRECISION ABSOLUTE-VALUE CIRCUIT

The OP07 provides stable operation with load capacitance of up to 500 pF and ±10 V swings; larger capacitances should be decoupled with a 50 Q decoupling resistor.

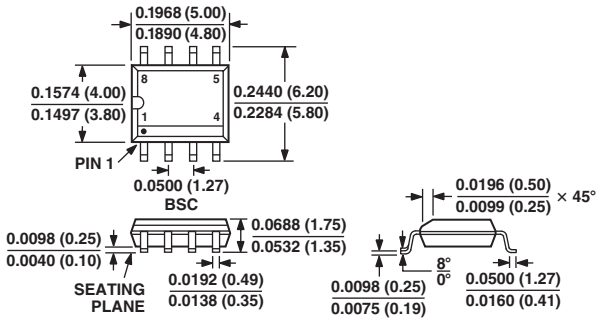
Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

*TO-99 Package only

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SO DIP
(S-Suffix)



Revision History

Location	Page

Data Sheet changed from REV. 0 to REV. A.

PRINTED IN U.S.A.

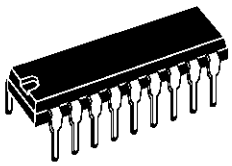
C00316–0–2/02(A)

SGS-THOMSON MICROELECTRONICS

ULN2801A
ULN2802A - ULN2803A
ULN2804A - ULN2805A

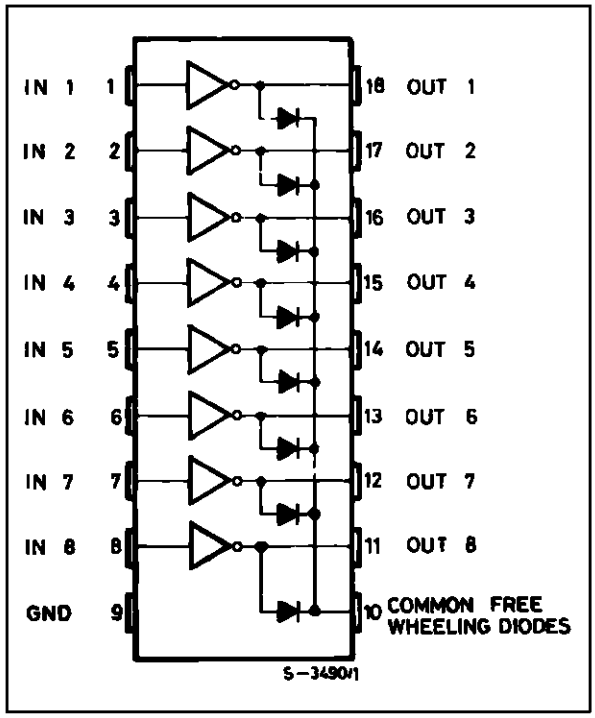
EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT



DIP18

PIN CONNECTION (top view)



DESCRIPTION

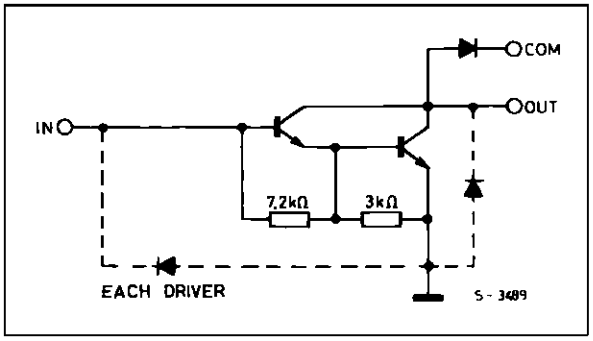
The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600mA (500mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor ; the ULN2802A has a 10.5kΩ input resistor and zener for 14-25V PMOS ; the ULN2803A has a 2.7kΩ input resistor for 5V TTL and CMOS ; the ULN2804A has a 10.5kΩ input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

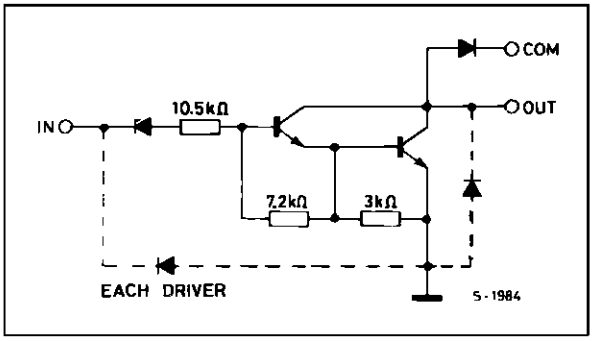
All types are supplied in a 18-lead plastic DIP with a copper lead from and feature the convenient input-opposite-output pinout to simplify board layout.

SCHEMATIC DIAGRAM AND ORDER CODES

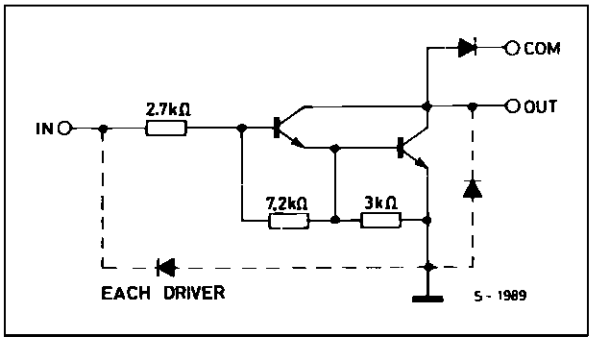
For ULN2801A (each driver for PMOS-CMOS)



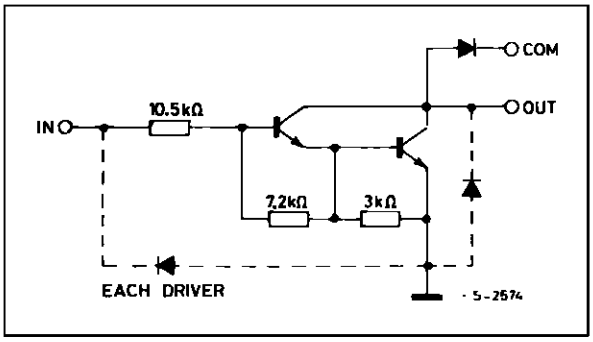
For ULN2802A (each driver for 14-15 V PMOS)



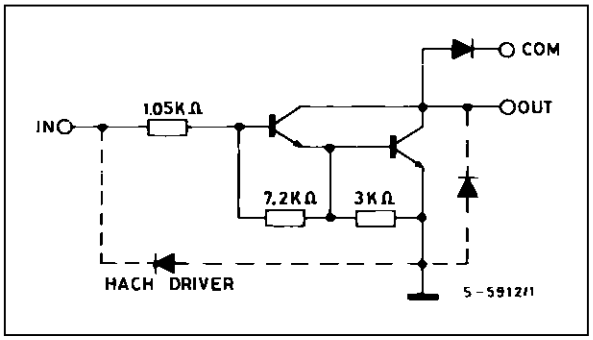
For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS



For ULN2805A (each driver for high out TTL)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULN2802A, UL2803A, ULN2804A for ULN2805A	 30 15	V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	 1.0 2.25	W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
Tj	Junction Temperature Range	– 20 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50V T_{amb} = 70°C, V_{CE} = 50V T_{amb} = 70°C for ULN2802A V_{CE} = 50V, V_i = 6V for ULN2804A V_{CE} = 50V, V_i = 1V			50 100 500 500	µA µA µA µA	1a 1a 1b 1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100mA, I_B = 250µA I_C = 200mA, I_B = 350µA I_C = 350mA, I_B = 500µA		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
$I_{i(on)}$	Input Current	for ULN2802A V_i = 17V for ULN2803A V_i = 3.85V for ULN2804A V_i = 5V V_i = 12V for ULN2805A V_i = 3V		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70°C, I_C = 500µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V for ULN2802A I_C = 300mA for ULN2803A I_C = 200mA I_C = 250mA I_C = 300mA for ULN2804A I_C = 125mA I_C = 200mA I_C = 275mA I_C = 350mA for ULN2805A I_C = 350mA			 13 2.4 2.7 3 5 6 7 8 2.4	 V V V V V V V V V	5
h_{FE}	DC Forward Current Gain	for ULN2801A V_{CE} = 2V, I_C = 350mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50V T_{amb} = 70°C, V_R = 50V			50 100	µA µA	6 6
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2	V	7

TEST CIRCUITS

Figure 1a.

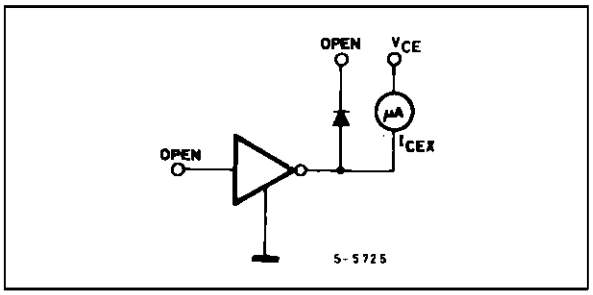


Figure 1b.

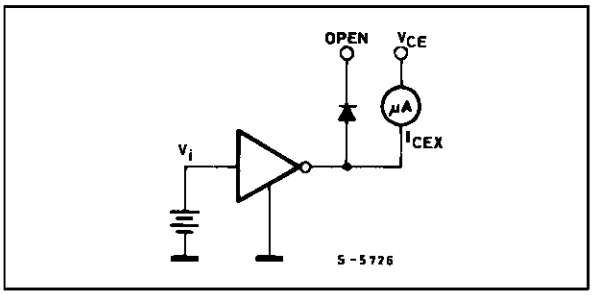


Figure 2.

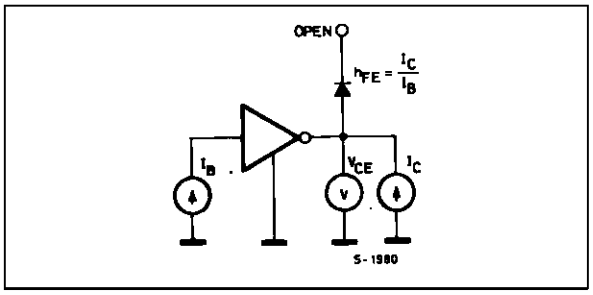


Figure 3.

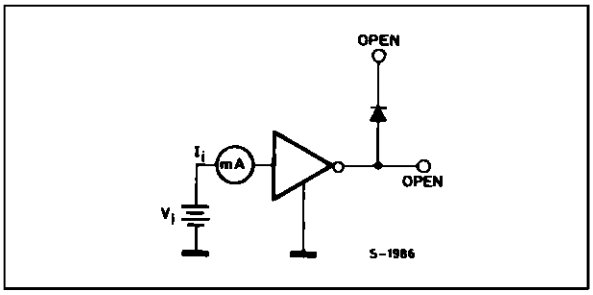


Figure 4.

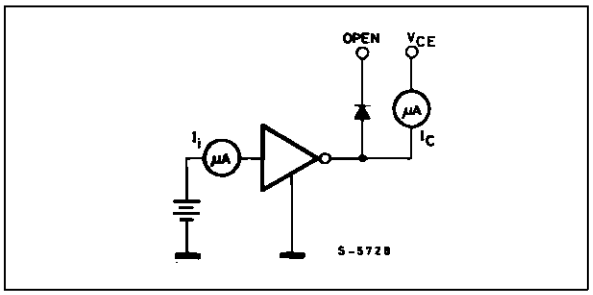


Figure 5.

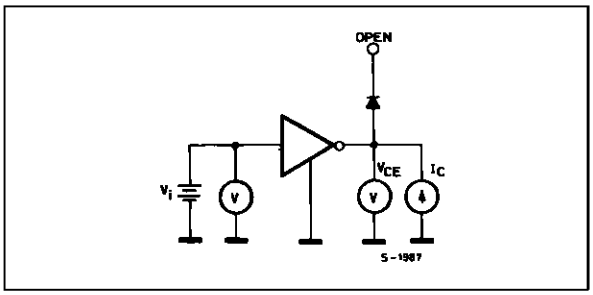


Figure 6.

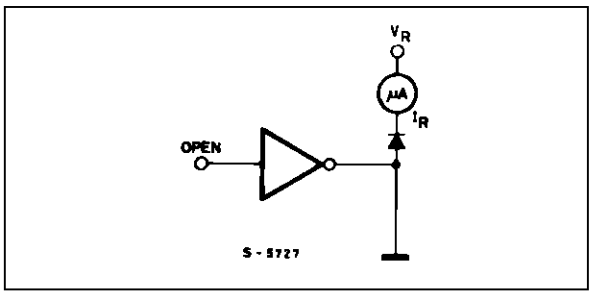


Figure 7.

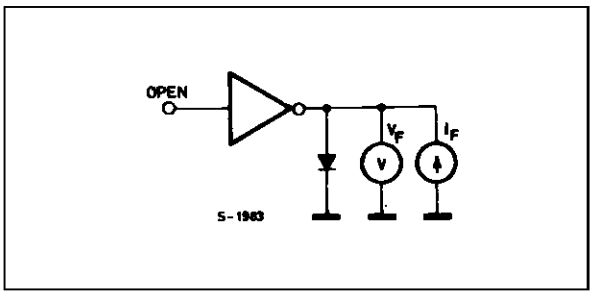


Figure 8 : Collector Current as a Function of Saturation Voltage.

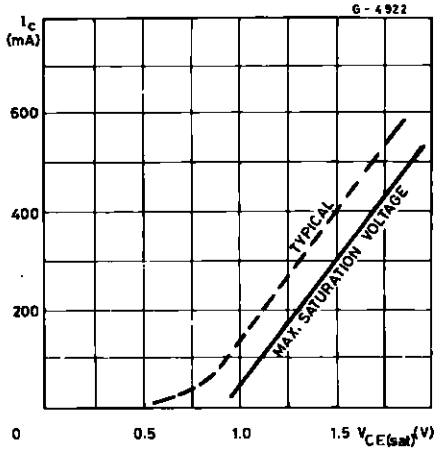


Figure 9 : Collector Current as a Function of Input Current.

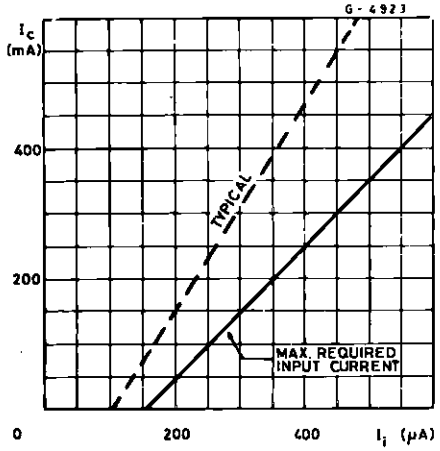


Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.

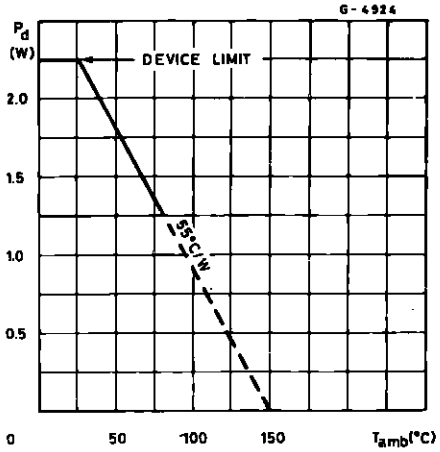


Figure 11 : Peak Collector Current as a Function of Duty Cycle.

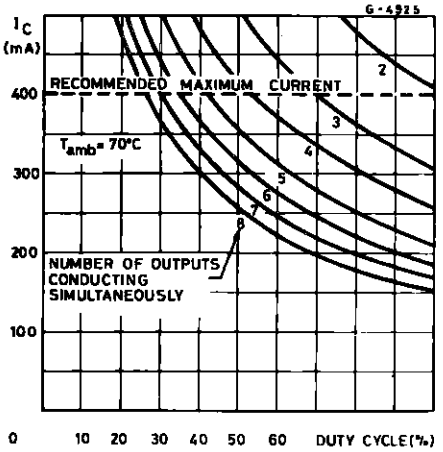


Figure 12 : Peak Collector Current as a Function of Duty.

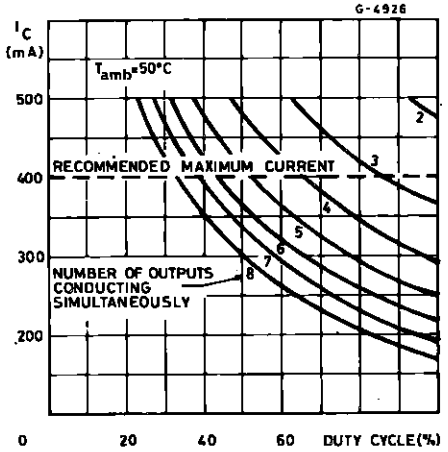


Figure 13 : Input Current as a Function of Input Voltage (for ULN2802A).

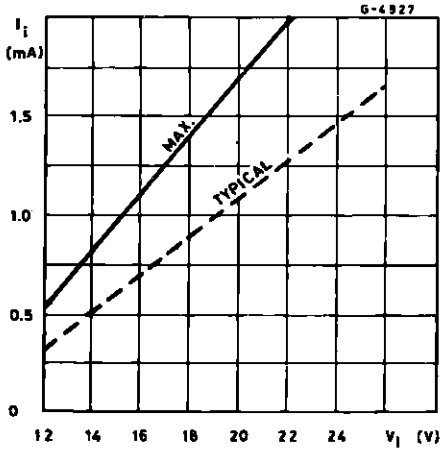


Figure 14 : Input Current as a Function of Input Voltage (for ULN2804A)

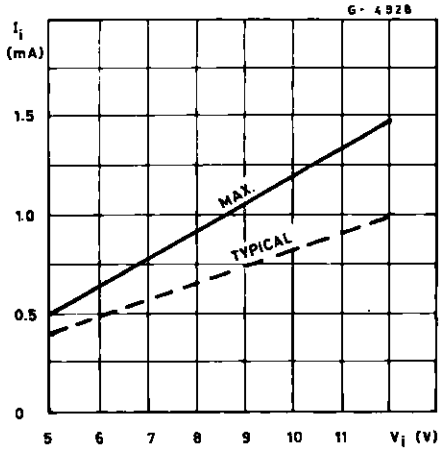


Figure 15 : Input Current as a Function of Input Voltage (for ULN2803A)

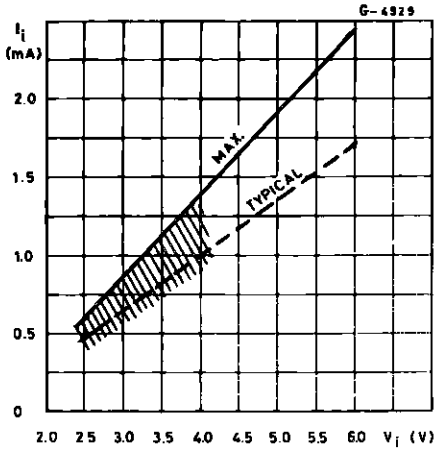
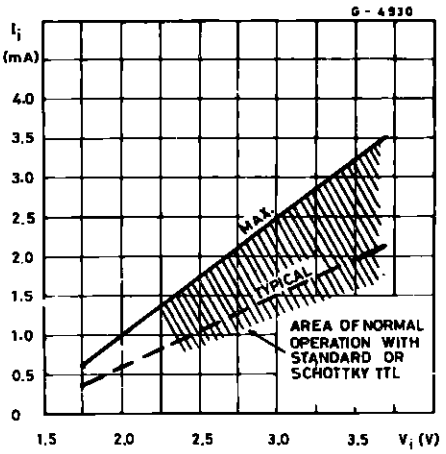
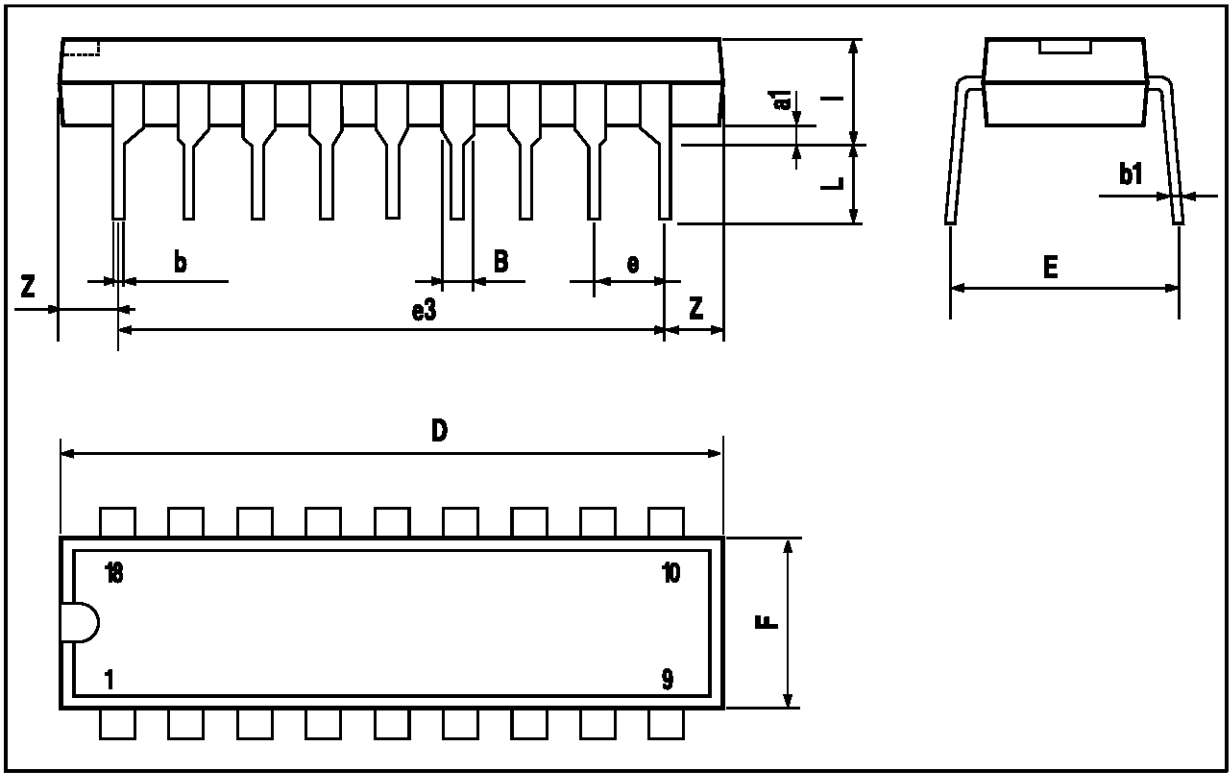


Figure 16 : Input Current as a Function of Input Voltage (for ULN2805A)



DIP18 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.46			0.018	
b1		0.25			0.010	
D			23.24			0.915
E		8.5			0.335	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z		1.27	1.59		0.050	0.063



FAIRCHILD SEMICONDUCTOR®

September 1983
Revised May 2005

MM74HC14
Hex Inverting Schmitt Trigger

General Description

The MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V

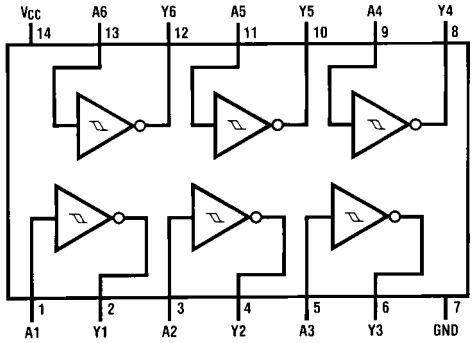
Ordering Code:

Order Number	Package Number	Package Description
MM74HC14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC14MX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC14SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC14MTCX_NL	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC14N_NL	N14A	Pb-Free 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

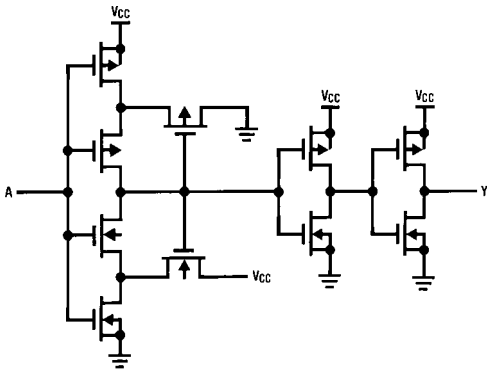
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Logic Diagram



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−55	+125	°C

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{T+}	Positive Going	Minimum	2.0V	1.2	1.0	1.0	1.0	V
	Threshold Voltage		4.5V	2.7	2.0	2.0	2.0	V
			6.0V	3.2	3.0	3.0	3.0	V
		Maximum	2.0V	1.2	1.5	1.5	1.5	V
			4.5V	2.7	3.15	3.15	3.15	V
			6.0V	3.2	4.2	4.2	4.2	V
V_{T-}	Negative Going	Minimum	2.0V	0.7	0.3	0.3	0.3	V
	Threshold Voltage		4.5V	1.8	0.9	0.9	0.9	V
			6.0V	2.2	1.2	1.2	1.2	V
		Maximum	2.0V	0.7	1.0	1.0	1.0	V
			4.5V	1.8	2.2	2.2	2.2	V
			6.0V	2.2	3.0	3.0	3.0	V
V_H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	0.2	V
			4.5V	0.9	0.4	0.4	0.4	V
			6.0V	1.0	0.5	0.5	0.5	V
		Maximum	2.0V	0.5	1.0	1.0	1.0	V
			4.5V	0.9	1.4	1.4	1.4	V
			6.0V	1.0	1.5	1.5	1.5	V
V_{OH}	Minimum HIGH Level	V_{IN} = V_{IL}	2.0V	2.0	1.9	1.9	1.9	V
	Output Voltage	$\|I_{OUT}\|$ = 20 μA	4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IL}						
		$\|I_{OUT}\|$ = 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level	V_{IN} = V_{IH}	2.0V	0	0.1	0.1	0.1	V
	Output Voltage	$\|I_{OUT}\|$ = 20 μA	4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH}						
		$\|I_{OUT}\|$ = 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent	V_{IN} = V_{CC} or GND	6.0V		2.0	20	40	μA
	Supply Current	I_{OUT} = 0 μA						

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	22	ns

AC Electrical Characteristics

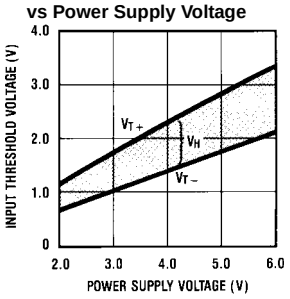
V_{CC} = 2.0V to 6.0V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C		Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	11	21	26	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

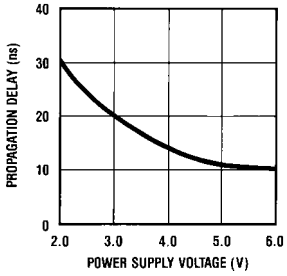
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Performance Characteristics

Input Threshold, V_{T+}, V_{T-}, vs Power Supply Voltage

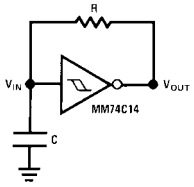


Propagation Delay vs Power Supply



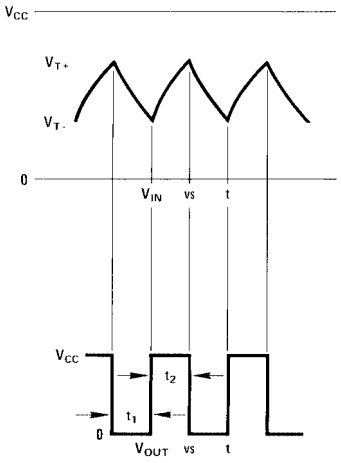
Typical Applications

Low Power Oscillator



$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

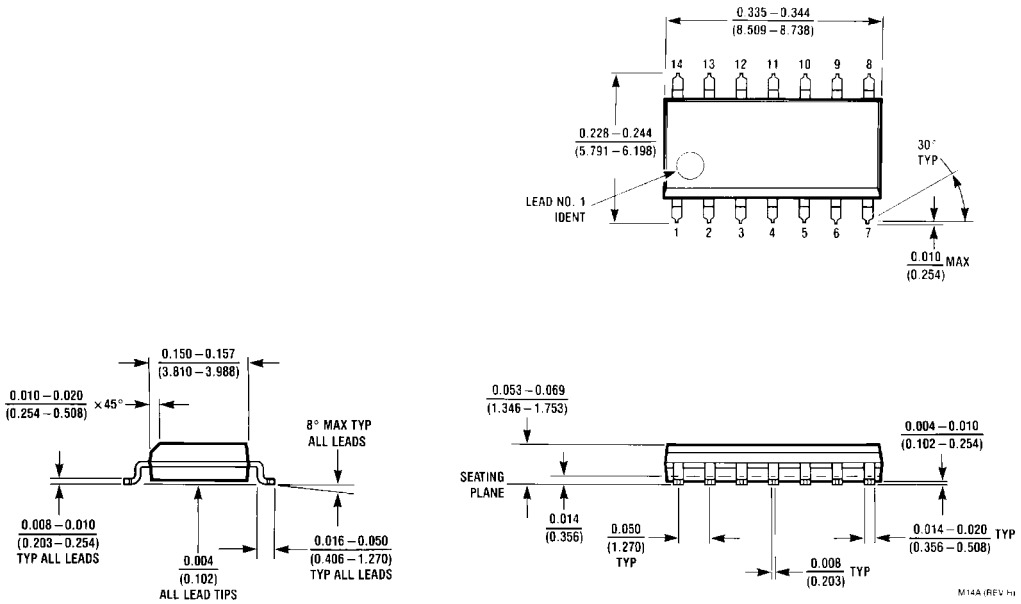
$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$



$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$

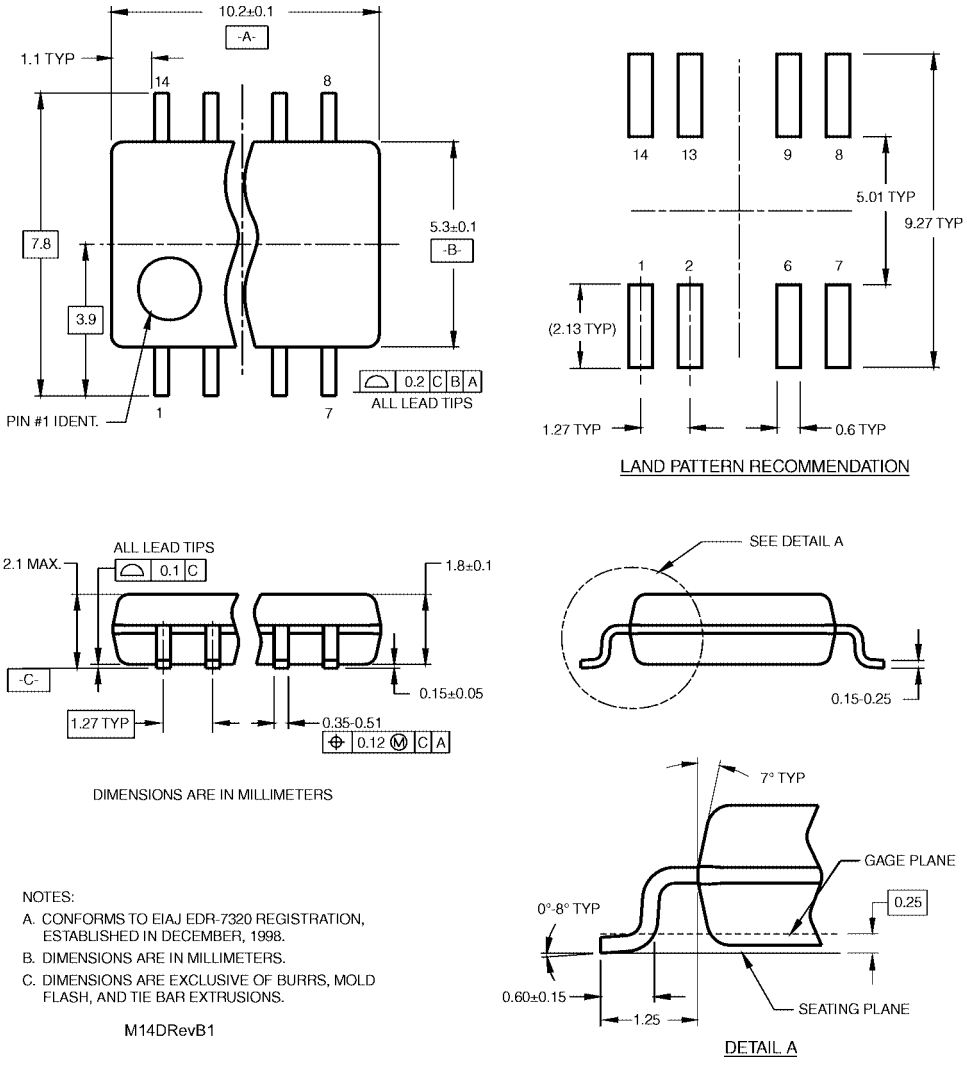
Note: The equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

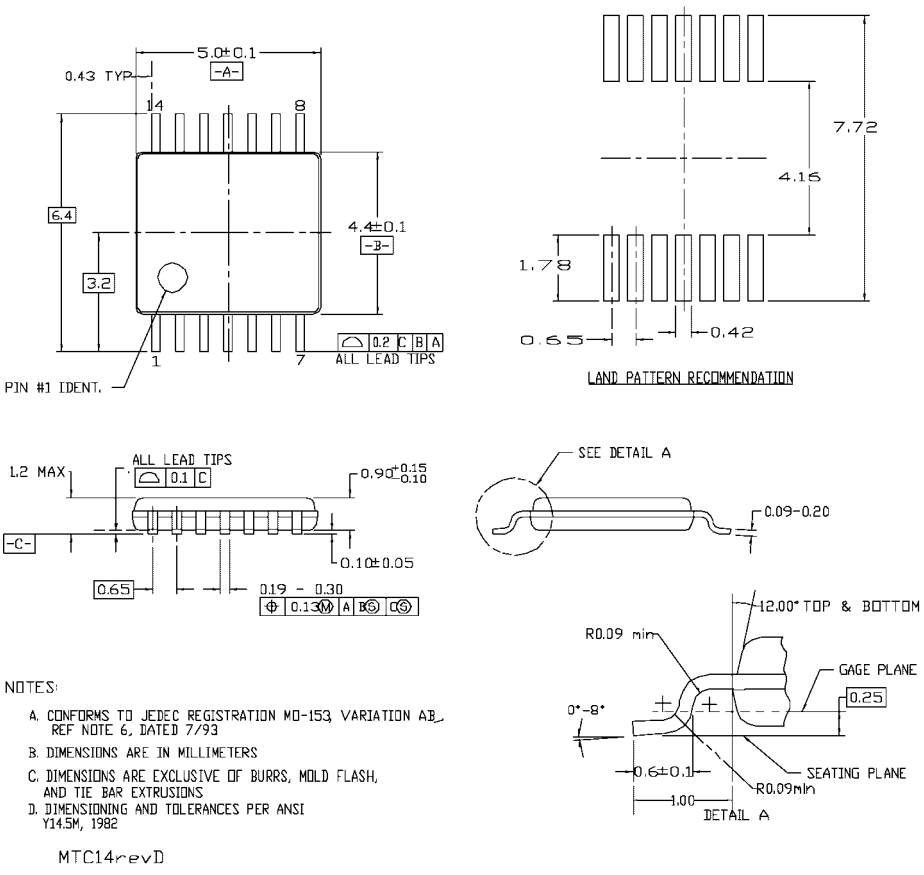
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

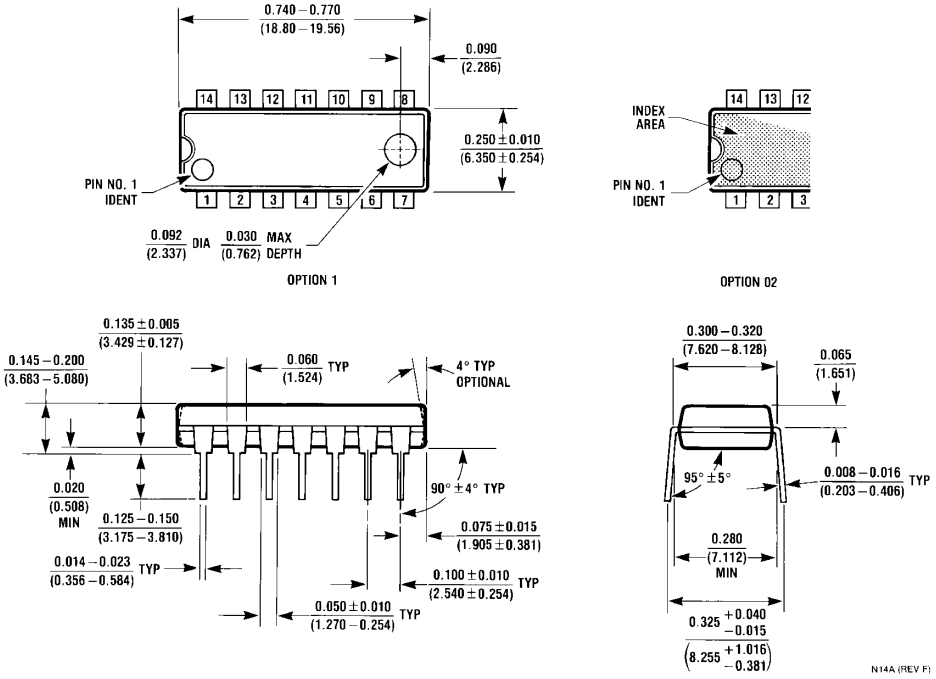
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A