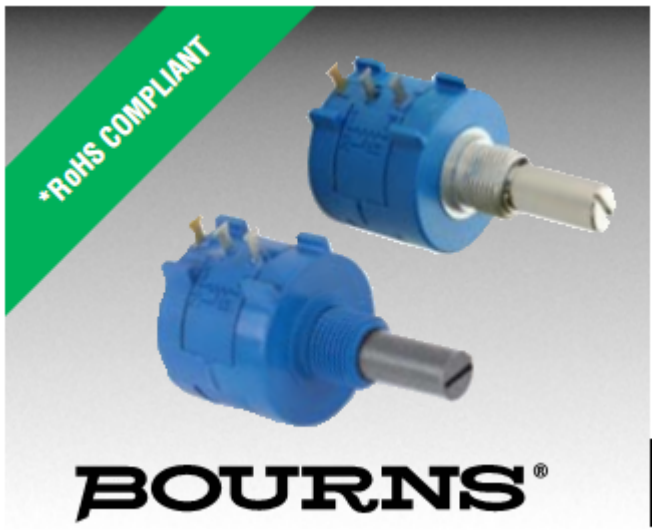
LAMPIRAN B

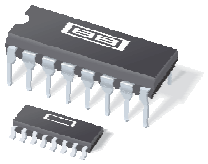
DATASHEET

Wirewound 3590



Angle, Mechanical	:	3600 °
Diameter, Shaft	:	0.248 "
Dielectric Strength	:	1500 VAC
Dimensions	:	0.875"Dia×0.732"L
Linearity	:	±0.25 %
Material, Element	:	Wirewound
Mounting Type	:	Panel
Number of Turns	:	10
Power, Rating	:	2 W
Resistance	:	1 Kilohms
Resistance, Insulation	:	1000 Megohms
Resolution	:	0.029 %
Rotational Life	:	1000000 Revolutions
Taper	:	Linear
Temperature Coefficient	:	±50 ppm/°C
Temperature, Operating, Maximum	:	+125 °C
Temperature, Operating, Minimum	:	+1 °C
Termination	:	Lug
Tolerance	:	±5 %
Torque	:	0.35 N-cm
Type	:	Potentiometer

BURR - BROWN®



INA125

INSTRUMENTATION AMPLIFIER
With Precision Voltage Reference

FEATURES

- LOW QUIESCENT CURRENT: 460 A
- PRECISION VOLTAGE REFERENCE: 1.24V, 2.5V, 5V or 10V
- SLEEP MODE
- LOW OFFSET VOLTAGE: 250 V max
- LOW OFFSET DRIFT: 2 V/ C max
- LOW INPUT BIAS CURRENT: 20nA max
- HIGH CMR: 100dB min
- LOW NOISE: 38nV/ Hz at f = 1kHz
- INPUT PROTECTION TO 40V
- WIDE SUPPLY RANGE
  Single Supply: 2.7V to 36V
  Dual Supply: 1.35V to 18V
- 16-PIN DIP AND SO-16 SOIC PACKAGES

APPLICATIONS

- PRESSURE AND TEMPERATURE BRIDGE AMPLIFIERS
- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- MULTI-CHANNEL DATA ACQUISITION
- BATTERY OPERATED SYSTEMS
- GENERAL PURPOSE INSTRUMENTATION

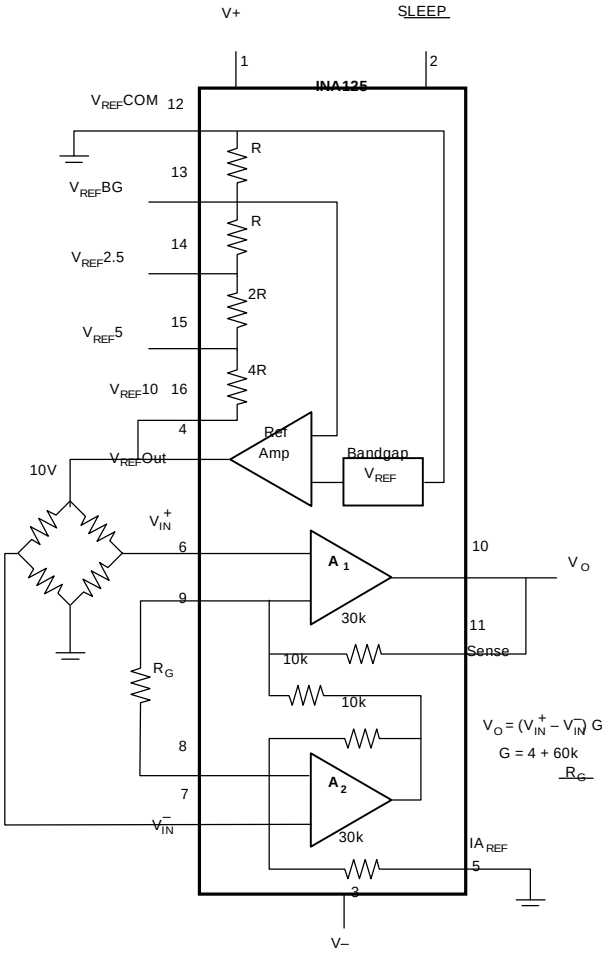
DESCRIPTION

The INA125 is a low power, high accuracy instrumentation amplifier with a precision voltage reference. It provides complete bridge excitation and precision differential-input amplification on a single integrated circuit.

A single external resistor sets any gain from 4 to 10,000. The INA125 is laser-trimmed for low offset voltage (250 V), low offset drift (2 V/ C), and high common-mode rejection (100dB at G = 100). It operates on single (+2.7V to +36V) or dual (1.35V to 18V) supplies.

The voltage reference is externally adjustable with pin-selectable voltages of 2.5V, 5V, or 10V, allowing use with a variety of transducers. The reference voltage is accurate to 0.5% (max) with 35ppm/ C drift (max). Sleep mode allows shutdown and duty cycle operation to save power.

The INA125 is available in 16-pin plastic DIP and SO-16 surface-mount packages and is specified for the –40 C to +85 C industrial temperature range.



SPECIFICATIONS: V_S = 15V

At T_A = +25 C, V_S = 15V, IA common = 0V, V_{REF} common = 0V, and R_L = 10k , unless otherwise noted.

PARAMETER	CONDITIONS	INA125P, U			INA125PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial			50	250		*	500	V V/
vs Temperature vs			0.25	2		*	5	C
Power Supply	V_S = 1.35V to 18V, G = 4		3	20		*	50	V/V
Long-Term Stability			0.2			*		V/mo
Impedance, Differential			10^{11} || 2			*		|| pF
Common-Mode			10^{11} || 9			*		|| pF
Safe Input Voltage Input				40			*	V
Voltage Range Common-			See Text			*		
Mode Rejection	V_{CM} = –10.7V to +10.2V							
	G = 4	78	84		72	*		dB
	G = 10	86	94		80	*		dB
	G = 100	100	114		90	*		dB
	G = 500	100	114		90	*		dB
BIAS CURRENT	V_{CM} = 0V		10	25		*	50	nA
vs Temperature			60			*		pA/ C
Offset Current			0.5	2.5		*	5	nA
vs Temperature			0.5			*		pA/ C
NOISE, RTI	R_S = 0							
Voltage Noise, f = 10Hz			40			*	—	nV/ Hz
f = 100Hz			38			*	—	nV/ Hz
f = 1kHz			38			*	—	nV/ Hz
f = 0.1Hz to 10Hz			0.8			*		Vp-p
Current Noise, f = 10Hz f			170			*	—	fA/ Hz
= 1kHz			56			*	—	fA/ Hz
f = 0.1Hz to 10Hz			5			*		pAp-p
GAIN								
Gain Equation			4 + 60k /R_G			*		V/V
Range of Gain		4		10,000	*		*	V/V
Gain Error	V_O = –14V to +13.3V							
	G = 4		0.01	0.075		*	0.1	%
	G = 10		0.03	0.3		*	0.5	%
	G = 100		0.05	0.5		*	1	%
	G = 500		0.1			*		%
Gain vs Temperature								
	G = 4		1	15		*	*	ppm/ C
	G > 4[1]		25	100		*	*	ppm/ C
Nonlinearity	V_O = –14V to +13.3V							
	G = 4		0.0004	0.002		*	0.004	% of FS
	G = 10		0.0004	0.002		*	0.004	% of FS
	G = 100		0.001	0.01		*	*	% of FS
	G = 500		0.002			*		% of FS
OUTPUT								
Voltage: Positive		(V+)–1.7	(V+)–0.9		*	*		V V
Negative		(V–)+1	(V–)+0.4		*	*		pF
Load Capacitance Stability			1000			*		mA
Short-Circuit Current			–9/+12			*		
VOLTAGE REFERENCE	V_{REF} = +2.5V, +5V, +10V							
Accuracy	I_L = 0		0.15	0.5		*	1	% ppm/
vs Temperature	I_L = 0		18	35		*	100	C ppm/V
vs Power Supply, V+	V+ = (V_{REF} + 1.25V) to +36V		20	50		*	100	ppm/mA
vs Load	I_L = 0 to 5mA		3	75		*	*	V
Dropout Voltage, (V+) – V_{REF}[2]	Ref Load = 2k	1.25	1		*	*		V
Bandgap Voltage Reference			1.24			*		%
Accuracy	I_L = 0		0.5			*		ppm/ C
vs Temperature	I_L = 0		18			*		

SPECIFICATIONS: V_S = 15V (CONT)

At T_A = +25 C, V_S = 15V, IA common = 0V, V_{REF} common = 0V, and R_L = 10k , unless otherwise noted.

PARAMETER CONDITIONS		INA125P, U			INA125PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 4		150			✻		kHz
	G = 10		45			✻		kHz
	G = 100		4.5			✻		kHz
	G = 500		0.9			✻		kHz
Slew Rate	G = 4, 10V Step G		0.2			✻		V/ s
Settling Time, 0.01%	= 4, 10V Step G =		60			✻		s
	10, 10V Step		83			✻		s
	G = 100, 10V Step		375			✻		s
	G = 500, 10V Step		1700			✻		s
Overload Recovery	50% Overdrive		5			✻		s
POWER SUPPLY								
Specified Operating Voltage			15			✻		V
Specified Voltage Range		1.35		18	✻		✻	V
Quiescent Current, Positive	I_O = I_{REF} = 0mA		460	525		✻	✻	A
Negative	I_O = I_{REF} = 0mA		–280	–325		✻	✻	A
Reference Ground Current[3]			180			✻		A
Sleep Current (V_{SLEEP} 100mV)	R_L = 10k , Ref Load = 2k		1	25		✻	✻	A
SLEEP MODE PIN[4]								
V_{IH} (Logic high input voltage)		+2.7		V+	✻		✻	V
V_{IL} (Logic low input voltage)		0		+0.1	✻		✻	V
I_{IH} (Logic high input current)			15			✻		A
I_{IL} (Logic low input current)			0			✻		A
Wake-up Time[5]			150			✻		s
TEMPERATURE RANGE								
Specification Range		–40		+85	✻		✻	C
Operation Range		–55		+125	✻		✻	C
Storage Range		–55		+125	✻		✻	C
Thermal Resistance, $_{JA}$								
16-Pin DIP			80			✻		C/W
SO-16 Surface-Mount			100			✻		C/W

✻ Specification same as INA125P, U.

NOTES: (1) Temperature coefficient of the "Internal Resistor" in the gain equation. Does not include TCR of gain-setting resistor, R_G. (2) Dropout voltage is the positive supply voltage minus the reference voltage that produces a 1% decrease in reference voltage. (3) V_{REF}COM pin. (4) Voltage measured with respect to Reference Common. Logic low input selects Sleep mode. (5) IA and Reference, see Typical Performance Curves.

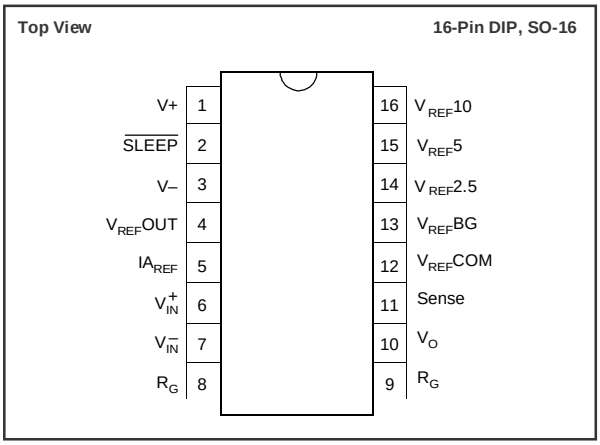
SPECIFICATIONS: V_S = +5V

At T_A = +25 C, V_S = +5V, IA common at V_S/2, V_{REF} common = V_S/2, V_{CM} = V_S/2, and R_L = 10k to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	INA125P, U			INA125PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial			75	500		✻	750	V V/
vs Temperature vs			0.25			✻		C
Power Supply	V_S = +2.7V to +36V		3	20		✻	50	V/V
Input Voltage Range			See Text			✻		
Common-Mode Rejection	V_{CM} = +1.1V to +3.6V							
	G = 4	78	84		72	✻		dB
	G = 10	86	94		80	✻		dB
	G = 100	100	114		90	✻		dB
	G = 500	100	114		90	✻		dB
GAIN								
Gain Error	V_O = +0.3V to +3.8V							
	G = 4		0.01			✻		%
OUTPUT								
Voltage, Positive		(V+)–1.2	(V+)–0.8		✻	✻		V
Negative		(V–)+0.3	(V–)+0.15		✻	✻		V
POWER SUPPLY								
Specified Operating Voltage			+5			✻		V
Operating Voltage Range		+2.7		+36	✻		✻	V
Quiescent Current	I_O = I_{REF} = 0mA		460	525		✻	✻	A
Sleep Current (V_{SLEEP} 100mV)	R_L = 10k , Ref Load = 2k		1	25		✻	✻	A

✻ Specification same as INA125P, U.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with ap- propriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage, V+ to V–	36V
Input Signal Voltage	40V
Output Short Circuit	Continuous
Operating Temperature	–55 C to +125 C
Storage Temperature	–55 C to +125 C
Lead Temperature (soldering, 10s)	+300 C

NOTE: Stresses above these ratings may cause permanent damage.

PACKAGE INFORMATION

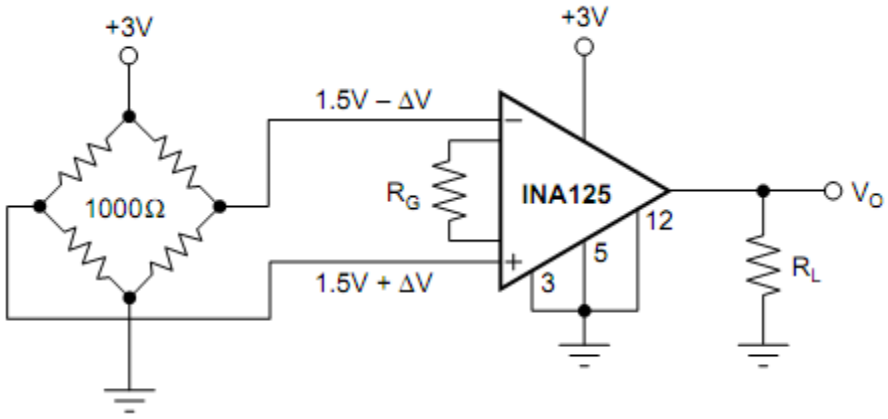
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
INA125PA	16-Pin Plastic DIP	180
INA125P	16-Pin Plastic DIP	180
INA125UA	SO-16 Surface-Mount	265
INA125U	SO-16 Surface-Mount	265

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

SINGLE SUPPLY OPERATION

The INA125 can be used on single power supplies of +2.7V to +36V. Figure 5 shows a basic single supply circuit. The IA_{REF}, V_{REF}COM, and V– terminals are connected to ground. Zero differential input voltage will demand an output volt- age of 0V (ground). When the load is referred to ground as shown, actual output voltage swing is limited to approxi- mately 150mV above ground. The typical performance curve "Output Voltage Swing vs Output Current" shows how the output swing varies with output current.

With single supply operation, careful attention should be paid to input common-mode range, output voltage swing of both op amps, and the voltage applied to the IA_{REF} terminal. V_{IN+} and $V_{IN–}$ must both be 1V above ground for linear operation. You cannot, for instance, connect the inverting input to ground and measure a voltage connected to the non- inverting input.

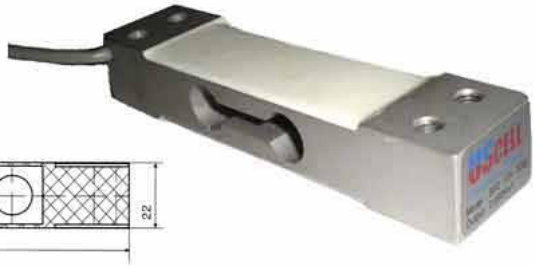


USCELL® TRANSDUCERS

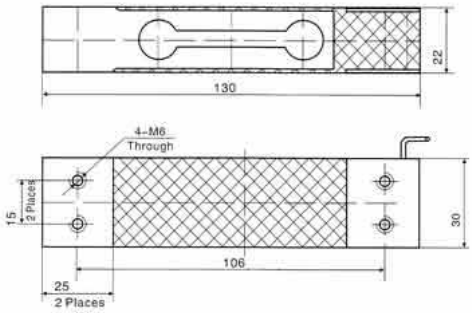
ANALOG LOAD CELL

SINGLE POINT TYPE MODEL : SP 2

ALUMINUM - ALLOY MATERIAL WITH COLORLESS ANODIZED
CAN USED FOR SMALL PLATFORM SCALE LIKE PRICING SCALE, WEIGHI
SCALE, COUNTING SCALE AND ELECTRO-MECHANIC SCALE



OUTLINE DIMENSION IN (mm)



Technical Parameter

Rated Load	3kg,6kg,8kg,10kg,15kg,20kg,30kg,40kg,50kg
Rated Output	2.0000±0.2mV/V
Total Error	±0.02%F.S
Creep(30minutes)	±0.02%F.S
Recommended Excitation Voltage	5V ~ 12V(DC)
Maximum Excitation Voltage	18V(DC)
Zero Balance	±2%F.S
Input Impedance	409±6Ω
Output Impedance	350±3Ω
Insulation Impedance	≥5000MΩ
Safe Overload	150%F.S
Ultimate Overload	200%F.S
Operating Temperature Range	(-35 ~ +65)°C
Compensated Temperature Range	(-10 ~ +40)°C
Temperature Effect On Load	±0.02%F.S/10°C
Temperature Effect On Zero	±0.02%F.S/10°C
Construction	Aluminum-Alloy
Protection Class	IP65
Citation	GB/T7551-2008/OIML R60
Mode of Connection	Input+:Red Input-:Black Output+:Green Output-:White

LCM MODULE

TINSHARP Industrial Co., Ltd.

DATA SHEET

TC1602A-01T

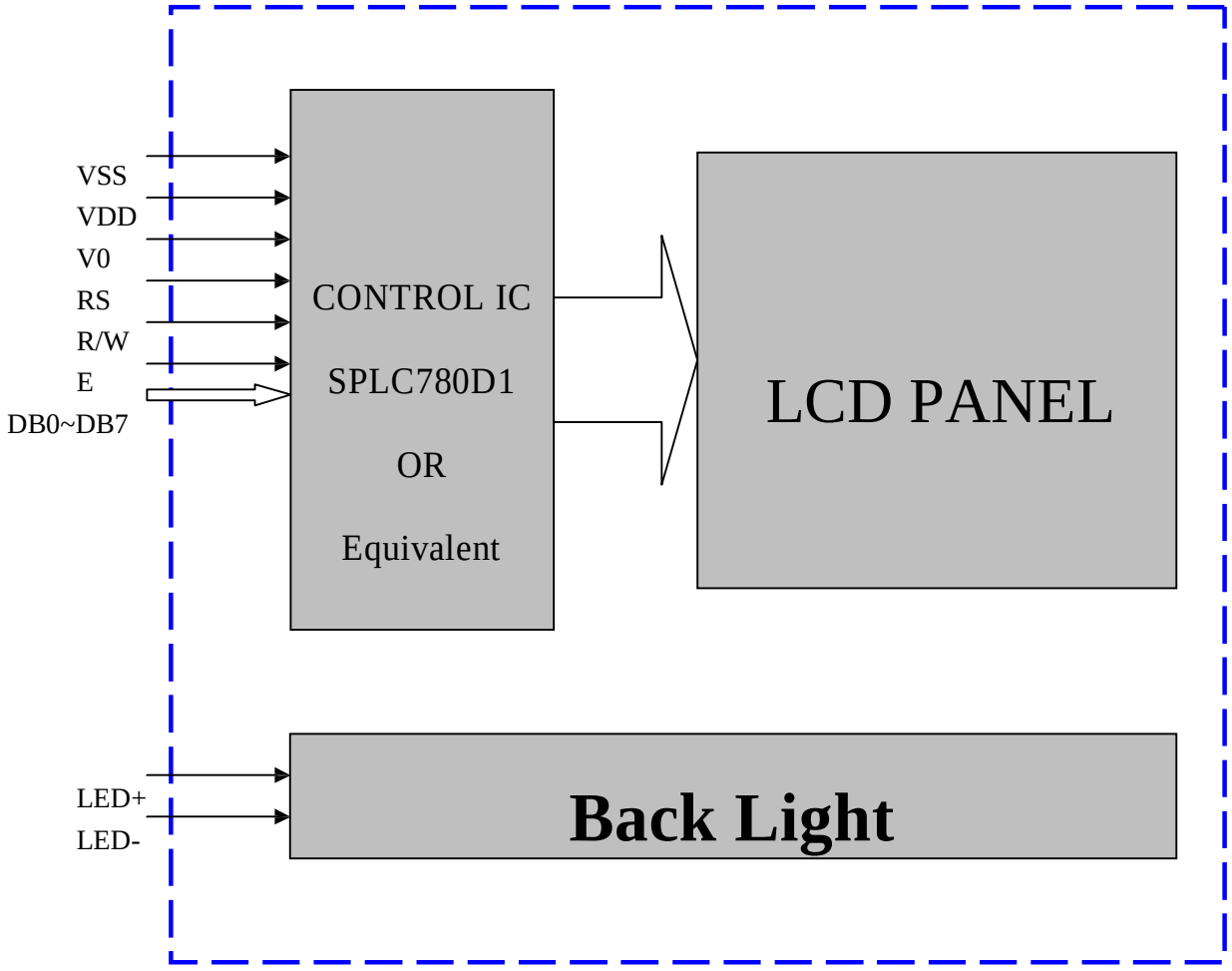
Specification for Approval

APPROVED BY	CHECKED BY	PREPARED BY

FUNCTIONS & FEATURES

- Construction : COB(Chip-on-Board)
- Display Format : 16x2 Characters
- Display Type : STN, Transflective, Positive, Y-G
- Controller : SPLC780D1 or equivalent controller
- Interface : 8-bit parallel interface
- Backlight : yellow-green\bottom lights
- Viewing Direction : 6 O'clock
- Driving Scheme : 1/16 Duty Cycle, 1/5 Bias
- Power Supply Voltage : 5.0 V
- V_{LCD} Adjustable For Best Contrast : 5.0 V (V_{OP}.)
- Operation temperature : -10℃ to +60℃
- Storage temperature : -20℃ to +70℃

BLOCK DIAGRAM



INTERFACE PIN FUNCTIONS

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground.
2	VDD	+5.0V	Power supply for logic operating.
3	V0	--	Adjusting supply voltage for LCD driving.
4	RS	H/L	A signal for selecting registers: 1: Data Register (for read and write) 0: Instruction Register (for write), Busy flag-Address Counter (for read).
5	R/W	H/L	R/W = "H":
6	E	H/L	An enable signal for writing or reading data.
7	DB0	H/L	This is an 8-bit bi-directional data bus.
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	LED+	+5.0V	Power supply for backlight.
16	LED-	0V	The backlight ground.

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Paramete	Symbol	Min	Max	Unit
Supply voltage for logic	V_{DD}	-0.3	+7.0	V
Supply voltage for LCD	V_0	0	V_{DD} +0.3	V
Input voltage	V_I	-0.3	V_{DD} +0.3	V
Normal Operating temperature	T_{OP}	-20	+70	℃
Normal Storage temperature	T_{ST}	-30	+80	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	T_{YP}	Max	Unit
Supply voltage for logic	VDD	--	4.8	5.0	5.2	V
Supply current for logic	IDD	--	--	120	150	mA
Operating voltage for LCD	VLCD	-10℃				
		25℃	4.8	5.0	5.2	V
		+60℃				
Input voltage " H " level	VIH	--	0.7 VDD	--	VDD+0.3	V
Input voltage "L" level	VIL	--	0	--	0.2VDD	V

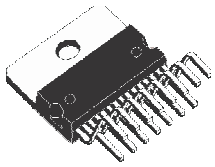
LED BACKLIGHT CHARACTERISTICS

COLOR	Wavelength λ p(nm)	Operating Voltage(± 0.15V)	Spectral line half width Δ λ (nm)	Forward Current (mA)
Yellow-green	--	4.1	--	100

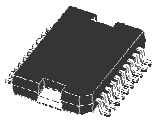
NOTE: Do not connect +5V directly to the backlight terminals. This will ruin the backlight.

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15



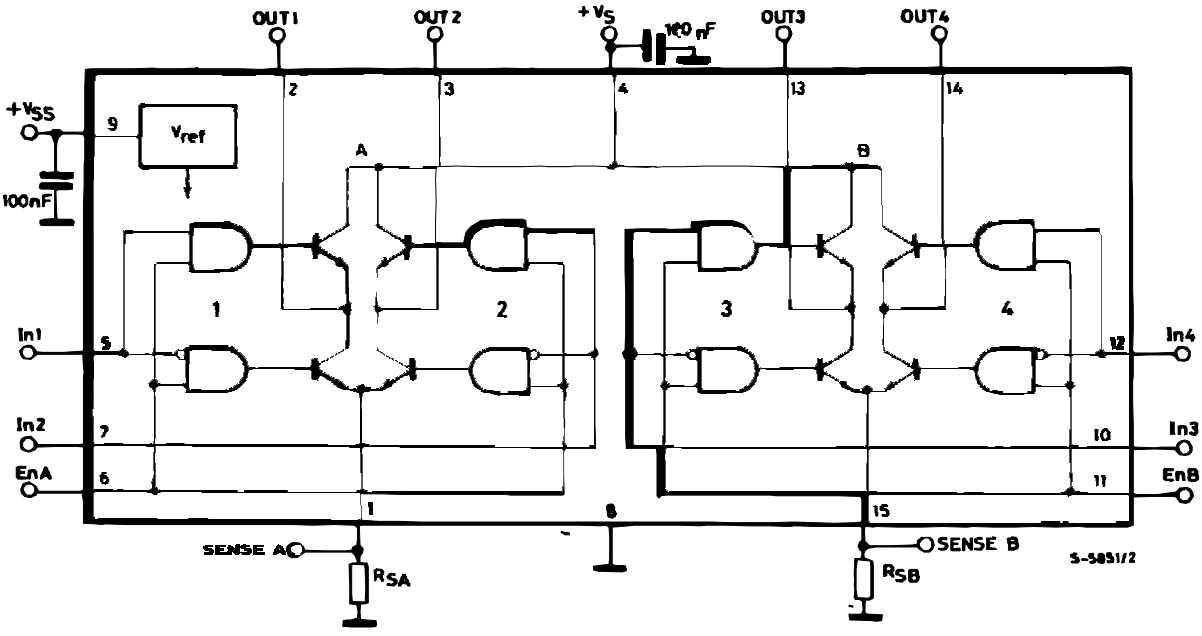
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15- lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver de-
signed to accept standard TTL logic levels and drive
inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the in- put signals. The emitters of the lower transistors of each bridge are connected together and the corre- sponding external terminal can be used for the con-
nection of anexternal sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

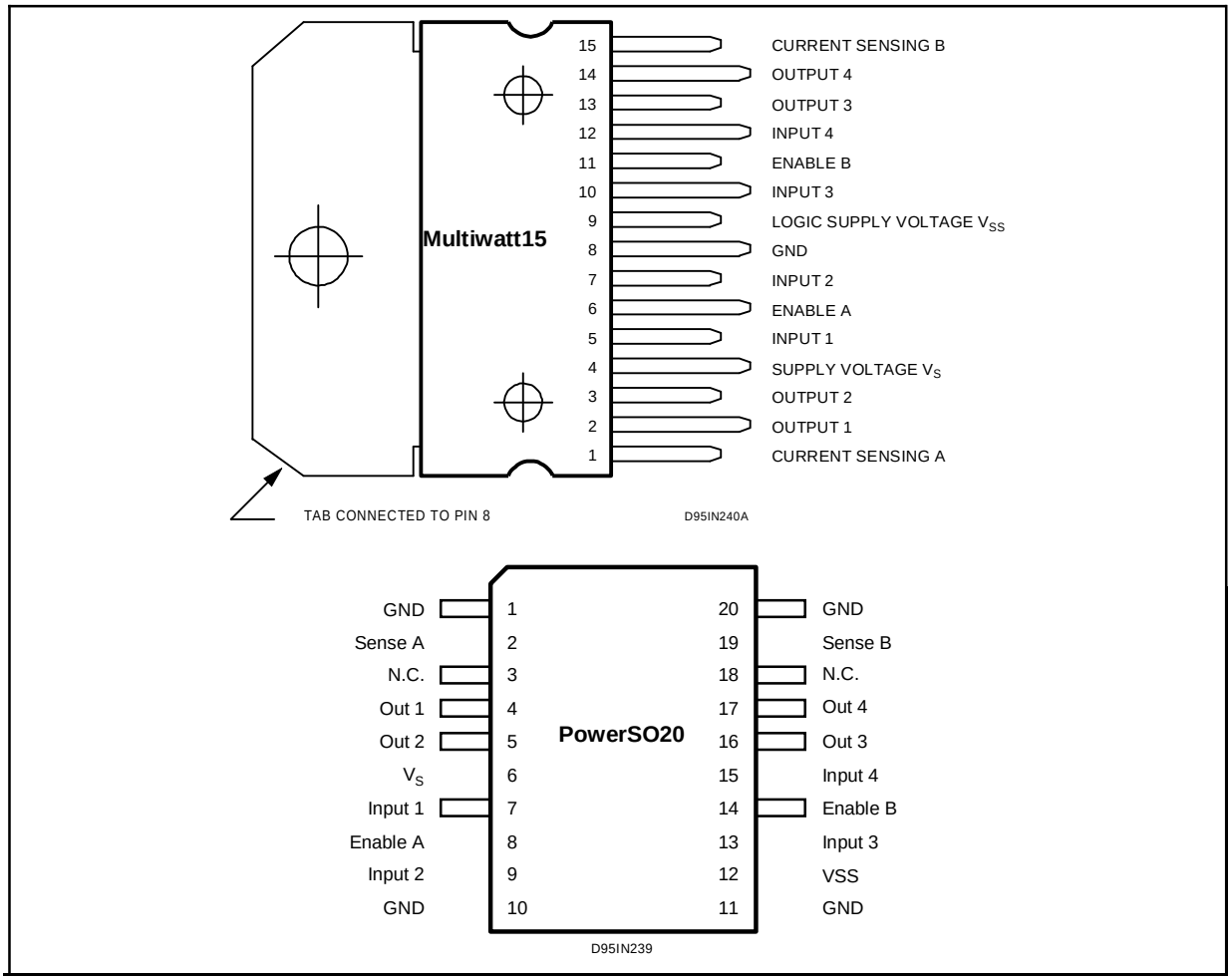
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_i,V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100 s) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75 C)	25	W
T_{op}	Junction Operating Temperature	–25 to 130	C
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25 C; unless otherwise specified)

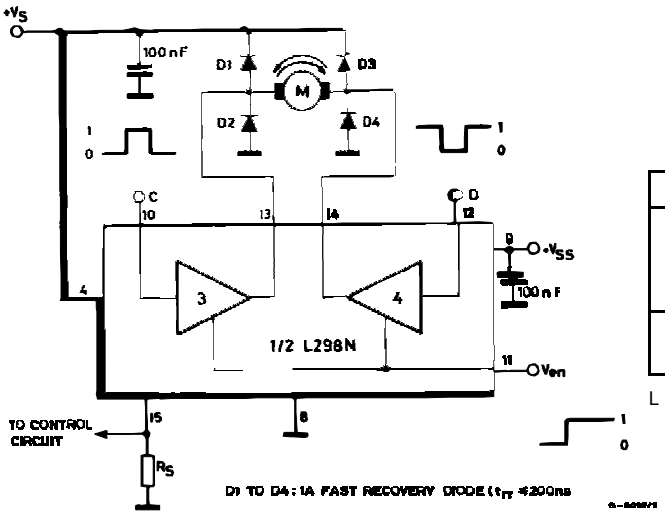
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition	V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)		4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0 V_i = L V_i = H		13 50	22 70	mA mA
		V_{en} = L V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0 V_i = L V_i = H		24 7	36 12	mA mA
		V_{en} = L V_i = X			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)		–0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)		2.3		VSS	V
I_{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L			–10	A
I_{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	Vi = H V_{SS} –0.6V		30	100	A
V_{en} = L	Enable Low Voltage (pins 6, 11)		–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)		2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L			–10	A
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H V_{SS} –0.6V		30	100	A
$V_{CEsat\ (H)}$	Source Saturation Voltage	I_L = 1A I_L = 2A	0.95	1.35 2	1.7 2.7	V V
$V_{CEsat\ (L)}$	Sink Saturation Voltage	I_L = 1A (5) I_L = 2A (5)	0.85	1.2 1.7	1.6 2.3	V V
V_{CEsat}	Total Drop	I_L = 1A (5) I_L = 2A (5)	1.80		3.2 4.9	V V
V_{sens}	Sensing Voltage (pins 1, 15)		–1 (1)		2	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_1 (V_i)	Source Current Turn-off Delay	0.5 V_i to 0.9 I_L (2); (4)		1.5		s
T_2 (V_i)	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		0.2		s
T_3 (V_i)	Source Current Turn-on Delay	0.5 V_i to 0.1 I_L (2); (4)		2		s
T_4 (V_i)	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.7		s
T_5 (V_i)	Sink Current Turn-off Delay	0.5 V_i to 0.9 I_L (3); (4)		0.7		s
T_6 (V_i)	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.25		s
T_7 (V_i)	Sink Current Turn-on Delay	0.5 V_i to 0.9 I_L (3); (4)		1.6		s
T_8 (V_i)	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.2		s
fc (V_i)	Commutation Frequency	I_L = 2A		25	40	KHz
T_1 (V_{en})	Source Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (2); (4)		3		s
T_2 (V_{en})	Source Current Fall Time	0.9 I_L to 0.1 I_L (2); (4)		1		s
T_3 (V_{en})	Source Current Turn-on Delay	0.5 V_{en} to 0.1 I_L (2); (4)		0.3		s
T_4 (V_{en})	Source Current Rise Time	0.1 I_L to 0.9 I_L (2); (4)		0.4		s
T_5 (V_{en})	Sink Current Turn-off Delay	0.5 V_{en} to 0.9 I_L (3); (4)		2.2		s
T_6 (V_{en})	Sink Current Fall Time	0.9 I_L to 0.1 I_L (3); (4)		0.35		s
T_7 (V_{en})	Sink Current Turn-on Delay	0.5 V_{en} to 0.9 I_L (3); (4)		0.25		s
T_8 (V_{en})	Sink Current Rise Time	0.1 I_L to 0.9 I_L (3); (4)		0.1		s

1) 1)Sensing voltage can be –1 V for t 50 sec; in steady state V_{sens} min – 0.5 V.
2) See fig. 2.
3) See fig. 4.
4) The load must be a pure resistor.

Figure 6 : Bidirectional DC Motor Control.



Inputs		Function
V_{en} = H	C = H ; D = L	Forward
	C = L ; D = H	Reverse
	C = D	Fast Motor Stop
V_{en} = L	C = X ; D = X	Free Running Motor Stop

L = Low H = High X = Don't care

Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 4/8/16/32K Bytes of In-System Self-Programmable Flash progam memory (ATmega48PA/88PA/168PA/328P)
  - 256/512/512/1K Bytes EEPROM (ATmega48PA/88PA/168PA/328P)
  - 512/1K/1K/2K Bytes Internal SRAM (ATmega48PA/88PA/168PA/328P)
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel 10-bit ADC in TQFP and QFN/MLF package
    Temperature Measurement
  - 6-channel 10-bit ADC in PDIP Package
    Temperature Measurement
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Byte-oriented 2-wire Serial Interface (Philips I^2C compatible)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-pin PDIP, 32-lead TQFP, 28-pad QFN/MLF and 32-pad QFN/MLF
- Operating Voltage:
  - 1.8 - 5.5V for ATmega48PA/88PA/168PA/328P
- Temperature Range:
  - -40°C to 85°C
- Speed Grade:
  - 0 - 20 MHz @ 1.8 - 5.5V
- Low Power Consumption at 1 MHz, 1.8V, 25°C for ATmega48PA/88PA/168PA/328P:
  - Active Mode: 0.2 mA
  - Power-down Mode: 0.1 µA
  - Power-save Mode: 0.75 µA (Including 32 kHz RTC)

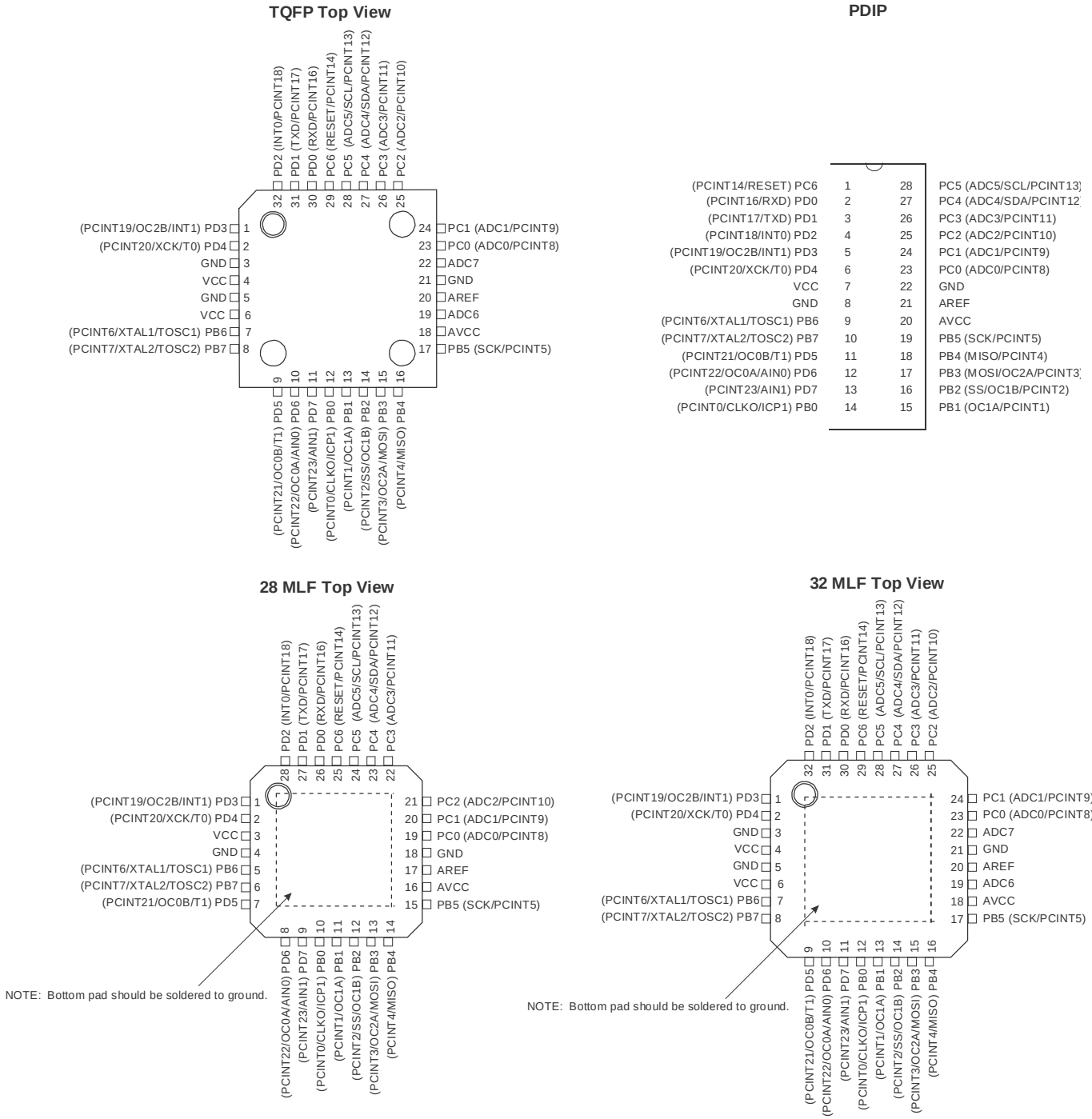
8-bit AVR® Microcontroller with 4/8/16/32K Bytes In-System Programmable Flash

ATmega48PA
ATmega88PA
ATmega168P
A
ATmega328P

Summary

1. Pin Configurations

Figure 1-1. Pinout ATmega48PA/88PA/168PA/328P



1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB7:0) XTAL1/XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in ”Alternate Functions of Port B” on page 76 and ”System Clock and Clock Options” on page 26.

1.1.4 Port C (PC5:0)

Port C is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The PC5..0 output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

1.1.5 PC6/$\overline{\text{RESET}}$

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 28-3 on page 308. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated in ”Alternate Functions of Port C” on page 79.

1.1.6 Port D (PD7:0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

The various special features of Port D are elaborated in ”Alternate Functions of Port D” on page 82.

1.1.7 AV_{CC}

AV_{CC} is the supply voltage pin for the A/D Converter, PC3:0, and ADC7:6. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that PC6..4 use digital supply voltage, V_{CC}.

1.1.8 AREF

AREF is the analog reference pin for the A/D Converter.

1.1.9 ADC7:6 (TQFP and QFN/MLF Package Only)

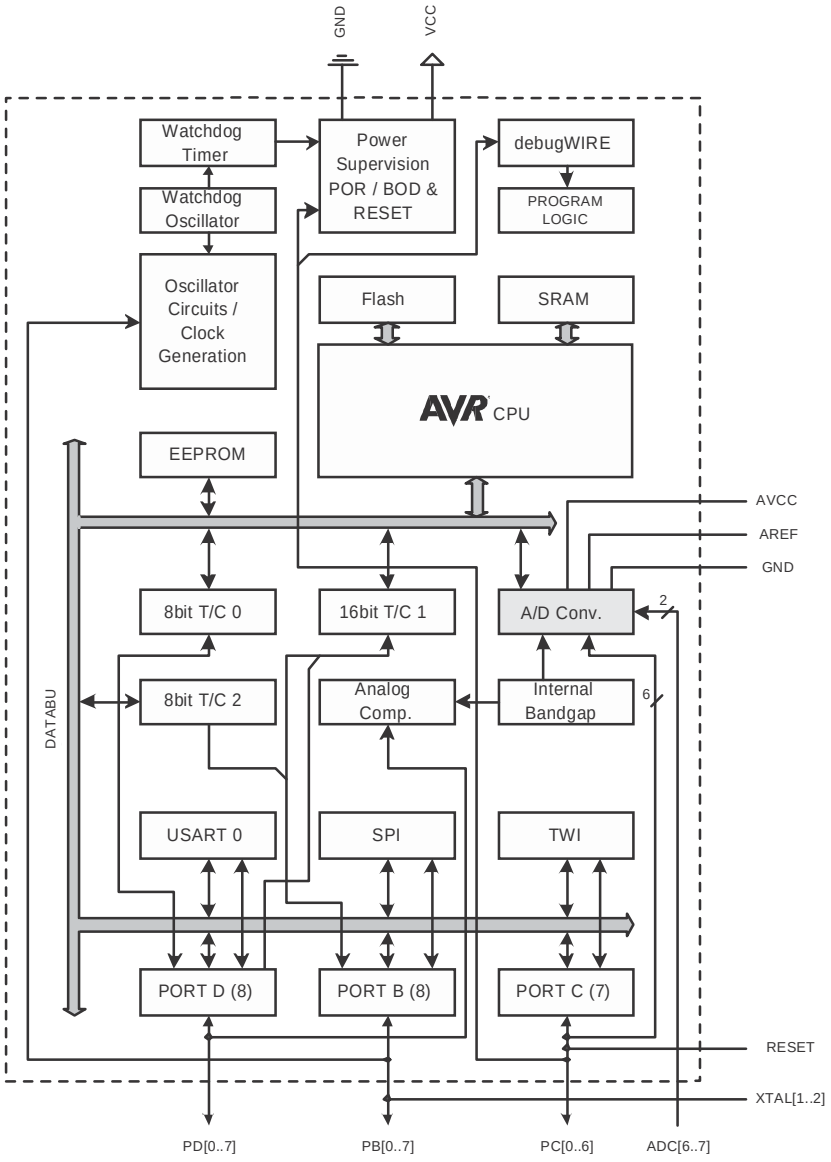
In the TQFP and QFN/MLF package, ADC7:6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

2. Overview

The ATmega48PA/88PA/168PA/328P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega48PA/88PA/168PA/328P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent

architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega48PA/88PA/168PA/328P provides the following features: 4/8/16/32K bytes of In-System Programmable Flash with Read-While-Write capabilities, 256/512/512/1K bytes EEPROM, 512/1K/1K/2K bytes SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte-oriented 2-wire Serial Interface, an SPI serial port, a 6-channel 10-bit ADC (8 channels in TQFP and QFN/MLF packages), a programmable Watchdog Timer with internal Oscillator, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, USART, 2-wire Serial Inter- face, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next inter- rupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduc- tion mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot pro- gram running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega48PA/88PA/168PA/328P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega48PA/88PA/168PA/328P AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2.2 Comparison Between ATmega48PA, ATmega88PA, ATmega168PA and ATmega328P

The ATmega48PA, ATmega88PA, ATmega168PA and ATmega328P differ only in memory sizes, boot loader support, and interrupt vector sizes. Table 2-1 summarizes the different memory and interrupt vector sizes for the three devices.

Table 2-1. Memory Size Summary

Device	Flash	EEPROM	RAM	Interrupt Vector Size
ATmega48PA	4K Bytes	256 Bytes	512 Bytes	1 instruction word/vector
ATmega88PA	8K Bytes	512 Bytes	1K Bytes	1 instruction word/vector
ATmega168PA	16K Bytes	512 Bytes	1K Bytes	2 instruction words/vector
ATmega328P	32K Bytes	1K Bytes	2K Bytes	2 instruction words/vector

ATmega88PA, ATmega168PA and ATmega328P support a real Read-While-Write Self-Programming mechanism. There is a separate Boot Loader Section, and the SPM instruction can only execute from there. In ATmega48PA, there is no Read-While-Write support and no sepa-

rate Boot Loader Section. The SPM instruction can execute from the entire Flash.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.