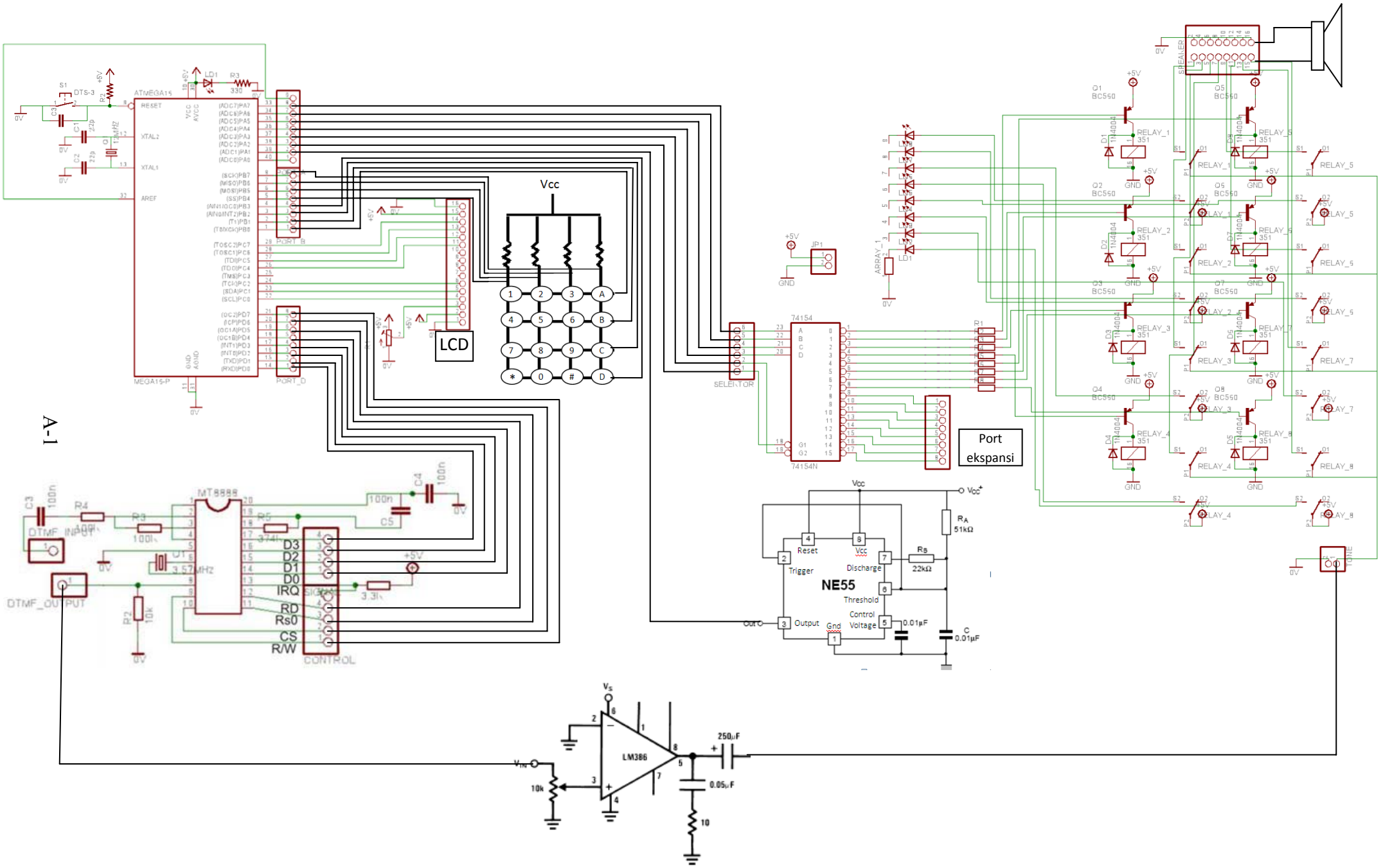
LAMPIRAN A

RANGKAIAN


ATMEGA15
MEGA15-P
PORT_B
PORT_D
LCD
Vcc
SELEKTOR
74154
74154N
Port ekspansi
MT8888
DTMF_INPUT
DTMF_OUTPUT
CONTROL
D3
D2
D1
D0
IRQ
RD
Rs0
CS
R/W
NE55
Trigger
Reset
Discharge
Threshold
Control Voltage
Output
Gnd
LM386
A-1

LAMPIRAN B

PROGRAM

```
/*****************************************************
This program was produced by the
CodeWizardAVR V1.25.3 Professional
Automatic Program Generator
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http://www.hpinfotech.com

Project :
Version :
Date    : 11/25/2009
Author  : Edwin
Company : Bonzo
Comments:

Chip type           : ATmega16
Program type        : Application
Clock frequency     : 16.000000 MHz
Memory model        : Small
External SRAM size  : 0
Data Stack size     : 256
*****************************************************/
#include <mega16.h>
#include <delay.h>
#include <stdio.h>

// Alphanumeric LCD Module functions
#asm
  .equ __lcd_port=0x15 ;PORTC
#endasm
#include <lcd.h>

int del;

#define PORT PORTD
#define d3 PORT.0
#define d2 PORT.1
#define d1 PORT.2
#define d0 PORT.3
#define wr PORT.7
#define cs PORT.6
#define rs0 PORT.5
#define rd PORT.4
#define delay delay_ms(del)

#define telkomsel 0x00
#define indosat 0x04
#define xl 0x08
#define axis 0x0C
#define three 0x10
#define cdma_roaming 0x14
```

```
#define cdma_lokal 0x18
#define tlp_rmh 0x1C

// Declare your global variables here

char text[30];
char keypressed;
char no_tlp[12]  ;
int i,j,k;
int dial[12],cal_tone,hitung;

void no_line(void)
{lcd_clear();
lcd_putsf("Maaf, Saluran");
lcd_gotoxy(0,1);
lcd_putsf("tidak terhubung");
delay_ms(3000);
i=0; no_tlp[0]=' ';no_tlp[1]=' ';no_tlp[2]=' ';no_tlp[3]=' ';no_tlp[4]=' ';no_tlp[5]='
';no_tlp[6]=' ';no_tlp[7]=' ';no_tlp[8]=' ';no_tlp[9]=' ';no_tlp[10]=' ';no_tlp[11]=' ';
dial[0]=0;dial[1]=0;dial[2]=0;dial[3]=0;dial[4]=0;dial[5]=0;dial[6]=0;dial[7]=0;dial[8]=0;dia
l[9]=0;dial[10]=0;dial[11]=0;k=0;
}

void out (char output)
{
DDRD=255;
wr=1;rd=1;rs0=1;cs=0;

if(output==1)
{d0=1;d1=0;d2=0;d3=1;}
else
{d0=0;d1=0;d2=0;d3=1;}

wr=0;
delay_us(1);
wr=1;
delay_us(1);

if(output==1)
{d0=1;d1=0;d2=0;d3=0;}
else
{d0=0;d1=0;d2=0;d3=0;}

wr=0;
delay_us(1);
wr=1;
delay_us(1);

}
```

```
void dtmf (char input)
{
        DDRD=0xFF;
        rd=1;
        wr=1;
        cs=0;
        rs0=0;
        delay_us(1);

        switch(input)
        {
        case 1:  d3=0;d2=0;d1=0;d0=1;break;
        case 2:  d3=0;d2=0;d1=1;d0=0;break;
        case 3:  d3=0;d2=0;d1=1;d0=1;break;
        case 4:  d3=0;d2=1;d1=0;d0=0;break;
        case 5:  d3=0;d2=1;d1=0;d0=1;break;
        case 6:  d3=0;d2=1;d1=1;d0=0;break;
        case 7:  d3=0;d2=1;d1=1;d0=1;break;
        case 8:  d3=1;d2=0;d1=0;d0=0;break;
        case 9:  d3=1;d2=0;d1=0;d0=1;break;
        case 0:  d3=1;d2=0;d1=1;d0=0;break;
        case '*':d3=1;d2=0;d1=1;d0=1;break;
        case '#':d3=1;d2=1;d1=0;d0=0;break;
        case 'a':d3=1;d2=1;d1=0;d0=1;break;
        case 'b':d3=1;d2=1;d1=1;d0=0;break;
        case 'c':d3=1;d2=1;d1=1;d0=1;break;
        case 'd':d3=0;d2=0;d1=0;d0=0;break;
        }

        wr=0;
        delay_us(1);
        wr=1;
        delay_us(1);

}

void tone (void)
{
cal_tone=0;
hitung=0;
DDRA.1=0;
PORTA.1=1;

periksa1:
if (PINA.1==0)
goto periksa2;
goto periksa1;

periksa2:
if (PINA.1==1)
```

```
{hitung=0;
goto periksa3;}
else
{hitung=hitung+1;
delay_us(1);
if (hitung<2000)
{goto periksa2;}
else
{no_line();}
}

periksa3:
if (PINA.1==0)
goto periksa4;
cal_tone=cal_tone+1;
goto periksa3;

periksa4:
if (cal_tone<1500 && cal_tone>1000)
{goto tone_panggil;}
else
{no_line();}

tone_panggil:
del=200;
for (j=0;j<i;j++)
{
out(1);dtmf(dial[j]);delay;out(0);delay;
}
PORTA=0xFC;
delay_ms(5);
i=0; no_tlp[0]=' ';no_tlp[1]=' ';no_tlp[2]=' ';no_tlp[3]=' ';no_tlp[4]=' ';no_tlp[5]='
';no_tlp[6]=' ';no_tlp[7]=' ';no_tlp[8]=' ';no_tlp[9]=' ';no_tlp[10]=' ';no_tlp[11]=' ';
dial[0]=0;dial[1]=0;dial[2]=0;dial[3]=0;dial[4]=0;dial[5]=0;dial[6]=0;dial[7]=0;dial[8]=0;dia
l[9]=0;dial[10]=0;dial[11]=0;k=0;
}

void selektor (void)
{
if (i>=10 && i<=12 && no_tlp[0]=='0' && no_tlp[1]=='8' )
{
 if (no_tlp[2]=='1')
 {
   if (no_tlp[3]=='7'|| no_tlp[3]=='8'||no_tlp[3]=='9')
   {
    lcd_gotoxy(0,1);
    lcd_putsf("XL");
    PORTA=xl;
    delay_ms(5);
    tone();     }
```

```
  if (no_tlp[3]=='5'||no_tlp[3]=='6')
  {
   lcd_gotoxy(0,1);
   lcd_putsf("Mentari");
   PORTA=indosat;
   delay_ms(5);
   tone();
  }
  if (no_tlp[3]=='1'||no_tlp[3]=='2'||no_tlp[3]=='3')
  {
   lcd_gotoxy(0,1);
   lcd_putsf("Telkomsel");
   PORTA=telkomsel;
   delay_ms(5);
   tone();
  }
 }
if (no_tlp[2]=='3')
{
 if (no_tlp[3]=='8')
 {
  lcd_gotoxy(0,1);
  lcd_putsf("Axis");
  PORTA=axis;
  delay_ms(5);
  tone();
 }
}
if (no_tlp[2]=='5')
{
 if (no_tlp[3]=='5'||no_tlp[3]=='6'||no_tlp[3]=='7'||no_tlp[3]=='8')
 {
  lcd_gotoxy(0,1);
  lcd_putsf("Indosat");
  PORTA=indosat;
  delay_ms(5);
  tone();
 }
 if (no_tlp[3]=='2'||no_tlp[3]=='3')
 {
  lcd_gotoxy(0,1);
  lcd_putsf("AS");
  PORTA=telkomsel;
  delay_ms(5);
  tone();
 }
}
if (no_tlp[2]=='7')
{
 if (no_tlp[3]=='7'||no_tlp[3]=='8')
```

```
 {
  lcd_gotoxy(0,1);
  lcd_putsf("XL");
  PORTA=xl;
  delay_ms(5);
  tone();
 }
}
if (no_tlp[2]=='8')
{
 if (no_tlp[3]=='8'||no_tlp[3]=='9')
 {
  lcd_gotoxy(0,1);
  lcd_putsf("Fren");
  PORTA=cdma_roaming;
  delay_ms(5);
  tone();
 }
 if (no_tlp[3]=='2')
 {
  lcd_gotoxy(0,1);
  lcd_putsf("Smart");
  PORTA=cdma_roaming;
  delay_ms(5);
  tone();
 }
}
if (no_tlp[2]=='9')
{
 if (no_tlp[3]=='6'||no_tlp[3]=='8')
 {
  lcd_gotoxy(0,1);
  lcd_putsf("Three");
  PORTA=three;
  delay_ms(5);
  tone();
 }
 }
}
if (i==8)
{
 if (no_tlp[0]=='2')
 {
  lcd_gotoxy(0,1);
  lcd_putsf("Hepi");
  PORTA=cdma_lokal;
  delay_ms(5);
  tone();
 }
 if (no_tlp[0]=='3')
```

```
{
 lcd_gotoxy(0,1);
 lcd_putsf("Star One");
 PORTA=cdma_lokal;
 delay_ms(5);
 tone();
}
if (no_tlp[0]=='7')
{
 lcd_gotoxy(0,1);
 lcd_putsf("Flexi");
 PORTA=cdma_lokal;
 delay_ms(5);
 tone();
}
if (no_tlp[0]=='9')
{
 lcd_gotoxy(0,1);
 lcd_putsf("Esia");
 PORTA=cdma_lokal;
 delay_ms(5);
 tone();
}
}
if (i==7)
{lcd_gotoxy(0,1);
 lcd_putsf("Tlp Rumah");
 PORTA=tlp_rmh;
 delay_ms(5);
 tone();
}
if (i>=3 && i<=12)
{lcd_gotoxy(0,1);
 lcd_putsf("other");
 PORTA=tlp_rmh;
 delay_ms(5);
 tone();
}
else
{
i=0;
no_tlp[0]=' ';no_tlp[1]=' ';no_tlp[2]=' ';no_tlp[3]=' ';no_tlp[4]=' ';no_tlp[5]=' ';no_tlp[6]='
';no_tlp[7]=' ';no_tlp[8]=' ';no_tlp[9]=' ';no_tlp[10]=' ';no_tlp[11]=' ';
dial[0]=0;dial[1]=0;dial[2]=0;dial[3]=0;dial[4]=0;dial[5]=0;dial[6]=0;dial[7]=0;dial[8]=0;dia
l[9]=0;dial[10]=0;dial[11]=0;
}
 }
```

```
char scan_keypadB_rev(void)
{
int scankey;
unsigned char keypressed=0;
char temp;
temp=PORTB;
DDRB = 0x0F;
PORTB = 0xFE;
delay_us(1);
scankey = PINB&0xf0;
k=k+1;
if(k<30)
{
switch (scankey)
  {
   case 0xE0 : PORTA=0xD1;delay_ms(1);keypressed = 1;
del=200;out(1);dtmf(1);delay;out(0);delay; no_tlp[i]='1';dial[i]=1;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0xD0 : PORTA=0xD1;delay_ms(1);keypressed = 2;
del=200;out(1);dtmf(2);delay;out(0);delay; no_tlp[i]='2';dial[i]=2;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0xB0 : PORTA=0xD1;delay_ms(1);keypressed = 3;
del=200;out(1);dtmf(3);delay;out(0);delay; no_tlp[i]='3';dial[i]=3;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0x70 : keypressed = 'A';  break;
   }
cek1:
scankey = PINB&0xf0; delay_us(1);
switch (scankey)
{
case 0xf0:  goto lanjut2;
default: goto cek1;
}
lanjut2:

   PORTB = 0xFD;
   delay_us(1);
scankey = PINB&0xf0;
switch (scankey)
  {
   case 0xE0 : PORTA=0xD1;delay_ms(1);keypressed = 4;
del=200;out(1);dtmf(4);delay;out(0);delay;  no_tlp[i]='4';dial[i]=4;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0xD0 : PORTA=0xD1;delay_ms(1);keypressed = 5;
del=200;out(1);dtmf(5);delay;out(0);delay;  no_tlp[i]='5';dial[i]=5;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0xB0 : PORTA=0xD1;delay_ms(1);keypressed = 6;
del=200;out(1);dtmf(6);delay;out(0);delay;  no_tlp[i]='6';dial[i]=6;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0x70 : keypressed = 'B'; selektor();k=0;  break;
```

```
   }
cek2:
scankey = PINB&0xf0; delay_us(1);
switch (scankey)
{
case 0xf0:  goto lanjut3;
default: goto cek2;
}
lanjut3:

   PORTB = 0xFB;
   delay_us(1);
   scankey = PINB&0xf0;
switch (scankey)
  {
   case 0xE0 : PORTA=0xD1;delay_ms(1);keypressed = 7;
del=200;out(1);dtmf(7);delay;out(0);delay;  no_tlp[i]='7';dial[i]=7;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0xD0 : PORTA=0xD1;delay_ms(1);keypressed = 8;
del=200;out(1);dtmf(8);delay;out(0);delay;  no_tlp[i]='8';dial[i]=8;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0xB0 : PORTA=0xD1;delay_ms(1);keypressed = 9;
del=200;out(1);dtmf(9);delay;out(0);delay;  no_tlp[i]='9';dial[i]=9;
i++;k=0;PORTA=0xD0;delay_ms(1);break;
   case 0x70 : keypressed = 'C';
   i=0; no_tlp[0]=' ';no_tlp[1]=' ';no_tlp[2]=' ';no_tlp[3]=' ';no_tlp[4]=' ';no_tlp[5]='
';no_tlp[6]=' ';no_tlp[7]=' ';no_tlp[8]=' ';no_tlp[9]=' ';no_tlp[10]=' ';no_tlp[11]=' ';

dial[0]=0;dial[1]=0;dial[2]=0;dial[3]=0;dial[4]=0;dial[5]=0;dial[6]=0;dial[7]=0;dial[8]=0;dia
l[9]=0;dial[10]=0;dial[11]=0;k=0;
    break;
   }
cek3:
scankey = PINB&0xf0; delay_us(1);
switch (scankey)
{
case 0xf0:  goto lanjut4;
default: goto cek3;
}
lanjut4:

   PORTB = 0xF7;
   delay_us(1);
   scankey = PINB&0xf0;
switch (scankey)
  {
   case 0xE0 : PORTA=0xD1;delay_ms(1);keypressed = '*';
del=200;out(1);dtmf('*');delay;out(0);delay; no_tlp[i]='*';dial[i]='*'; i++;
k=0;PORTA=0xD0;delay_ms(1);break;
```

```
   case 0xD0 : PORTA=0xD1;delay_ms(1);keypressed = '0';
del=200;out(1);dtmf(0);delay;out(0);delay; no_tlp[i]='0';dial[i]=0; i++;
k=0;PORTA=0xD0;delay_ms(1);break;
   case 0xB0 : PORTA=0xD1;delay_ms(1);keypressed = '#';
del=200;out(1);dtmf('#');delay;out(0);delay; no_tlp[i]='#';dial[i]='#'; i++;
k=0;PORTA=0xD0;delay_ms(1);break;
   case 0x70 : keypressed = 'D'; i=i-1; no_tlp[i]=' ';k=0; break;
   }

cek4:
scankey = PINB&0xf0; delay_us(1);
switch (scankey)
{
case 0xf0: goto lanjut5;
default: goto cek4;
}
lanjut5:
 return keypressed;
 }
 else
 {k=0;
 selektor();
 //tone();
  }
  }

void main(void)
{
// Declare your local variables here

// Input/Output Ports initialization
// Port A initialization
// Func7=Out Func6=Out Func5=Out Func4=Out Func3=Out Func2=Out Func1=Out
Func0=Out
// State7=0 State6=0 State5=0 State4=0 State3=0 State2=0 State1=0 State0=0
PORTA=0b11000000;
DDRA=0xFF;

// Port B initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTB=0x00;
DDRB=0x00;

// Port C initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTC=0x00;
DDRC=0x00;
```

```
// Port D initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTD=0x00;
DDRD=0x00;

// Timer/Counter 0 initialization
// Clock source: System Clock
// Clock value: Timer 0 Stopped
// Mode: Normal top=FFh
// OC0 output: Disconnected
TCCR0=0x00;
TCNT0=0x00;
OCR0=0x00;

// Timer/Counter 1 initialization
// Clock source: System Clock
// Clock value: Timer 1 Stopped
// Mode: Normal top=FFFFh
// OC1A output: Discon.
// OC1B output: Discon.
// Noise Canceler: Off
// Input Capture on Falling Edge
// Timer 1 Overflow Interrupt: Off
// Input Capture Interrupt: Off
// Compare A Match Interrupt: Off
// Compare B Match Interrupt: Off
TCCR1A=0x00;
TCCR1B=0x00;
TCNT1H=0x00;
TCNT1L=0x00;
ICR1H=0x00;
ICR1L=0x00;
OCR1AH=0x00;
OCR1AL=0x00;
OCR1BH=0x00;
OCR1BL=0x00;

// Timer/Counter 2 initialization
// Clock source: System Clock
// Clock value: Timer 2 Stopped
// Mode: Normal top=FFh
// OC2 output: Disconnected
ASSR=0x00;
TCCR2=0x00;
TCNT2=0x00;
OCR2=0x00;

// External Interrupt(s) initialization
// INT0: Off
```

```
// INT1: Off
// INT2: Off
MCUCR=0x00;
MCUCSR=0x00;

// Timer(s)/Counter(s) Interrupt(s) initialization
TIMSK=0x00;

// Analog Comparator initialization
// Analog Comparator: Off
// Analog Comparator Input Capture by Timer/Counter 1: Off
ACSR=0x80;
SFIOR=0x00;

// LCD module initialization
lcd_init(16);
 k=0;

while (1)
    {
    // Place your code here
 if (i<1)
 {lcd_clear();
 lcd_putsf("Masukan Nomor yg");
 lcd_gotoxy(0,1);
 lcd_putsf("Dituju");
 delay_ms(250);
}
 else
 {
 lcd_clear();

sprintf(text,"%c%c%c%c%c%c%c%c%c%c%c%c",no_tlp[0],no_tlp[1],no_tlp[2],no_tlp[3],
no_tlp[4],no_tlp[5],no_tlp[6],no_tlp[7],no_tlp[8],no_tlp[9],no_tlp[10],no_tlp[11]);
 lcd_puts(text);
 delay_ms(100);
  }
 scan_keypadB_rev();
          };
 }
```

LAMPIRAN C

DATASHEET ATMEGA 16

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 16K Bytes of In-System Self-programmable Flash program memory
  - 512 Bytes EEPROM
  - 1K Byte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    - 8 Single-ended Channels
    - 7 Differential Channels in TQFP Package Only
    - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, and 44-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega16L
  - 4.5 - 5.5V for ATmega16
- Speed Grades
  - 0 - 8 MHz for ATmega16L
  - 0 - 16 MHz for ATmega16
- Power Consumption @ 1 MHz, 3V, and 25°C for ATmega16L
  - Active: 1.1 mA
  - Idle Mode: 0.35 mA
  - Power-down Mode: < 1 µA

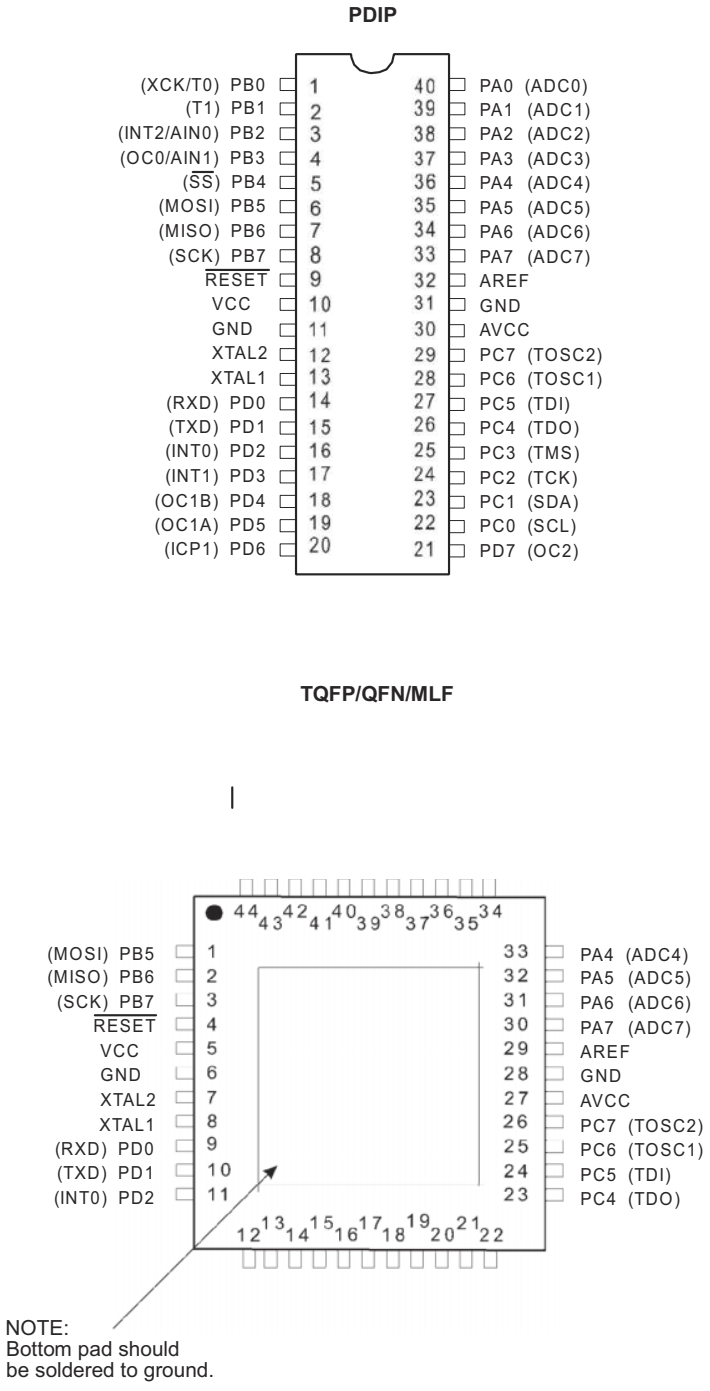
8-bit AVR® Microcontroller with 16K Bytes In-System Programmable Flash

ATmega16
ATmega16L

Summary

Pin Configurations

Figure 1. Pinout ATmega16



Disclaimer

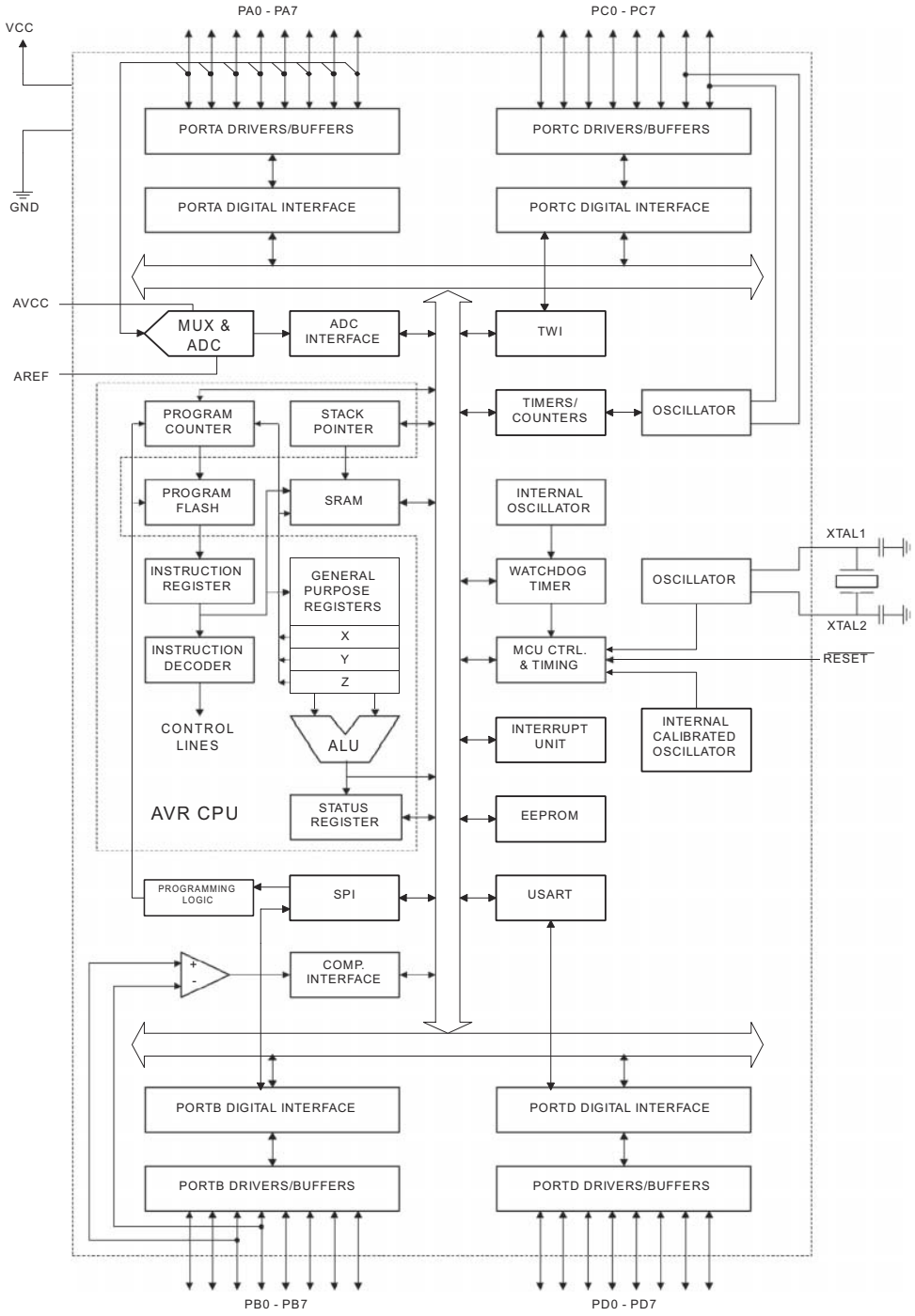
Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Overview

The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega16 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega16 provides the following features: 16K bytes of In-System Programmable Flash Program memory with Read-While-Write capabilities, 512 bytes EEPROM, 1K byte SRAM, 32 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, Internal and External Interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain (TQFP package only), a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the USART, Two-wire interface, A/D Converter, SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next External Interrupt or Hardware Reset. In Power-save mode, the Asynchronous Timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega16 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega16 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC Digital supply voltage.

GND Ground.

Port A (PA7..PA0) Port A serves as the analog inputs to the A/D Converter.

Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B (PB7..PB0) Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega16 as listed on page 58.

Port C (PC7..PC0) Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PC5(TDI), PC3(TMS) and PC2(TCK) will be activated even if a reset occurs.

Port C also serves the functions of the JTAG interface and other special features of the ATmega16 as listed on page 61.

Port D (PD7..PD0) Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega16 as listed on page 63.

$\overline{\text{RESET}}$ Reset Input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a reset.

XTAL1 Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2 Output from the inverting Oscillator amplifier.

AVCC AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

AREF AREF is the analog reference pin for the A/D Converter.

LAMPIRAN D

DATASHEET MT8888

MT8888C/MT8888C-1

Integrated DTMF Transceiver with Intel Micro Interface

ISSUE 2 May 1995

Features

- Central office quality DTMF transmitter/receiver
- Low power consumption
- High speed Intel micro interface
- Adjustable guard time
- Automatic tone burst mode
- Call progress tone detection to -30dBm

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Description

The MT8888C is a monolithic DTMF transceiver with call progress filter. It is fabricated in CMOS technology offering low power consumption and high reliability.

Ordering Information

MT8888CE/CE-1	20 Pin Plastic DIP
MT8888CC/CC-1	20 Pin Ceramic DIP
MT8888CS/CS-1	20 Pin SOIC
MT8888CN/CN-1	24 Pin SSOP

-40°C to +85°C

The receiver section is based upon the industry standard MT8870 DTMF receiver while the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones.

The MT8888C utilizes an Intel micro interface, which allows the device to be connected to a number of popular microcontrollers with minimal external logic. The MT8888C-1 is functionally identical to the MT8888C except the receiver is enhanced to accept lower level signals, and also has a specified low signal rejection level.

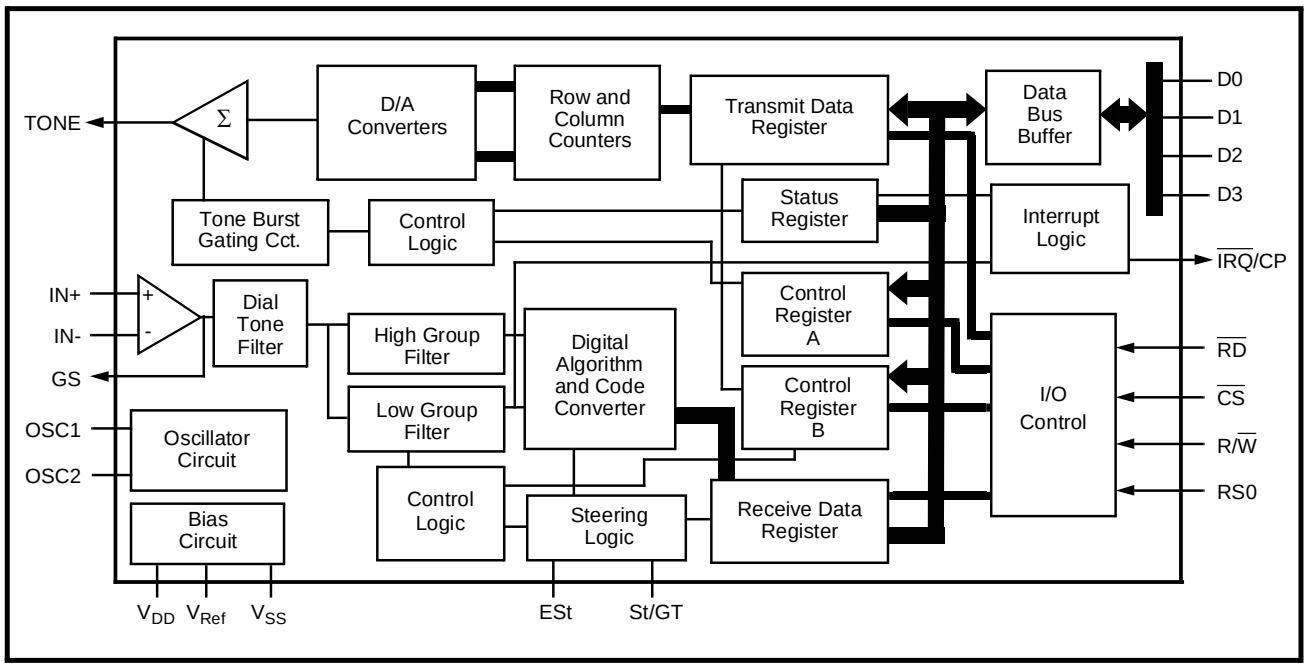


Figure 1 - Functional Block Diagram

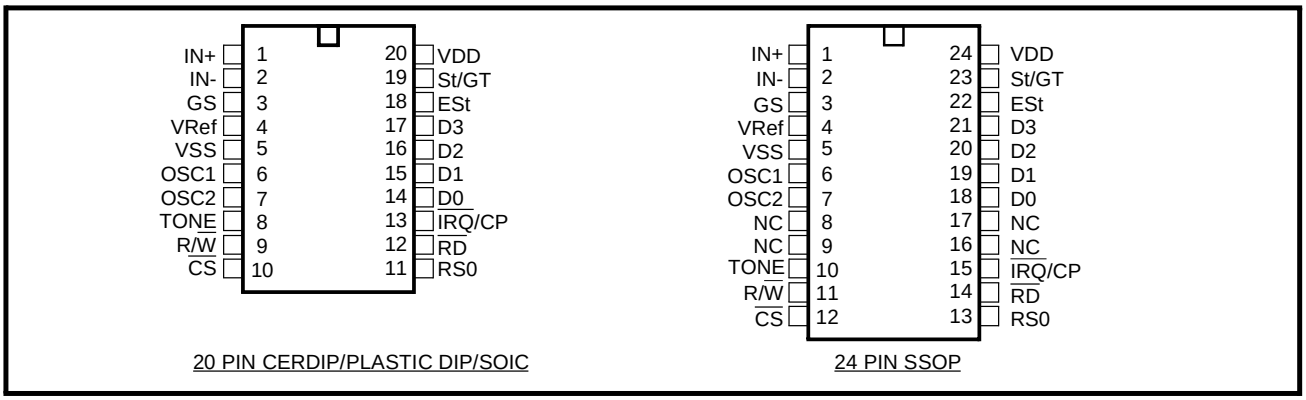


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
20	24		
1	1	IN+	**Non-inverting** op-amp input.
2	2	IN-	**Inverting** op-amp input.
3	3	GS	**Gain Select**. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage** output (V_{DD}/2).
5	5	V_{SS}	Ground (0V).
6	6	OSC1	**Oscillator** input. This pin can also be driven directly by an external clock.
7	7	OSC2	**Oscillator** output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is driven externally.
8	10	TONE	Output from internal DTMF transmitter.
9	11	$\overline{WR}$	**$\overline{Write}$** microprocessor input. TTL compatible.
10	12	$\overline{CS}$	**Chip Select** input. Active Low. This signal must be qualified externally by address latch enable (ALE) signal, see Figure 12.
11	13	RS0	**Register Select** input. Refer to Table 3 for bit interpretation. TTL compatible.
12	14	$\overline{RD}$	**$\overline{Read}$** microprocessor input. TTL compatible.
13	15	$\overline{IRQ}$/ CP	**Interrupt Request/Call Progress** (open drain) output. In interrupt mode, this output goes low when a valid DTMF tone burst has been transmitted or received. In call progress mode, this pin will output a rectangular signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter, see Figure 8.
14-17	18-21	D0-D3	Microprocessor Data Bus. High impedance when $\overline{CS}$ = 1 or $\overline{RD}$ = 1. TTL compatible.
18	22	ESt	**Early Steering** output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	23	St/GT	**Steering Input/Guard Time** output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	24	V_{DD}	Positive power supply (5V typ.).
	8,9 16,17	NC	No Connection.

Functional Description

The MT8888C/MT8888C-1 Integrated DTMF Transceiver consists of a high performance DTMF receiver with an internal gain setting amplifier and a DTMF generator which employs a burst counter to synthesize precise tone bursts and pauses. A call progress mode can be selected so that frequencies within the specified passband can be detected. The Intel micro interface allows microcontrollers, such as the 8080, 80C31/51 and 8085, to access the MT8888C/MT8888C-1 internal registers.

Input Configuration

The input arrangement of the MT8888C/MT8888C-1 provides a differential-input operational amplifier as well as a bias source (V_{Ref}), which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment. In a single-ended configuration, the input pins are connected as shown in Figure 3.

Figure 4 shows the necessary connections for a differential input configuration.

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Table 1). These filters incorporate notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section, which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

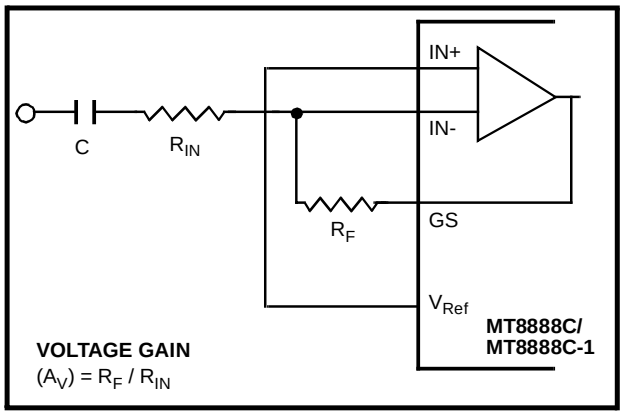


Figure 3 - Single-Ended Input Configuration

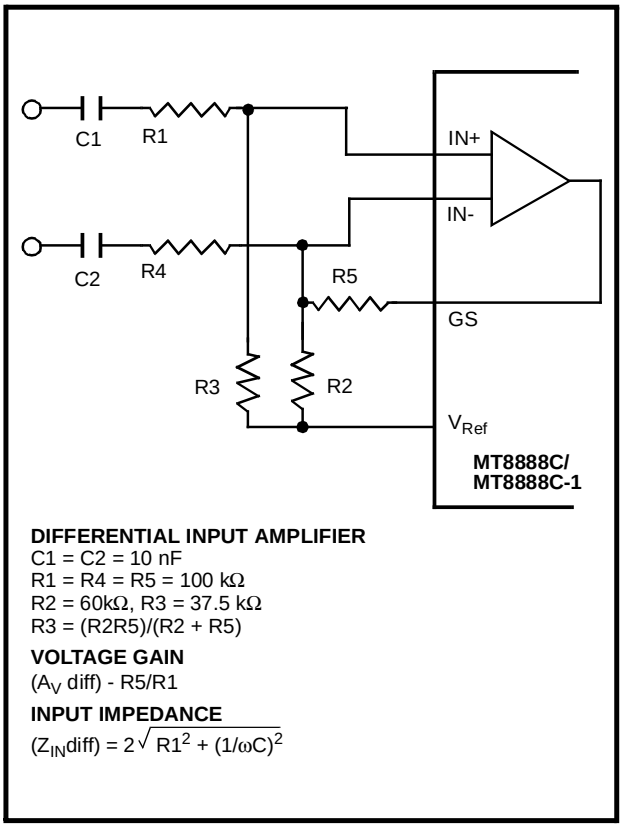


Figure 4 - Differential Input Configuration

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0= LOGIC LOW, 1= LOGIC HIGH

Table 1. Functional Encode/Decode Table

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 5) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. The status of the delayed steering flag can be monitored by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bidirectional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

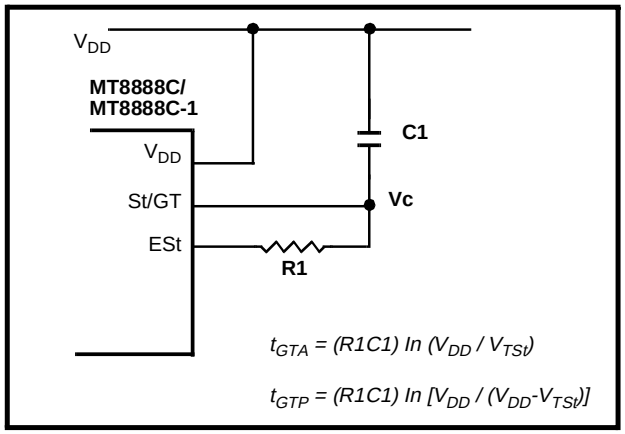


Figure 5 - Basic Steering Circuit

Guard Time Adjustment

The simple steering circuit shown in Figure 5 is adequate for most applications. Component values are chosen according to the following inequalities (see Figure 7):

$$t_{REC} \geq t_{DPmax}+t_{GTPmax} - t_{DAmin}$$
$$t_{\overline{REC}} \leq t_{DPmin}+t_{GTPmin} - t_{DAmax}$$
$$t_{ID} \geq t_{DAmax}+t_{GTAmax} - t_{DPmin}$$
$$t_{DO} \leq t_{DAmin}+t_{GTAmin} - t_{DPmax}$$

The value of t_{DP} is a device parameter (see AC Electrical Characteristics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 µF is recommended for most

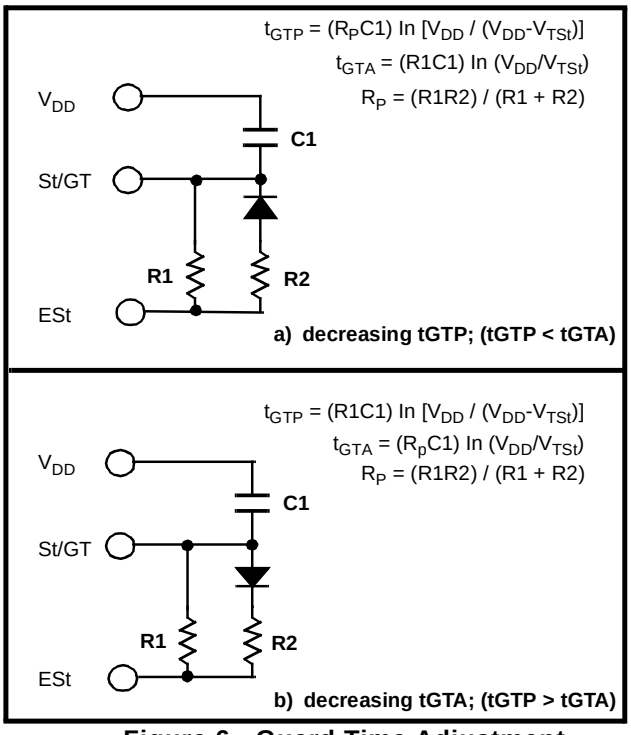


Figure 6 - Guard Time Adjustment

applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independent tone present (t_{GTP}) and tone absent (t_{GTA}) guard times. This may be necessary to meet system specifications which place both accept and reject limits on tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity.

Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain a valid signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 6. The receiver timing is shown in Figure 7 with a description of the events in Figure 9.

Call Progress Filter

A call progress mode, using the MT8888C/ MT8888C-1, can be selected allowing the detection of various tones, which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 7). Figure 8 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input, which are within the 'accept' bandwidth limits of the filter, are hard-limited by a high gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the $\overline{IRQ}$/CP pin will remain low.

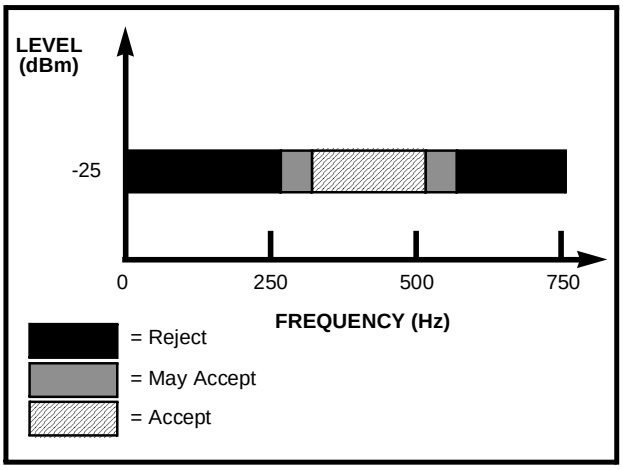


Figure 8 - Call Progress Response

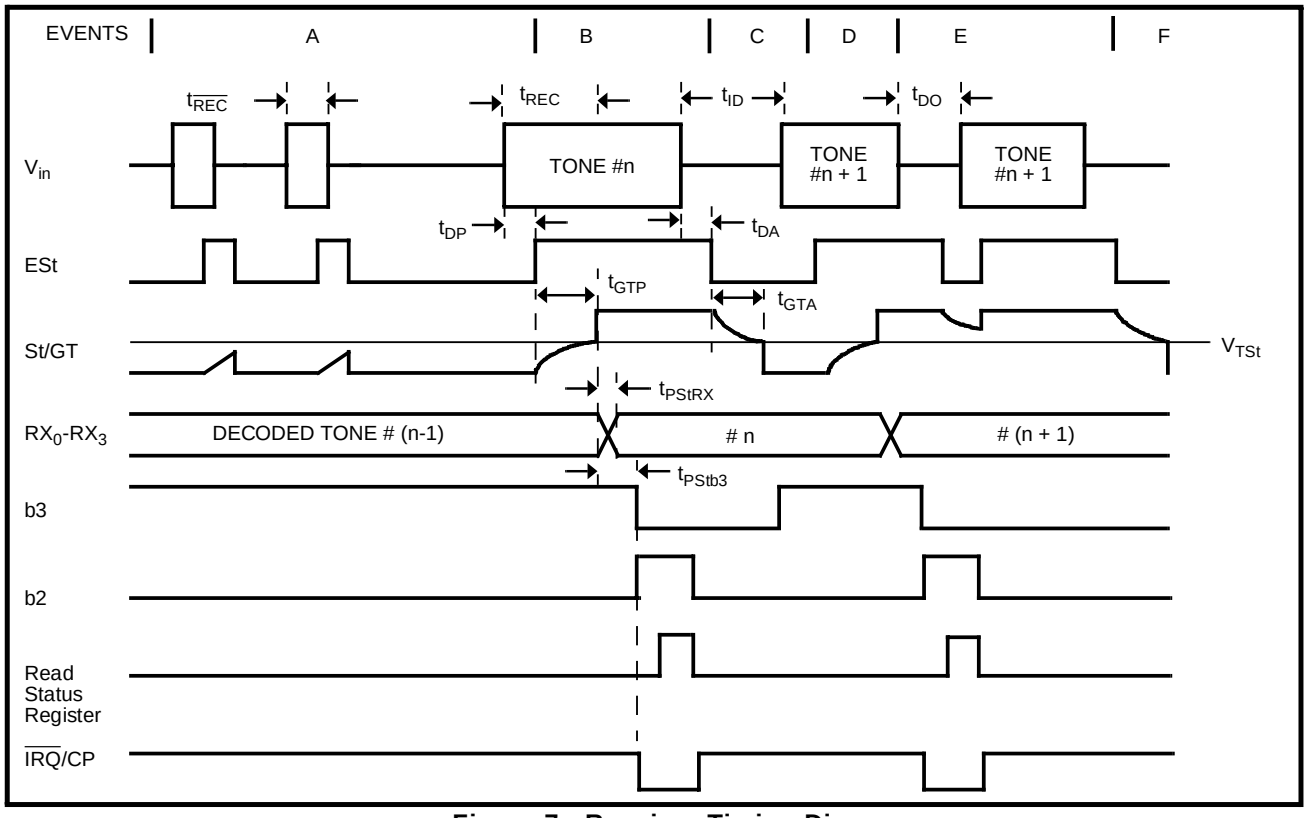


Figure 7 - Receiver Timing Diagram

EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

D) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.

E) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.

F) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$\overline{IRQ}$/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
$t_{\overline{REC}}$	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 9 - Description of Timing Events

DTMF Generator

The DTMF transmitter employed in the MT8888C/ MT8888C-1 is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 1 must be written to the transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically, the high group to low group amplitude ratio (twist) is 2 dB to compensate for high group attenuation on long loops.

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length, which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count, as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the frequency can also be varied. The divider output clocks another counter, which addresses the sinewave lookup ROM.

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones, which are then mixed using a low noise summing amplifier. The oscillator described needs no “start-up” time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 8 kHz. It can be seen from Figure 8 that the distortion products are very low in amplitude.

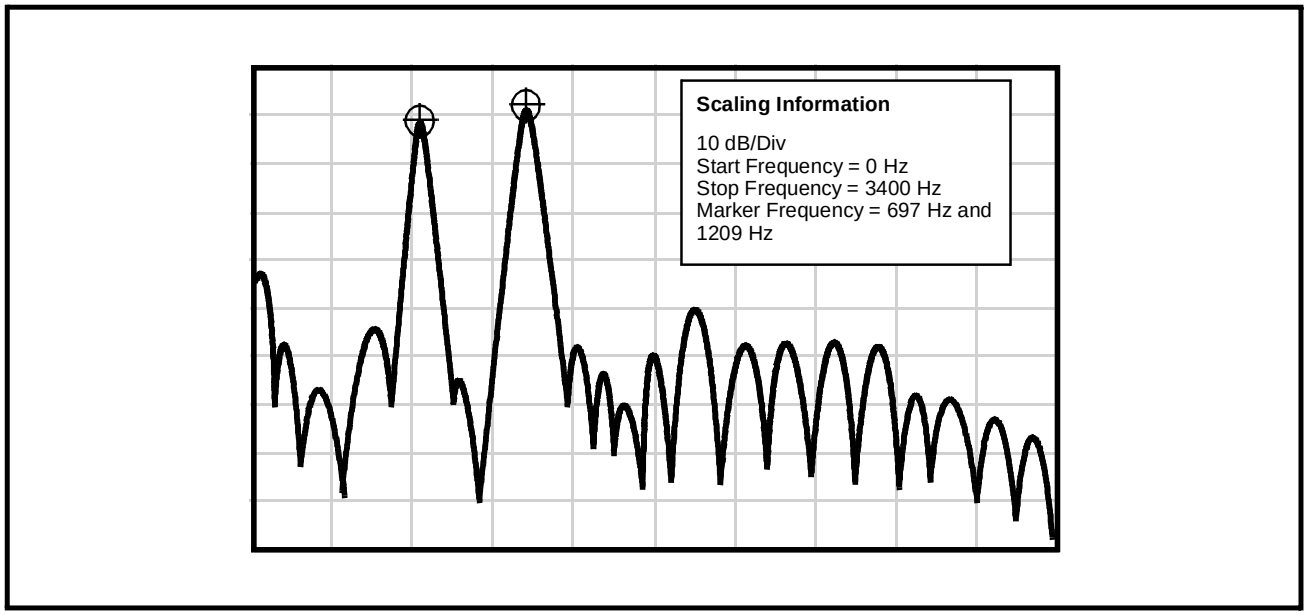


Figure 10 - Spectrum Plot

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms±1 ms, which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, the burst/pause duration is doubled to 102 ms ±2 ms. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation and distortion measurements. Refer to Control Register B description for details.

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 2. Actual Frequencies Versus Standard Requirements

Distortion Calculations

The MT8888C/MT8888C-1 is capable of producing precise tone bursts with minimal error in frequency (see Table 2). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage.

$$\text{THD (\%)} = 100 \frac{\left(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + ... V^2_{nf}}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

The Fourier components of the tone output correspond to V_{2f}.... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 10.

$$THD\ (\%) = 100 \frac{\sqrt{V^2_{2L} + V^2_{3L} + ... V^2_{nL} + V^2_{2H} + V^2_{3H} + .. V^2_{nH} + V^2_{IMD}}}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD (%) For a Dual Tone

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal. The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency Tolerance:	±0.1%
Resonance Mode:	Parallel
Load Capacitance:	18pF
Maximum Series Resistance:	150 ohms
Maximum Drive Level:	2mW

e.g. CTS Knights MP036S
Toyocom TQC-203-A-9S

A number of MT8888C/MT8888C-1 devices can be connected as shown in Figure 11 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer with the OSC2 outputs left unconnected.

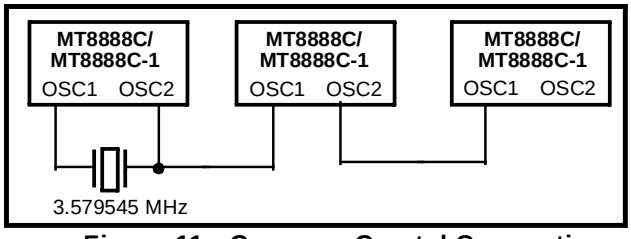


Figure 11 - Common Crystal Connection

Microprocessor Interface

The MT8888C/MT8888C-1 incorporates an Intel microprocessor interface which is compatible with fast versions (16 MHz) of the 80C51. No wait cycles need to be inserted.

Figures 17 and 18 are the timing diagrams for the Intel 8031, 8051 and 8085 (5 MHz) microcontrollers. By NANDing the address latch enable (ALE) output with the high-byte address (P2) decode output, $\overline{CS}$ is generated. Figure 12 summarizes the connection of these Intel processors to the MT8888C/MT8888C-1 transceiver.

The microprocessor interface provides access to five internal registers. The read-only Receive Data Register contains the decoded output of the last valid DTMF digit received. Data entered into the write-only Transmit Data Register will determine which tone pair is to be generated (see Table 1 for coding details). Transceiver control is accomplished with two control registers (see Tables 6 and 7), CRA and CRB, which have the same address. A write operation to CRB is executed by first setting the most significant bit (b3) in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will be directed back to CRA. The read-only status register indicates the current transceiver state (see Table 8).

A software reset must be included at the beginning of all programs to initialize the control registers upon power-up or power reset (see Figure 17). Refer to Tables 4-7 for bit descriptions of the two control registers.

The multiplexed $\overline{IRQ}$/CP pin can be programmed to generate an interrupt upon validation of DTMF signals or when the transmitter is ready for more data (burst mode only). Alternatively, this pin can be configured to provide a squarewave output of the call progress signal. The $\overline{IRQ}$/CP pin is an open drain output and requires an external pull-up resistor (see Figure 13).

RS0	$\overline{WR}$	$\overline{RD}$	FUNCTION
0	0	1	Write to Transmit Data Register
0	1	0	Read from Receive Data Register
1	0	1	Write to Control Register
1	1	0	Read from Status Register

Table 3. Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/DTMF	TOUT

Table 4. CRA Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	$\frac{BURST}{ENABLE}$

Table 5. CRB Bit Positions

BIT	NAME	DESCRIPTION
b0	TOUT	Tone Output Control. A logic high enables the tone output; a logic low turns the tone output off. This bit controls all transmit tone functions.
b1	CP/$\overline{\text{DTMF}}$	Call Progress or DTMF Mode Select. A logic high enables the receive call progress mode; a logic low enables DTMF mode. In DTMF mode the device is capable of receiving and transmitting DTMF signals. In CP mode a rectangular wave representation of the received tone signal will be present on the $\overline{\text{IRQ}}$/CP output pin if IRQ has been enabled (control register A, b2=1). In order to be detected, CP signals must be within the bandwidth specified in the AC Electrical Characteristics for Call Progress. Note: DTMF signals cannot be detected when CP mode is selected.
b2	IRQ	Interrupt Enable. A logic high enables the interrupt function; a logic low de-activates the interrupt function. When IRQ is enabled and DTMF mode is selected (control register A, b1=0), the $\overline{\text{IRQ}}$/CP output pin will go low when either 1) a valid DTMF signal has been received for a valid guard time duration, or 2) the transmitter is ready for more data (burst mode only).
b3	RSEL	Register Select. A logic high selects control register B for the next write cycle to the control register address. After writing to control register B, the following control register write cycle will be directed to control register A.

Table 6. Control Register A Description

BIT	NAME	DESCRIPTION
b0	$\overline{\text{BURST}}$	Burst Mode Select. A logic high de-activates burst mode; a logic low enables burst mode. When activated, the digital code representing a DTMF signal (see Table 1) can be written to the transmit register, which will result in a transmit DTMF tone burst and pause of equal durations (typically 51 msec.). Following the pause, the status register will be updated (b1 - Transmit Data Register Empty), and an interrupt will occur if the interrupt mode has been enabled. When CP mode (control register A, b1) is enabled the normal tone burst and pause durations are extended from a typical duration of 51 msec to 102 msec. When $\overline{\text{BURST}}$ is high (de-activated) the transmit tone burst duration is determined by the TOUT bit (control register A, b0).
b1	TEST	Test Mode Control. A logic high enables the test mode; a logic low de-activates the test mode. When TEST is enabled and DTMF mode is selected (control register A, b1=0), the signal present on the $\overline{\text{IRQ}}$/CP pin will be analogous to the state of the DELAYED STEERING bit of the status register (see Figure 7, signal b3).
b2	S/$\overline{\text{D}}$	Single or Dual Tone Generation. A logic high selects the single tone output; a logic low selects the dual tone (DTMF) output. The single tone generation function requires further selection of either the row or column tones (low or high group) through the C/$\overline{\text{R}}$ bit (control register B, b3).
b3	C/$\overline{\text{R}}$	Column or Row Tone Select. A logic high selects a column tone output; a logic low selects a row tone output. This function is used in conjunction with the S/$\overline{\text{D}}$ bit (control register B, b2).

Table 7. Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED}}$ $\overline{\text{STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 8. Status Register Description

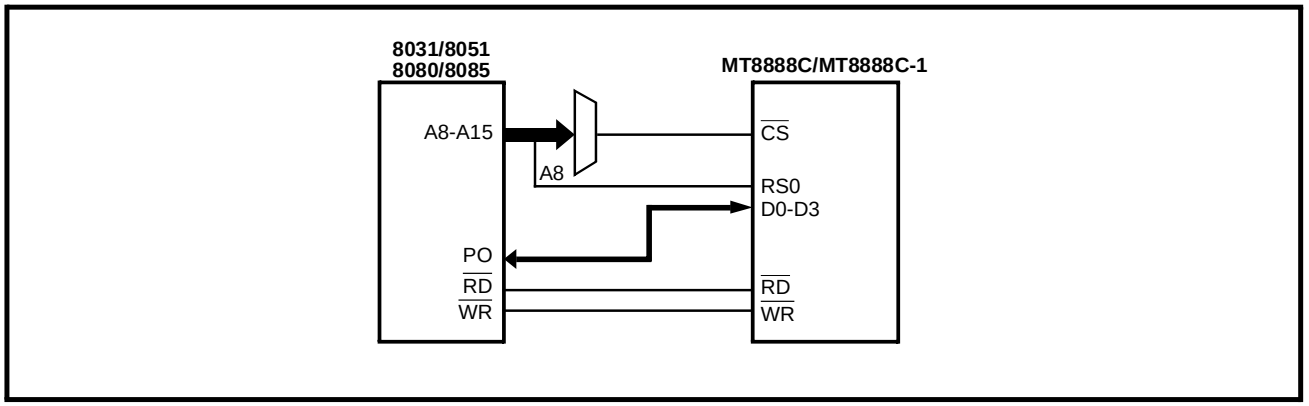


Figure 12 - MT8888C Interface Connections for Various Intel Micros

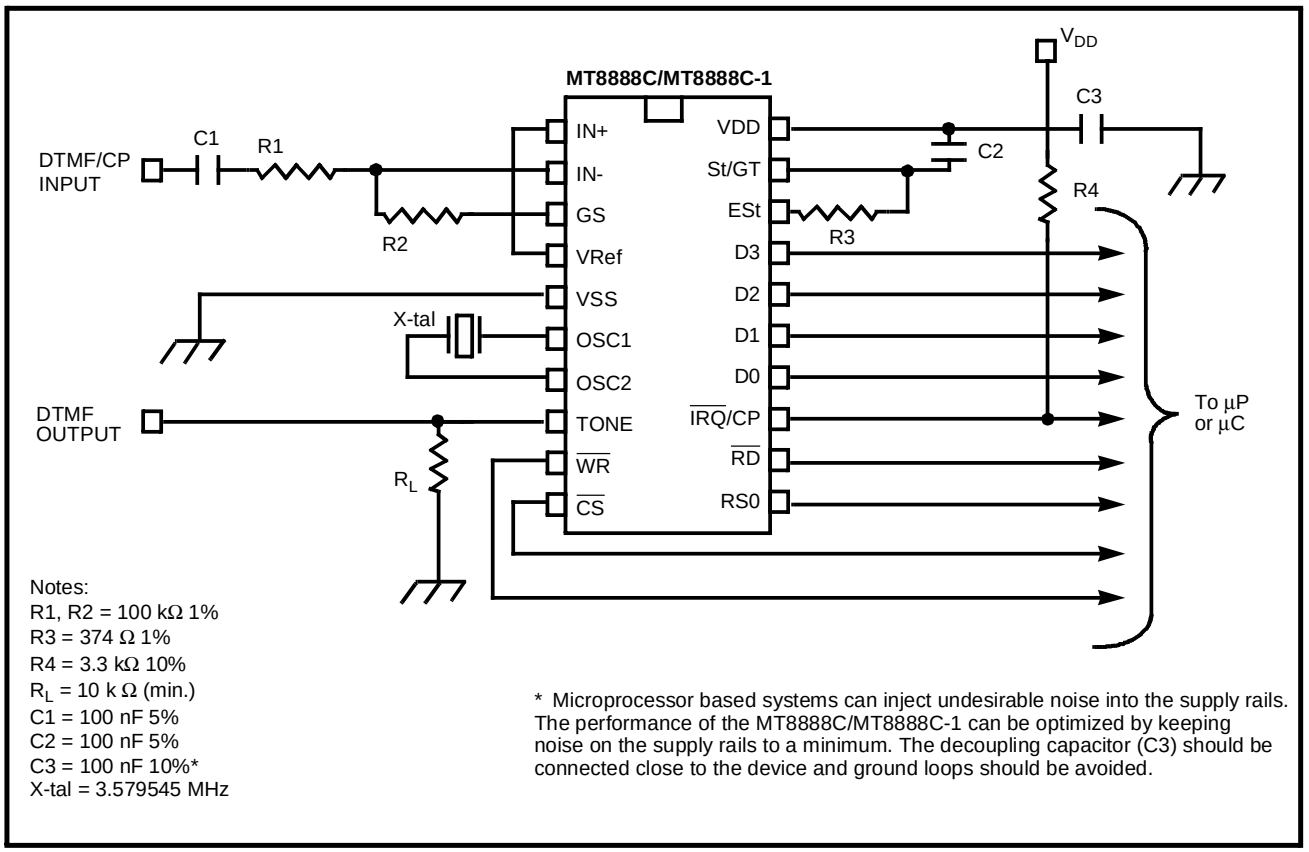


Figure 13 - Application Circuit (Single-Ended Input)

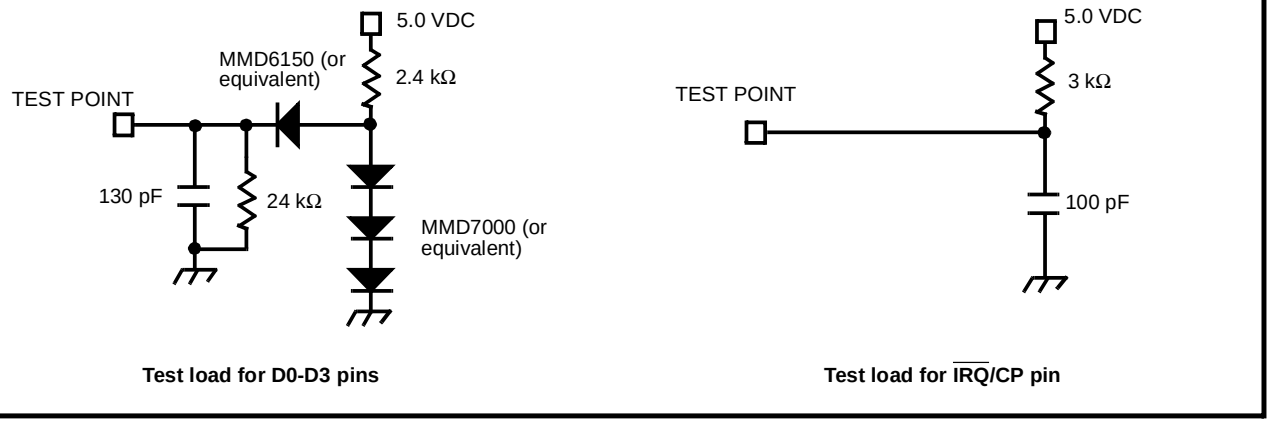


Figure 14 - Test Circuits

INITIALIZATION PROCEDURE

A software reset must be included at the beginning of all programs to initialize the control registers after power up.The initialization procedure should be implemented 100ms after power up.

Description:	**Control**			**Data**			
	RS0	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Read Status Register	1	1	0	X	X	X	X
2) Write to Control Register	1	0	1	0	0	0	0
3) Write to Control Register	1	0	1	0	0	0	0
4) Write to Control Register	1	0	1	1	0	0	0
5) Write to Control Register	1	0	1	0	0	0	0
6) Read Status Register	1	1	0	X	X	X	X

TYPICAL CONTROL SEQUENCE FOR BURST MODE APPLICATIONS

Transmit DTMF tones of 50 ms burst/50 ms pause and Receive DTMF Tones.

Sequence:

	RS0	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Write to Control Register A (tone out, DTMF, $\overline{IRQ}$, Select Control Register B)	1	0	1	1	1	0	1
2) Write to Control Register B (burst mode)	1	0	1	0	0	0	0
3) Write to Transmit Data Register (send a digit 7)	0	0	1	0	1	1	1
4) Wait for an interrupt or poll Status Register							
5) Read the Status Register	1	1	0	X	X	X	X
-if bit 1 is set, the Tx is ready for the next tone, in which case...							
Write to Transmit Register (send a digit 5)	0	0	1	0	1	0	1
-if bit 2 is set, a DTMF tone has been received, in which case....							
Read the Receive Data Register	0	1	0	X	X	X	X
-if both bits are set...							
Read the Receive Data Register	0	1	0	X	X	X	X
Write to Transmit Data Register	0	0	1	0	1	0	1

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (±2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 15 - Application Notes

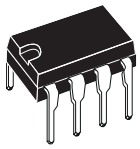
LAMPIRAN E

DATASHEET NE555

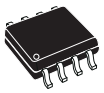
NE555
SA555 - SE555

GENERAL PURPOSE SINGLE BIPOLAR TIMERS

- LOW TURN OFF TIME
- MAXIMUM OPERATING FREQUENCY GREATER THAN 500kHz
- TIMING FROM MICROSECONDS TO HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- HIGH OUTPUT CURRENT CAN SOURCE OR SINK 200mA
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER^{o}C



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

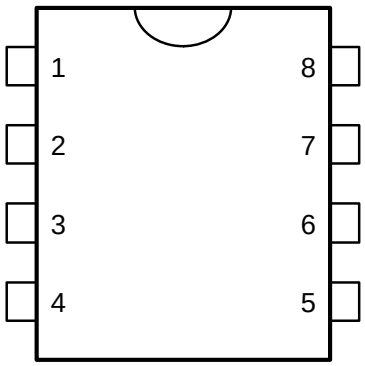
DESCRIPTION

The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.

ORDER CODES

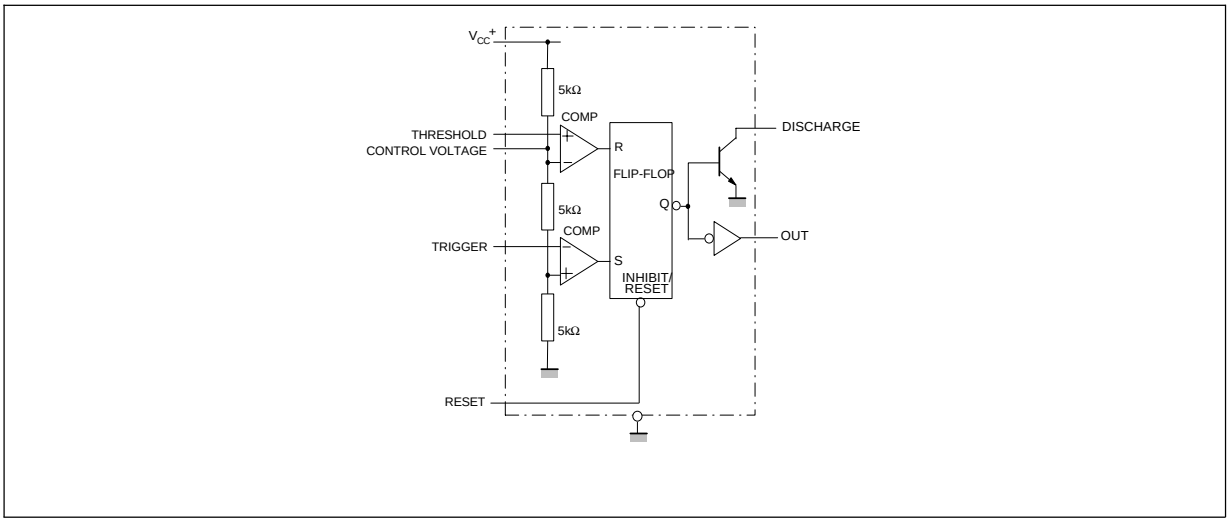
Part Number	Temperature Range	Package	
		N	D
NE555	0^{o}C, 70^{o}C	•	•
SA555	–40^{o}C, 105^{o}C	•	•
SE555	–55^{o}C, 125^{o}C	•	•

PIN CONNECTIONS (top view)

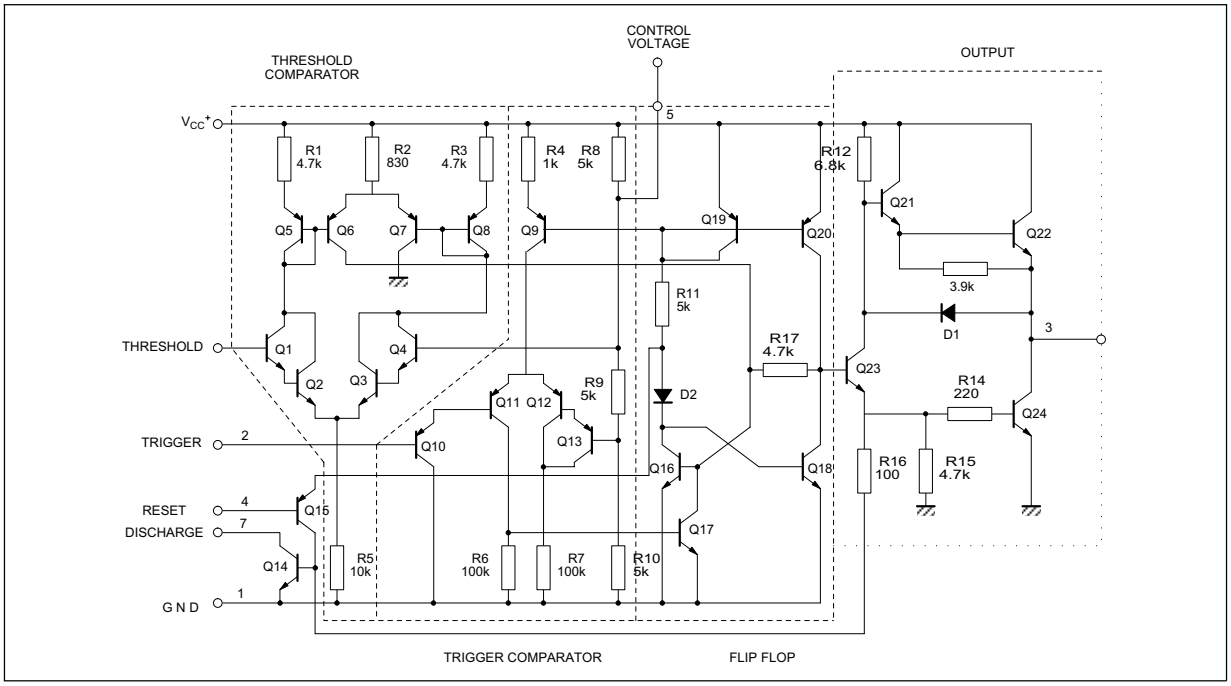


1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - V_{CC}

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{cc}	Supply Voltage		18	V
T_{oper}	Operating Free Air Temperature Range	for NE555 for SA555 for SE555	0 to 70 –40 to 105 –55 to 125	^oC
T_j	Junction Temperature		150	^oC
T_{stg}	Storage Temperature Range		–65 to 150	^oC

OPERATING CONDITIONS

Symbol	Parameter	SE555	NE555 - SA555	Unit
V_{CC}	Supply Voltage	4.5 to 18	4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V_{CC}	V

ELECTRICAL CHARACTERISTICS

T_{amb} = +25°C, V_{CC} = +5V to +15V (unless otherwise specified)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CC}	Supply Current (R_L ∞) (- note 1) Low State V_{CC} = +5V V_{CC} = +15V High State V_{CC} = 5V		 3 10 2	 5 12		 3 10 2	 6 15	mA
	Timing Error (monostable) (R_A = 2k to 100kΩ, C = 0.1µF) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 0.5 30 0.05	 2 100 0.2		 1 50 0.1	 3 0.5	 % ppm/°C %/V
	Timing Error (astable) (R_A, R_B = 1kΩ to 100kΩ, C = 0.1µF, V_{CC} = +15V) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 1.5 90 0.15			 2.25 150 0.3		 % ppm/°C %/V
V_{CL}	Control Voltage level V_{CC} = +15V V_{CC} = +5V	 9.6 2.9	 10 3.33	 10.4 3.8	 9 2.6	 10 3.33	 11 4	V
V_{th}	Threshold Voltage V_{CC} = +15V V_{CC} = +5V	 9.4 2.7	 10 3.33	 10.6 4	 8.8 2.4	 10 3.33	 11.2 4.2	V
I_{th}	Threshold Current - (note 3)		0.1	0.25		0.1	0.25	µA
V_{trig}	Trigger Voltage V_{CC} = +15V V_{CC} = +5V	 4.8 1.45	 5 1.67	 5.2 1.9	 4.5 1.1	 5 1.67	 5.6 2.2	V
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	0.9		0.5	2.0	µA
V_{reset}	Reset Voltage - (note 4)	0.4	0.7	1	0.4	0.7	1	V
I_{reset}	Reset Current V_{reset} = +0.4V V_{reset} = 0V		 0.1 0.4	 0.4 1		 0.1 0.4	 0.4 1.5	mA
V_{OL}	Low Level Output Voltage V_{CC} = +15V, $I_{O(sink)}$ = 10mA $I_{O(sink)}$ = 50mA $I_{O(sink)}$ = 100mA $I_{O(sink)}$ = 200mA V_{CC} = +5V, $I_{O(sink)}$ = 8mA $I_{O(sink)}$ = 5mA		 0.1 0.4 2 2.5 0.1 0.05	 0.15 0.5 2.2 0.25 0.2		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	V
V_{OH}	High Level Output Voltage V_{CC} = +15V, $I_{O(source)}$ = 200mA $I_{O(source)}$ = 100mA V_{CC} = +5V, $I_{O(source)}$ = 100mA	 13 3	 12.5 13.3 3.3		 12.75 2.75	 12.5 13.3 3.3		V

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at V_{CC} = +5V and V_{CC} = +15V.
3. This will determine the maximum value of R_A + R_B for +15V operation the max total is R = 20MΩ and for 5V operation the max total R = 3.5MΩ.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	SE555			NE555 - SA555			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{dis(off)}$	Discharge Pin Leakage Current (output high) (V_{dis} = 10V)		20	100		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 5) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		 180 80	 480 200		 180 80	 480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	200 200		100 100	300 300	ns
t_{off}	Turn off Time - (note 6) (V_{reset} = V_{CC})		0.5			0.5		µs

Notes : 5. No protection against excessive Pin 7 current is necessary, providing the package dissipation rating will not be exceeded.
6. Time mesaured from a positive going input pulse from 0 to 0.8x V_{CC} into the threshold to the drop from high to low of the output trigger is tied to treshold.

Figure 1 : Minimum Pulse Width Required for Trigering

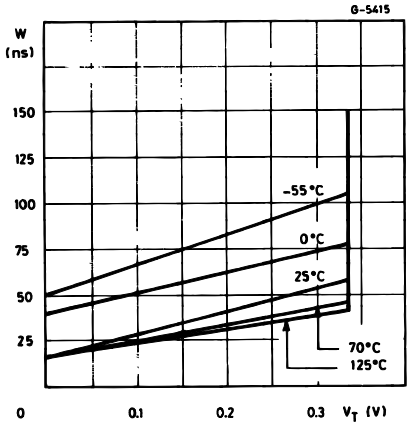


Figure 2 : Supply Current versus Supply Voltage

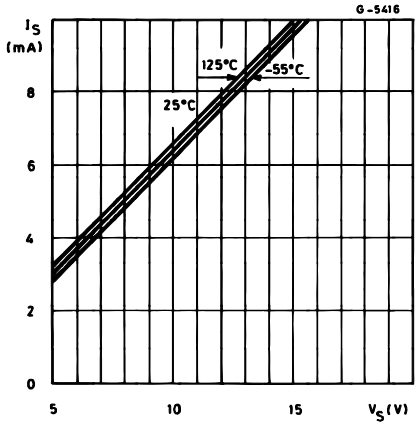


Figure 3 : Delay Time versus Temperature

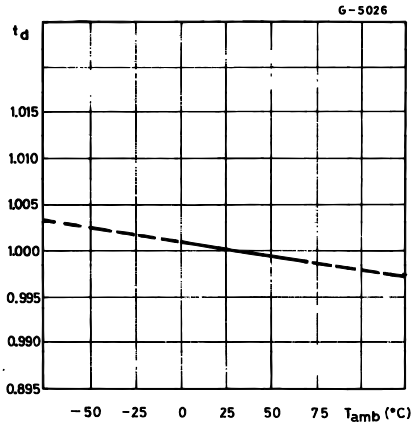


Figure 4 : Low Output Voltage versus Output Sink Current

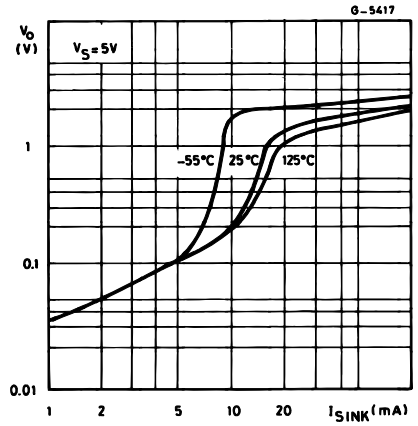


Figure 5 : Low Output Voltage versus Output Sink Current

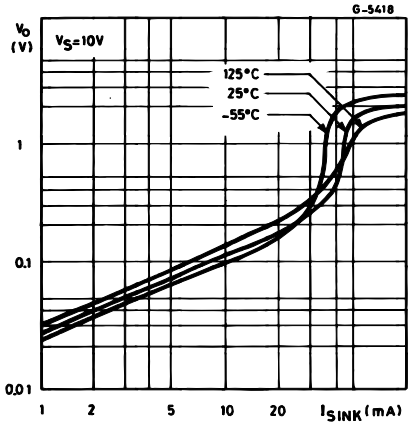


Figure 6 : Low Output Voltage versus Output Sink Current

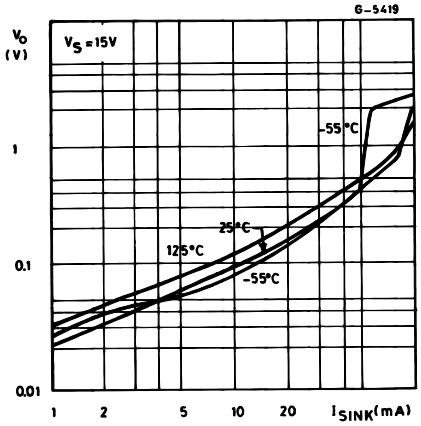


Figure 7 : High Output Voltage Drop versus Output

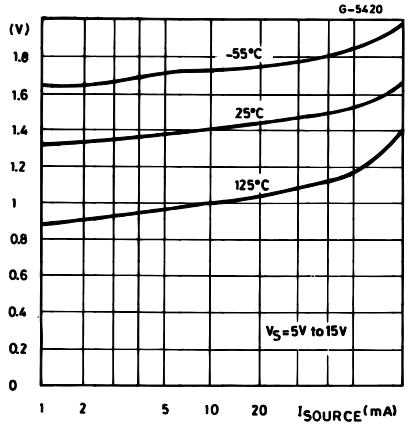


Figure 8 : Delay Time versus Supply Voltage

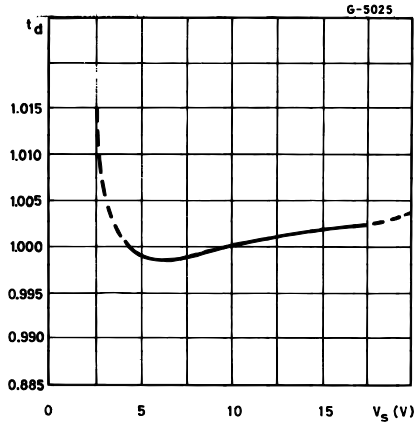
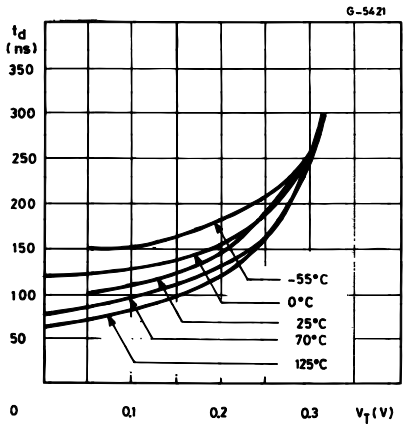


Figure 9 : Propagation Delay versus Voltage Level of Trigger Value

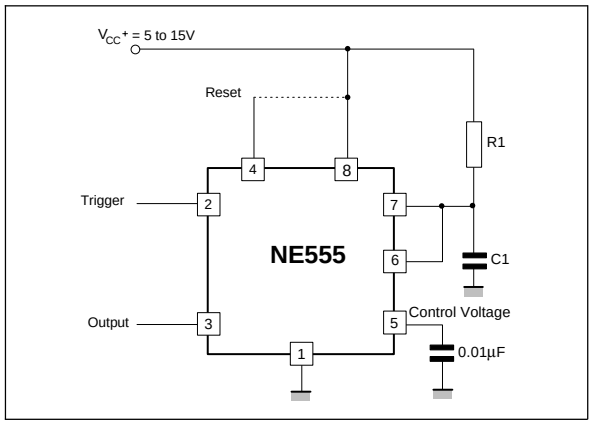


APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capacitor is initially held discharged by a transistor inside the timer.

Figure 10



The circuit triggers on a negative-going input signal when the level reaches 1/3 Vcc. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R_1C_1$ and is easily determined by figure 12.

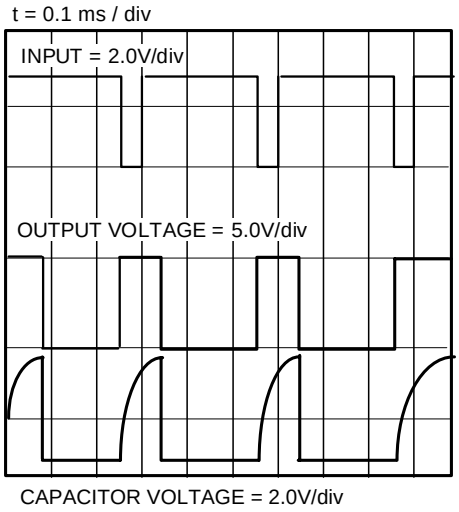
Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in applied, the output is driven to its LOW state.

When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R_1C_1$. When the voltage across the capacitor equals 2/3 V_{cc}, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state.

Figure 11 shows the actual waveforms generated in this mode of operation.

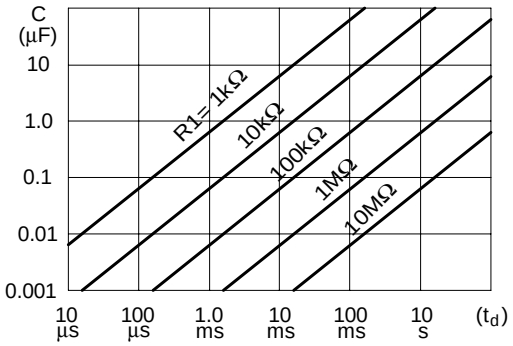
When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 11



R1 = 9.1kΩ, C1 = 0.01µF, R_L = 1kΩ

Figure 12



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R_1 and R_2 and discharges through R_2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C_1 charges and discharges between 1/3 V_{cc} and 2/3 Vcc. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 13

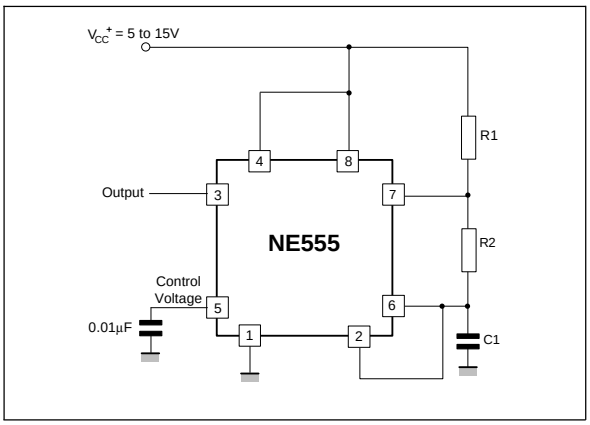


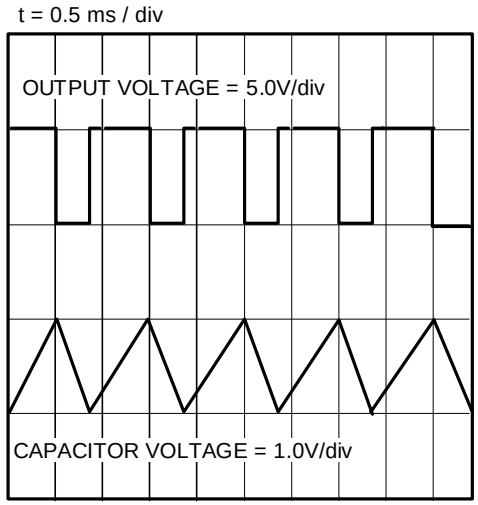
Figure 14 shows actual waveforms generated in this mode of operation.
The charge time (output HIGH) is given by :
$t_1 = 0.693 (R_1 + R_2) C_1$
and the discharge time (output LOW) by :
$t_2 = 0.693 (R_2) C_1$
Thus the total period T is given by :
$T = t_1 + t_2 = 0.693 (R_1 + 2R_2) C_1$
The frequency ofoscillation is them :

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) C_1}$$

and may be easily found by figure 15.
The duty cycle is given by :

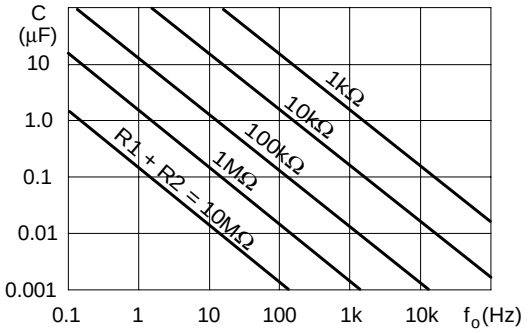
$$D = \frac{R_2}{R_1 + 2R_2}$$

Figure 14



R1 = R2 = 4.8kΩ, C1= 0.1µF, R_L = 1kΩ

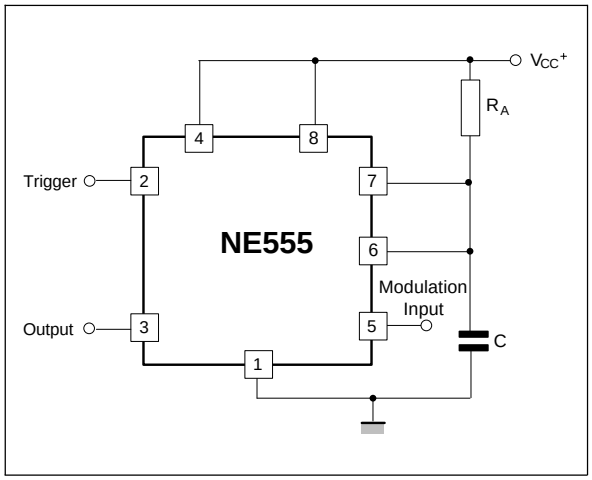
Figure 15 : Free Running Frequency versus R_1, R_2 and C_1



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width Modulator.



LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit configuration that will perform this function.

Figure 17.

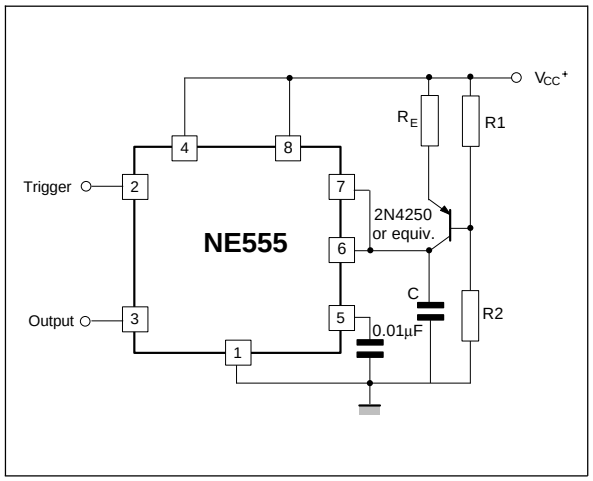
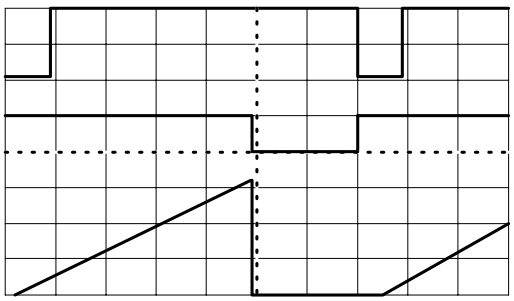


Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by :

$$T = \frac{(2/3\ V_{CC}\ R_E\ (R_{1+}\ R_{2)}\ C}{R_1\ V_{CC} - V_{BE}\ (R_{1+}\ R_{2)}} \quad V_{BE} = 0.6V$$

Figure 18 : Linear Ramp.



V_{CC} = 5V
Time = 20µs/DIV
R_1 = 47kΩ
R_2 = 100kΩ
R_E = 2.7kΩ
C = 0.01µF

Top trace : input 3V/DIV
Middle trace : output 5V/DIV
Bottom trace : output 5V/DIV
Bottom trace : capacitor voltage 1V/DIV

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle the resistors R_A and R_E may be connected as in figure 19. The time preriod for the output high is the same as previous,

$t_1 = 0.693\ R_A\ C.$

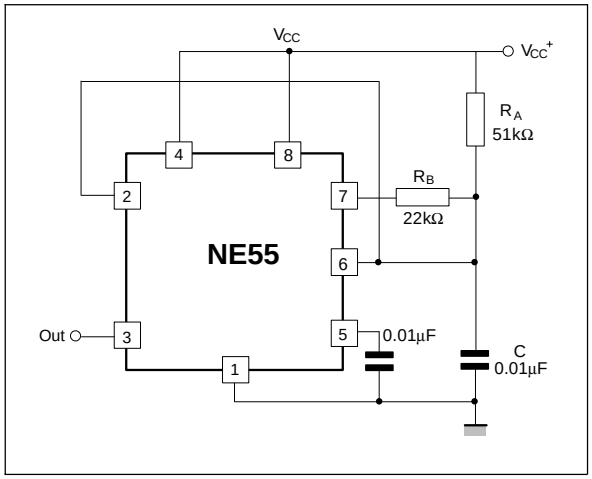
For the output low it is $t_2 =$

$$[(R_A R_B)/(R_A + R_B)]\ CLn\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

Note that this circuit will not oscillate if R_B is greater

Figure 19 : 50% Duty Cycle Oscillator.



than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

LAMPIRAN F

DATASHEET LM386

National Semiconductor

August 2000

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

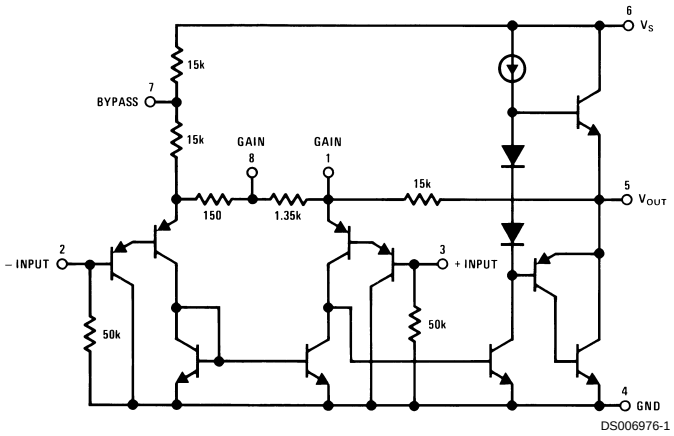
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

Applications

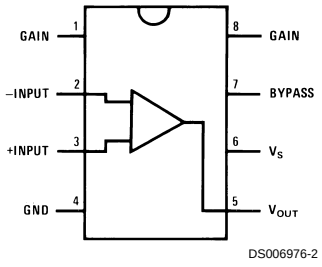
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



DS006976-1

Small Outline,
Molded Mini Small Outline,
and Dual-In-Line Packages



DS006976-2

Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	−65˚C to +150˚C
Operating Temperature	0˚C to +70˚C
Junction Temperature	+150˚C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260˚C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215˚C
Infrared (15 sec)	+220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37˚C/W
θ_{JA} (DIP)	107˚C/W
θ_{JC} (SO Package)	35˚C/W
θ_{JA} (SO Package)	172˚C/W
θ_{JA} (MSOP)	210˚C/W
θ_{JC} (MSOP)	56˚C/W

Electrical Characteristics (Notes 1, 2)

T_A = 25˚C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW		0.2		%
	f = 1 kHz, Pins 1 and 8 Open				
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF		50		dB
	Pins 1 and 8 Open, Referred to Output				
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25˚C, the device must be derated based on a 150˚C maximum junction temperature and 1) a thermal resistance of 107˚C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170˚C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≃ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

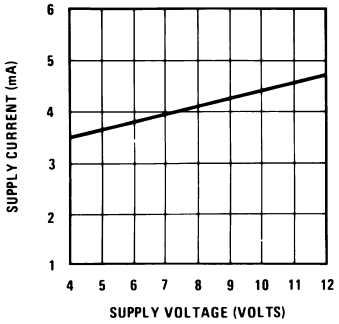
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 µF capacitor or a short to ground depending on the dc source resistance on the driven input.

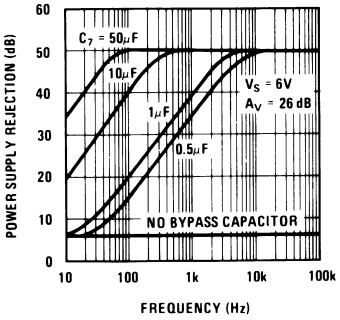
Typical Performance Characteristics

Quiescent Supply Current vs Supply Voltage



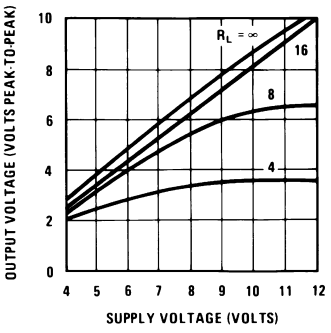
DS006976-5

Power Supply Rejection Ratio (Referred to the Output) vs Frequency



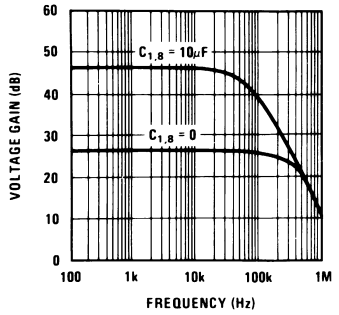
DS006976-12

Peak-to-Peak Output Voltage Swing vs Supply Voltage



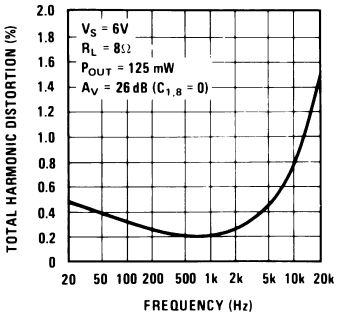
DS006976-13

Voltage Gain vs Frequency



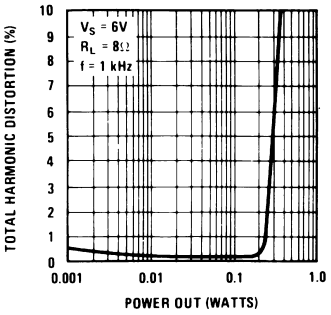
DS006976-14

Distortion vs Frequency



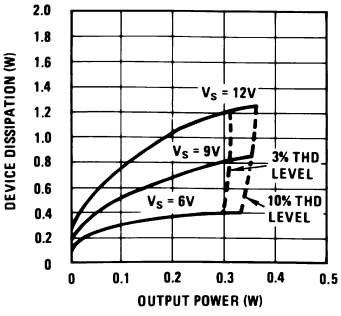
DS006976-15

Distortion vs Output Power



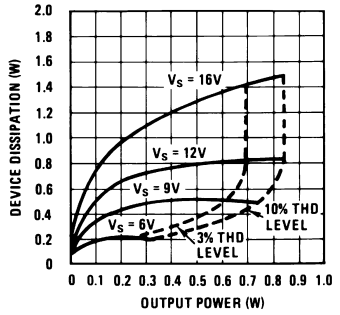
DS006976-16

Device Dissipation vs Output Power—4Ω Load



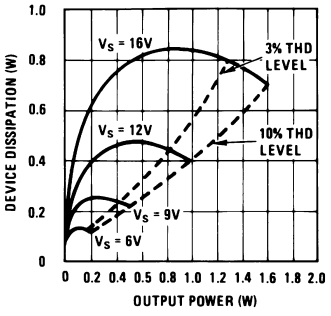
DS006976-17

Device Dissipation vs Output Power—8Ω Load



DS006976-18

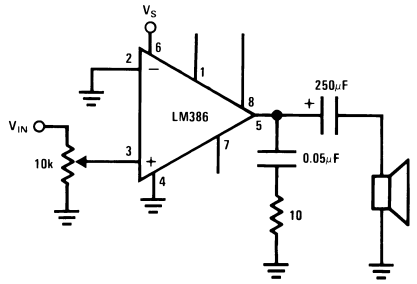
Device Dissipation vs Output Power—16Ω Load



DS006976-19

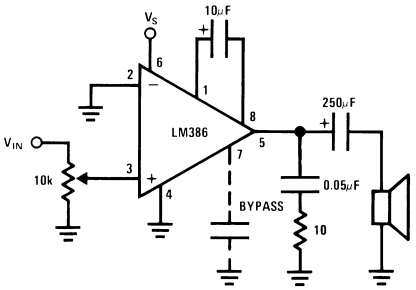
Typical Applications

Amplifier with Gain = 20
Minimum Parts



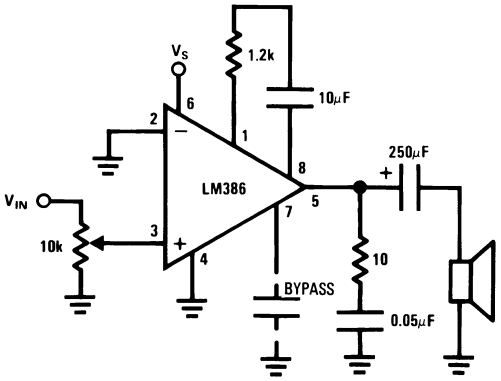
DS006976-3

Amplifier with Gain = 200



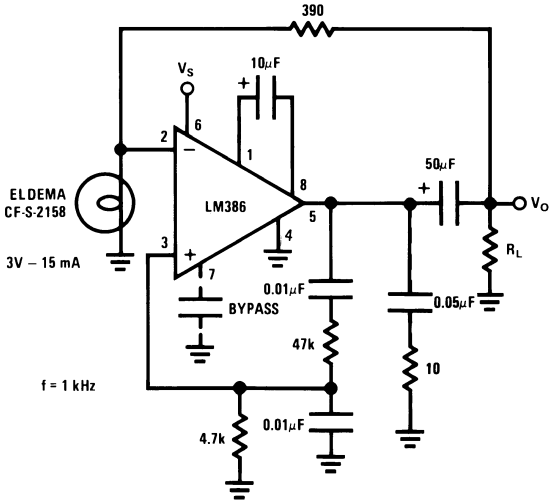
DS006976-4

Amplifier with Gain = 50



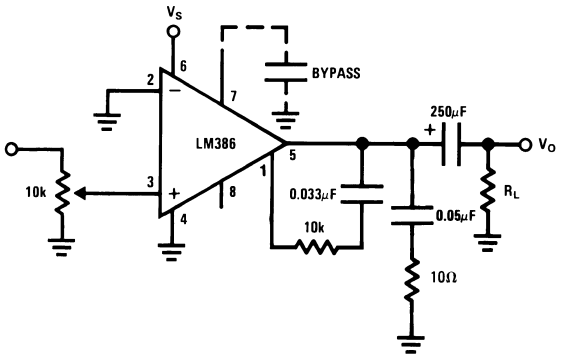
DS006976-6

Low Distortion Power Wienbridge Oscillator



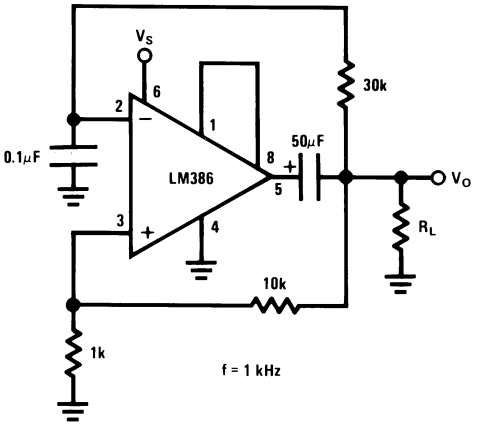
DS006976-7

Amplifier with Bass Boost



DS006976-8

Square Wave Oscillator



DS006976-9