LAMPIRAN A
PROGRAM PADA PENGONTROL MIKRO ATMEGA8535

PROGRAM UTAMA

```
//****************Program dengan metode space shift code******************
.include "c:\appnotes\m8535def.inc"
.org 0x0000
.def temp=r16
.def count=r17
.def data=r18
.def test1=r19
.def time=r20
.equ startcutoff=21 ;2,688 ms
.equ bit0cutoff=7 ;0,896 ms
.equ bit1cutoff=18 ;2,304 ms
.equ bit2cutoff=13 ;1,664 ms
.equ bit3cutoff=5 ;0,64 ms
.equ bit4cutoff=3 ;0,384 ms
.equ num1=0x80
.equ num2=0x81
.equ num3=0x82
.equ num4=0x83
.equ num5=0x84
.equ num6=0x85
.equ num7=0x86
.equ num8=0x87
.equ num9=0x88
.equ num0=0x89
.equ timer_value=0xf0fa
rjmp reset

reset:
ldi temp,low(ramend)
out spl,temp
ldi temp,high(ramend)
out sph,temp

// inisialisasi i/o dan timer
ldi temp,0xff
```

```
out ddrb,temp
out ddra,temp
ldi temp,0x00
out portb,temp
out porta,temp
out ddrc,temp
ldi temp,0x01
out portc,temp
ldi temp,0b00000101
out tccr0,temp;set prescaler 1024

// toggle switch
mainer:
ldi test1,0

main0:
sbrc test1,0
main1:
sbr test1,1

main2:
sbrc test1,1
main3:
sbr test1,2

main4:
sbrc test1,2
main5:
sbr test1,4

main6:
sbrc test1,3
main7:
sbr test1,8

// delay_132ms
ldi temp,0b00000100
out timsk,temp
```

```
ldi temp,high(timer_value)
out tcnt1h,temp
ldi temp,low(timer_value)
out tcnt1l,temp
ldi temp,0b00000101
out tccr1b,temp

looptimer:
in r20,tifr
sbrs r20,tov1
rjmp looptimer
ldi temp,0b00000100
out tifr,temp

//deteksi dan baca start bit
main:
sbic pinc,0;wait for start bit
rjmp main

ldi temp,0
out tcnt0,temp

parta:
sbis pinc,0
rjmp parta

in temp,tcnt0
cpi temp,startcutoff;test pulse size
brlo partb
rjmp main

partb:
cpi temp,bit1cutoff
breq main
brge partc
rjmp main
```

```
// deteksi dan baca data
partc: ;decoding subroutine
ldi count,8;counting
clr data

partd:
sbic pinc,0
rjmp partd

ldi temp,0
out tcnt0,temp

parte:
sbis pinc,0
rjmp parte

in temp,tcnt0
cpi temp,bit2cutoff
brlo partf
rjmp main

partf:
cpi temp,bit0cutoff
brlo partg
lsr data
sbr data,128
dec count
breq check_data ;all data received
rjmp partd ;or continue decoding

partg:
cpi temp,bit3cutoff
breq main
brge main
cpi temp,bit4cutoff
breq main
brge selang1
```

```
brlo main
selang1:
lsr data
cbr data,128
dec count
breq check_data ;all data received
rjmp partd ;or continue decoding

check_data:
cpi data,num1
breq onlight0
cpi data,num2
breq onlight1
cpi data,num3
breq onlight2
cpi data,num4
breq onlight3
cpi data,num9
breq onlight4
cpi data,num0
breq onlight5
rjmp main0

onlight0:
sbrc test1,0
rjmp lamp0_off
sbi portb,0          ;lamp1_on
rjmp main1
lamp0_off:
cbi portb,0          ;lamp1_off
cbr test1,1
rjmp main0

onlight1:
sbrc test1,1
rjmp lamp1_off
sbi portb,1          ;lamp2_on
rjmp main3
```

```
lamp1_off:
cbi portb,1         ;lamp2_off
cbr test1,2
rjmp main2

onlight2:
sbrc test1,2
rjmp lamp2_off
sbi portb,2         ;lamp3_on
rjmp main5
lamp2_off:
cbi portb,2         ;lamp3_off
cbr test1,4
rjmp main4

onlight3:
sbrc test1,3
rjmp lamp3_off
sbi portb,3         ;lamp4_on
rjmp main7
lamp3_off:
cbi portb,3         ;lamp4_off
cbr test1,8
rjmp main6

onlight4:
clr temp
out portb,temp    ;all_lamp_off
rjmp mainer

onlight5:
ser temp
out portb,temp     ;all_lamp_on
ldi test1,0xff
rjmp main0
```

```
//******************Program Metode Pulse Shift Code*********************
.include "c:\appnotes\m8535def.inc"
.org 0x0000
.def temp=r16
.def count=r17
.def count1=r24
.def data=r18
.def test1=r19
.def time=r20
.def data1=r21
.def data2=r22
.def data3=r23
.equ startcutoff=26 ;3,328 ms
.equ bit0cutoff=17 ;2,176 ms
.equ bit1cutoff=23 ;2,944 ms
.equ bit2cutoff=21 ;2,688 ms
.equ bit3cutoff=7 ;0,896 ms
.equ bit4cutoff=3 ;0,384 ms
.equ timer_value=0xf0fa
rjmp reset

reset:
ldi temp,low(ramend)
out spl,temp
ldi temp,high(ramend)
out sph,temp
start:
ldi temp,0xff
out ddrb,temp
out ddra,temp
ldi temp,0x00
out portb,temp
out porta,temp
out ddrc,temp
ldi temp,0xff
out portc,temp
ldi temp,0b00000101
out tccr0,temp
```

```
mainer:
ldi test1,0

//toggle switch
main0:
sbrc test1,0

main1:
sbr test1,1

main2:
sbrc test1,1
main3:
sbr test1,2

main4:
sbrc test1,2
main5:
sbr test1,4

main6:
sbrc test1,3
main7:
sbr test1,8



// delay 132_ms
ldi temp,0b00000100
out timsk,temp
ldi temp,high(timer_value)
out tcnt1h,temp
ldi temp,low(timer_value)
out tcnt1l,temp
ldi temp,0b00000101
out tccr1b,temp

looptimer:
```

```
in r20,tifr
sbrs r20,tov1
rjmp looptimer
ldi temp,0b00000100
out tifr,temp

//deteksi dan baca start bit
main:
sbic pinc,0;wait for start bit
rjmp main

parta:
sbis pinc,0
rjmp parta

ldi temp,0
out tcnt0,temp

clear:
sbic pinc,0
rjmp clear

in temp,tcnt0
cpi temp,startcutoff;test pulse size
brlo partb
rjmp main

partb:
cpi temp,bit1cutoff
breq main
brge partc
rjmp main

// deteksi dan baca 22 bit
partc:;decoding subroutine
ldi count1,0
repeat:
ldi count,8;counting
```

```
clr data

partd:
sbis pinc,0
rjmp partd

ldi temp,0
out tcnt0,temp

parte:
sbic pinc,0
rjmp parte

in temp,tcnt0
cpi temp,bit2cutoff
brlo partf
rjmp main

partf:
cpi temp,bit0cutoff
brlo partg
lsr data
sbr data,128
inc count1
cpi count1,22
breq partm
dec count
breq parth ;all data received
rjmp partd ;or continue decoding

partg:
cpi temp,bit3cutoff
brge main
cpi temp,bit4cutoff
brlo main
lsr data
cbr data,128
inc count1
```

```
cpi count1,22
breq partm
dec count
breq parth ;all data received
rjmp partd ;or continue decoding

parth:;decoding subroutine
cpi count1,8
breq finished_data1
cpi count1,16
breq finished_data2
rjmp main
finished_data1:
mov data1,data
rjmp repeat
finished_data2:
mov data2,data
rjmp repeat


partm:
mov data3,data

cpi data1,0x00
breq a
cpi data1,0x40
breq b
cpi data1,0x20
breq c
cpi data1,0x60
breq d
cpi data1,0x80
breq e
cpi data1,0xa0
breq f
rjmp main

a:
```

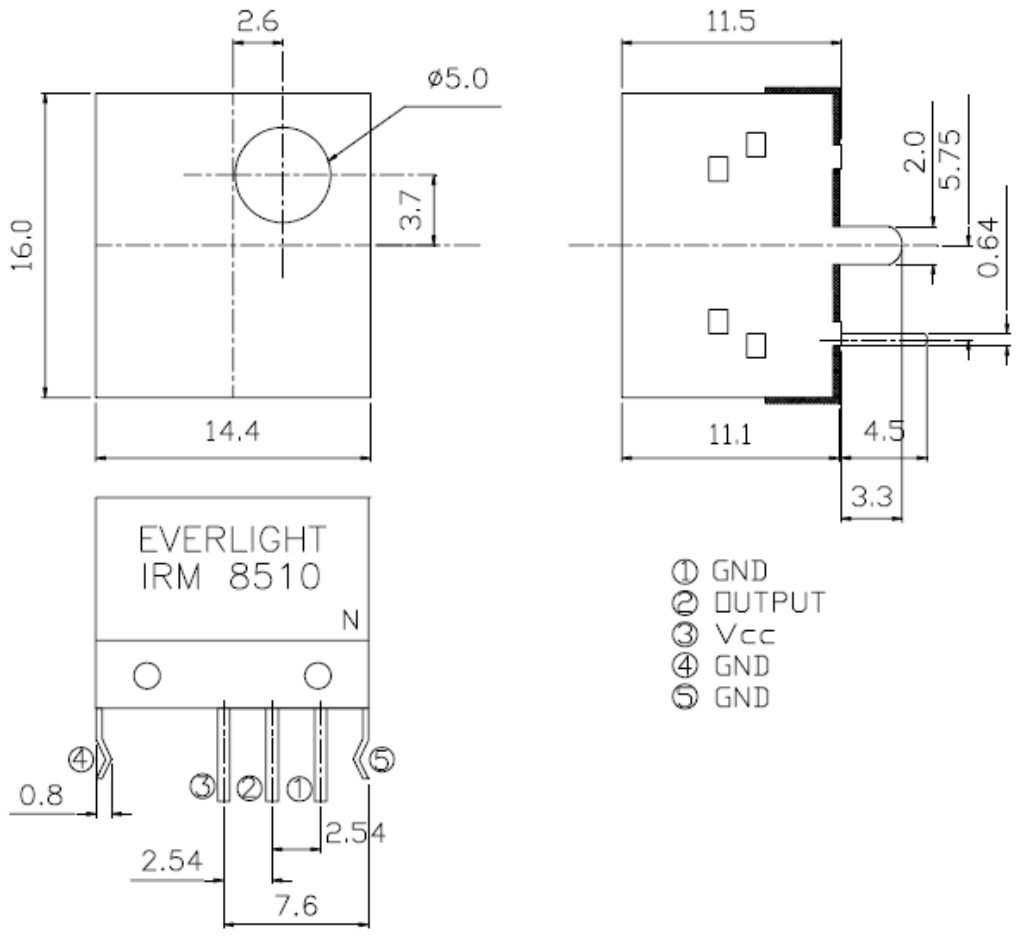
```
cpi data2,0xfa
breq p1
rjmp main

b:
cpi data2,0xfa
breq p2
rjmp main

c:
cpi data2,0xfa
breq p3
rjmp main

d:
cpi data2,0xfa
breq p4
rjmp main

e:
cpi data2,0xfa
breq p5
rjmp main

f:
cpi data2,0xfa
breq p6
rjmp main

p1:                  //tombol 1
cpi data3,0xbc
breq onlight0
rjmp main
p3:                 //tombol 3
cpi data3,0xb8
breq onlight1
rjmp main
p2:                 //tombol 2
```

```
cpi data3,0xb4
breq onlight2
rjmp main
p4:                 //tombol 4
cpi data3,0xb0
breq onlight3
rjmp main
p5:                 //tombol5
cpi data3,0xac
breq onlight4
rjmp main
p6:                  //tombol6
cpi data3,0xa8
breq onlight5
rjmp main

onlight0:
sbrc test1,0
rjmp lamp0_off
sbi portb,0      ;lamp1_on
rjmp main1
lamp0_off:
cbi portb,0      ;lamp1_off
cbr test1,1
rjmp main0

onlight1:
sbrc test1,1
rjmp lamp1_off
sbi portb,1      ;lamp2_on
rjmp main3
lamp1_off:
cbi portb,1      ;lamp2_off
cbr test1,2
rjmp main2

onlight2:
sbrc test1,2
```

```
rjmp lamp2_off
sbi portb,2       ;lamp3_on
rjmp main5
lamp2_off:
cbi portb,2       ;lamp3_off
cbr test1,4
rjmp main4

onlight3:
sbrc test1,3
rjmp lamp3_off
sbi portb,3       ;lamp4_on
rjmp main7
lamp3_off:
cbi portb,3       ;lamp4_off
cbr test1,8
rjmp main6

onlight4:
clr temp
out portb,temp          ;all_lamp_off
rjmp mainer

onlight5:
ser temp
out portb,temp          ;all_lamp_on
ldi test1,0xff
rjmp main0
```

LAMPIRAN B
DATA SHEET IR – 8510

PACKAGE DIMENSIONS :



OFFICE: NO 25,Lane 76,Chung Yang Rd, Sec.3 Tucheng, Taipei 236, Taiwan, R.O.C.
TEL : 886-2-2267-2000,2266-9936 (22 Lines)
FAX : 886-2-2267-6189
http://www.everlight.com

NOTES :

1. This drawing measure is a standard value. All dimensions are in millimeter.
2. In case of designation is tolerance ± 0.3mm.
3. Lead spacing is measured where the lead emerge from the package.
4. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
5. These specification sheets include materials protected under copyright of EVERLIGHT corporation. Please don't reproduce or cause anyone to reproduce them without EVERLIGHT consent.
6. When using this produce, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.

Description :

1. The module is a small type infrared remote control system receiver which has been developed and designed by utilizing the latest hybrid technology.
2. This single unit type module incorporates a photo diode and a receiving preamplifier IC.
3. The demodulated output signal can directly be decoded by a microprocessor.

Feature :

1. High protection ability to EMI and metal case can be customized.
2. Mold type and metal case type to meet the design of front panel.
3. Elliptic lens to improve the characteristic against
4. Line-up for various center carrier frequencies.
5. Low voltage and low power consumption.
6. High immunity against ambient light.
7. Photodiode with integrated circuit.
8. TTL and CMOS compatibility.
9. Long reception distance.
10. High sensitivity.

Application :

1. Optical switch
2. Light detecting portion of remote control
   - AV instruments such as Audio, TV, VCR, CD, MD, etc.
   - Home appliances such as Air-conditioner, Fan , etc.
   - The other equipments with wireless remote control.
   - CATV set top boxes
   - Multi-media Equipment

Absolute maximum ratings :

(Ta=25℃)

Parameter	Symbol	Ratings	Unit	Notice
Supply Voltage	Vcc	4.3~5.7	V	
Operating Temperature	Topr	-10～+60	℃	
Storage Temperature	Tstg	-20～+70	℃	
Soldering Temperature	Tsol	260	℃	4mm from mold body less than 5 seconds

Electro Optical Characteristics :

(Ta=25℃)

Parameter	Symbol	MIN	TYP	MAX	Unit	Condition
Supply Voltage	Vcc	4.7	5	5.3	V	DC voltage
Supply Current	Icc	-	-	3	mA	No signal input
B.P.F Center Frequency	fo	-	37.9	-	KHz	
Peak Wavelength	λ p	-	940	-	nm	
Transmission Distance	L_0	5	-	-	m	At the ray axis *1
	L_{45}	2.5	-			
Half Angle	θ	-	45	-	deg	
High Level Pulse Width	T_H	400	-	800	μs	At the ray axis *2
Low Level Pulse Width	T_L	400	-	800	μs	
High Level Output Voltage	V_H	4.5	-	-	V	
Low Level Output Voltage	V_L			0.5	V	

*1:The ray receiving surface at a vertex and relation to the ray axis in the range of ϕ= 0° and ϕ=45°.

*2:A range from 30cm to the arrival distance. Average value of 50 pulses.

■ TEST METHOD：

The specified electro-optical characteristics is satisfied under the following Conditions at the controllable distance.

①Measurement place

A place that is nothing of extreme light reflected in the room.

②External light

Project the light of ordinary white fluorescent lamps which are not high Frequency lamps and must be less then 10 Lux at the module surface. (Ee≦10Lux)

③Standard transmitter

A transmitter whose output is so adjusted as to Vo=400mVp-p and the output Wave form shown in Fig.-1.According to the measurement method shown in Fig.-2 the standard transmitter is specified. However, the infrared photodiode to be used for the transmitter should be λp=940nm, $\Delta\lambda$=50nm. Also, photo diode is used of PD438B (V_R=5V).
(Standard light / Light source temperature 2856°K).

④Measuring system

According to the measuring system shown in Fig.-3

■ Module schematic & circuit：

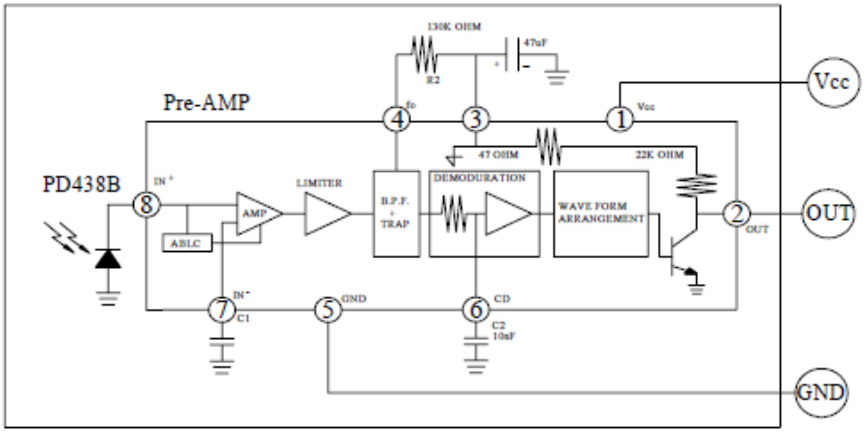
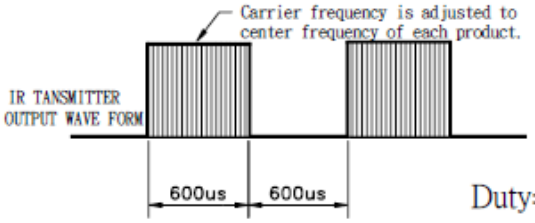
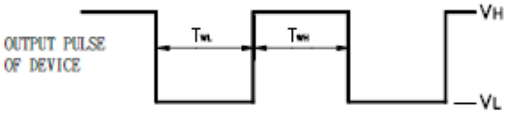


Fig.-1 Transmitter Wave Form



D.U.T Output Pulse



Duty=0.5

Fig.-2 Measuring Method

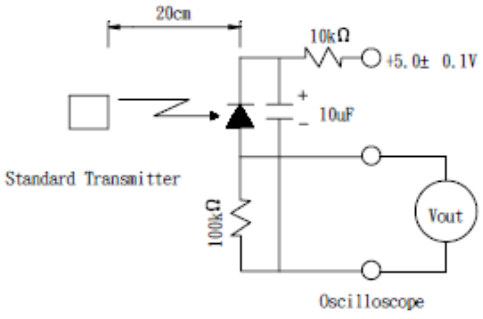
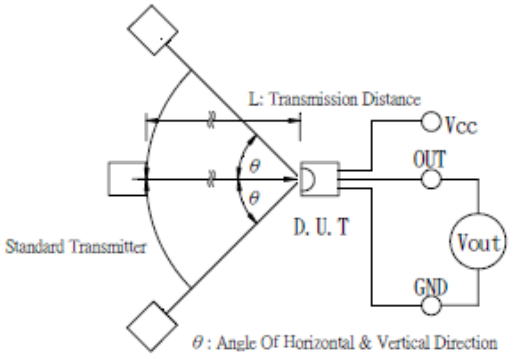


Fig.-3 Measuring System



TYPICAL ELECTRICAL/OPTICAL/CHARACTERISTICS CURVES

Fig.-4 Relative Spectral Sensitivity vs. Wavelength

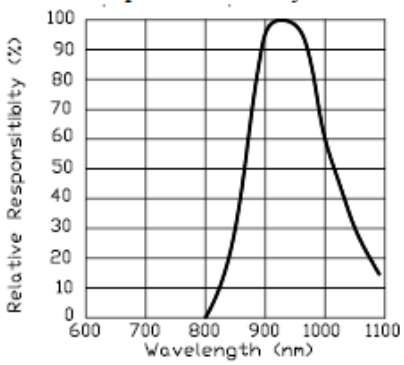


Fig.-5 Relative Transmission Distance vs. Direction

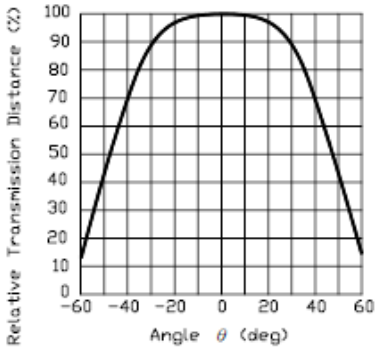


Fig.-6 Output Pulse Length vs. Arrival Distance

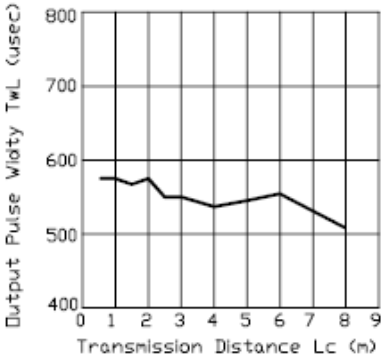


Fig.-7 Arrival Distance vs. Supply Voltage

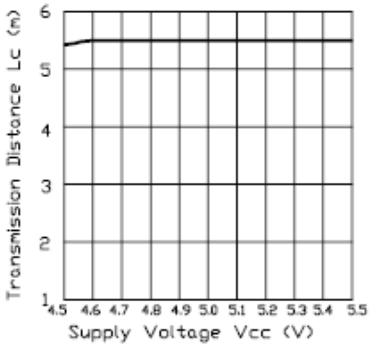


Fig.-8 Relative Transmission Distance vs. Center Carrier Frequency

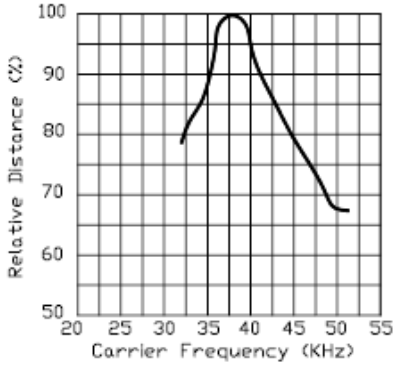
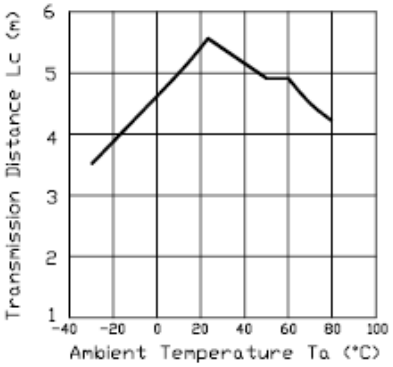


Fig.-9 Arrival Distance vs. Ambient Temperature



Reliability test item and condition :

The reliability of products shall be satisfied with items listed below.
Confidence level: 90%
LTPD: 10%

Test Items	Test Conditions	Failure Judgement Criteria	Samples(n) Defective(c)
Operation life	Vcc=5V,Ta:25℃ 1000hrs	$L_0 \leqq L \times 0.8$ $L_{45} \leqq L \times 0.8$ L: Lower specification limit	n=22,c=0
Temperature cycle	1 cycle -20℃ +25℃ +70℃ (30min) 5min (30min) 50 cycle test		n=22,c=0
Thermal shock	-10℃ to +70℃ (5min) (10sec) (5min) 50 cycle test		n=22,c=0
High temperature storage	Temp: +70℃ 1000hrs		n=22,c=0
Low temperature storage	Temp: -20℃ 1000hrs		n=22,c=0
High temperature High humidity	Ta: 85℃ RH:85% 1000hrs		n=22,c=0
Solder heat	Temp: 260± 5℃ 5sec 4mm Form the bottom of the package.		n=22,c=0
Solderability	Temp: 230± 5℃ 5sec 4mm Form the bottom of the package.	More than 90% of Lead to be covered by soldering	n=22,c=0

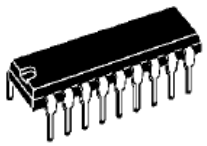
LAMPIRAN C
DATA SHEET ULN – 2803

SGS-THOMSON MICROELECTRONICS

ULN2801A
ULN2802A - ULN2803A
ULN2804A - ULN2805A

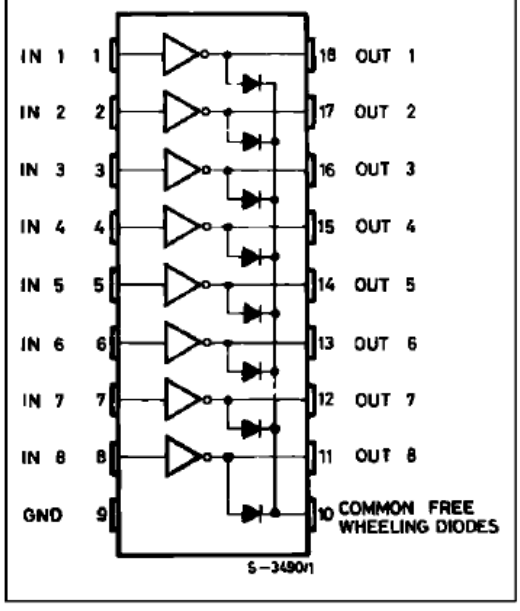
EIGHT DARLINGTON ARRAYS

- EIGHT DARLINGTONS WITH COMMON EMITTERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMILIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT



DIP18

PIN CONNECTION (top view)



DESCRIPTION

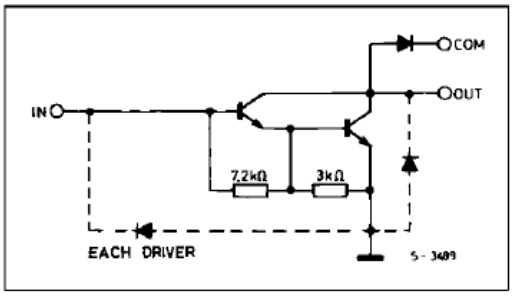
The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600mA (500mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor ; the ULN2802A has a 10.5kΩ input resistor and zener for 14-25V PMOS ; the ULN2803A has a 2.7kΩ input resistor for 5V TTL and CMOS ; the ULN2804A has a 10.5kΩ input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

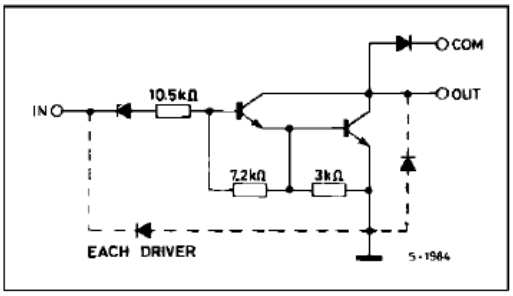
All types are supplied in a 18-lead plastic DIP with a copper lead frame and feature the convenient input-opposite-output pinout to simplify board layout.

SCHEMATIC DIAGRAM AND ORDER CODES

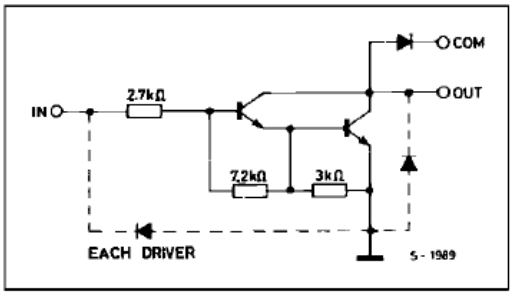
For ULN2801A (each driver for PMOS-CMOS)



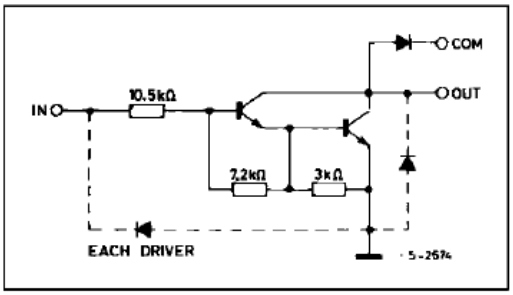
For ULN2802A (each driver for 14-15 V PMOS)



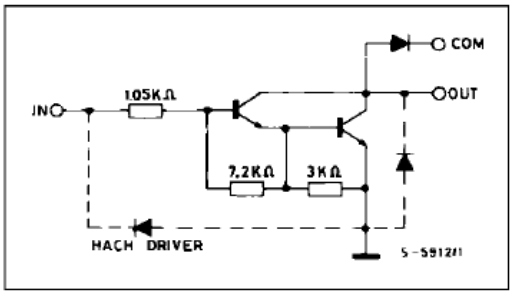
For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS



For ULN2805A (each driver for high out TTL)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_i	Input Voltage for ULN2802A, UL2803A, ULN2804A for ULN2805A	 30 15	V
I_C	Continuous Collector Current	500	mA
I_B	Continuous Base Current	25	mA
P_{tot}	Power Dissipation (one Darlington pair) (total package)	 1.0 2.25	W
T_{amb}	Operating Ambient Temperature Range	– 20 to 85	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
Tj	Junction Temperature Range	– 20 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	55	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CEX}	Output Leakage Current	V_{CE} = 50V T_{amb} = 70°C, V_{CE} = 50V T_{amb} = 70°C for ULN2802A V_{CE} = 50V, V_i = 6V for ULN2804A V_{CE} = 50V, V_i = 1V			50 100 500 500	µA µA µA µA	1a 1a 1b 1b
$V_{CE(sat)}$	Collector-emitter Saturation Voltage	I_C = 100mA, I_B = 250µA I_C = 200mA, I_B = 350µA I_C = 350mA, I_B = 500µA		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
$I_{i(on)}$	Input Current	for ULN2802A V_i = 17V for ULN2803A V_i = 3.85V for ULN2804A V_i = 5V V_i = 12V for ULN2805A V_i = 3V		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA mA	3
$I_{i(off)}$	Input Current	T_{amb} = 70°C, I_C = 500µA	50	65		µA	4
$V_{i(on)}$	Input Voltage	V_{CE} = 2 V for ULN2802A I_C = 300mA for ULN2803A I_C = 200mA I_C = 250mA I_C = 300mA for ULN2804A I_C = 125mA I_C = 200mA I_C = 275mA I_C = 350mA for ULN2805A I_C = 350mA			 13 2.4 2.7 3 5 6 7 8 2.4	 V V V V V V V V V	5
h_{FE}	DC Forward Current Gain	for ULN2801A V_{CE} = 2V, I_C = 350mA	1000			–	2
C_i	Input Capacitance			15	25	pF	–
t_{PLH}	Turn-on Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
t_{PHL}	Turn-off Delay Time	0.5 V_i to 0.5 V_o		0.25	1	µs	–
I_R	Clamp Diode Leakage Current	V_R = 50V T_{amb} = 70°C, V_R = 50V			50 100	µA µA	6 6
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2	V	7

LAMPIRAN D
DATA SHEET ATMEGA8535

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 512 Bytes Internal SRAM
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    8 Single-ended Channels
    7 Differential Channels for TQFP Package Only
    2 Differential Channels with Programmable Gain at 1x, 10x, or 200x for TQFP Package Only
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-lead PLCC, and 44-pad MLF
- Operating Voltages
  - 2.7 - 5.5V for ATmega8535L
  - 4.5 - 5.5V for ATmega8535
- Speed Grades
  - 0 - 8 MHz for ATmega8535L
  - 0 - 16 MHz for ATmega8535

8-bit AVR® Microcontroller with 8K Bytes In-System Programmable Flash

ATmega8535
ATmega8535L

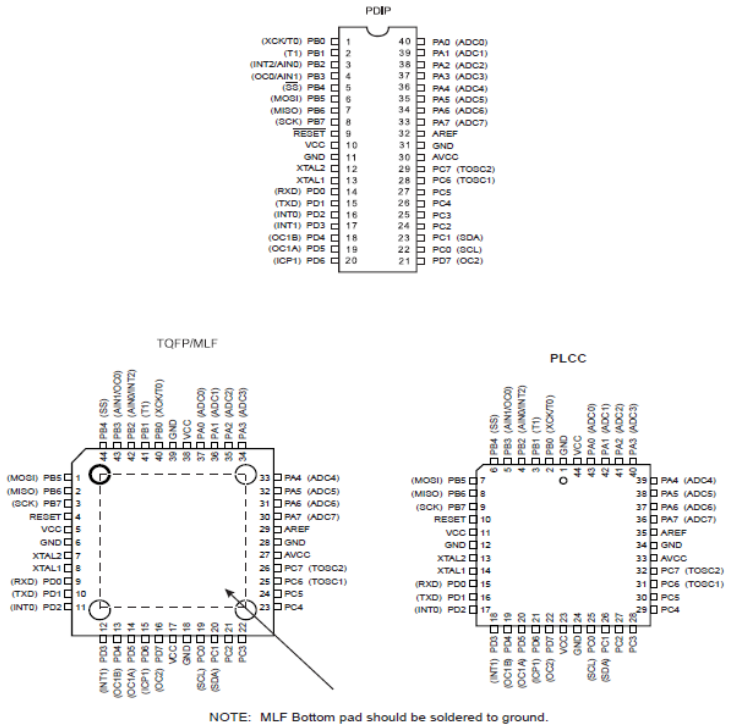
Preliminary Summary

Rev. 2502ES–AVR–12/03

Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.

Pin Configurations

Figure 1. Pinout ATmega8535



NOTE: MLF Bottom pad should be soldered to ground.

Disclaimer

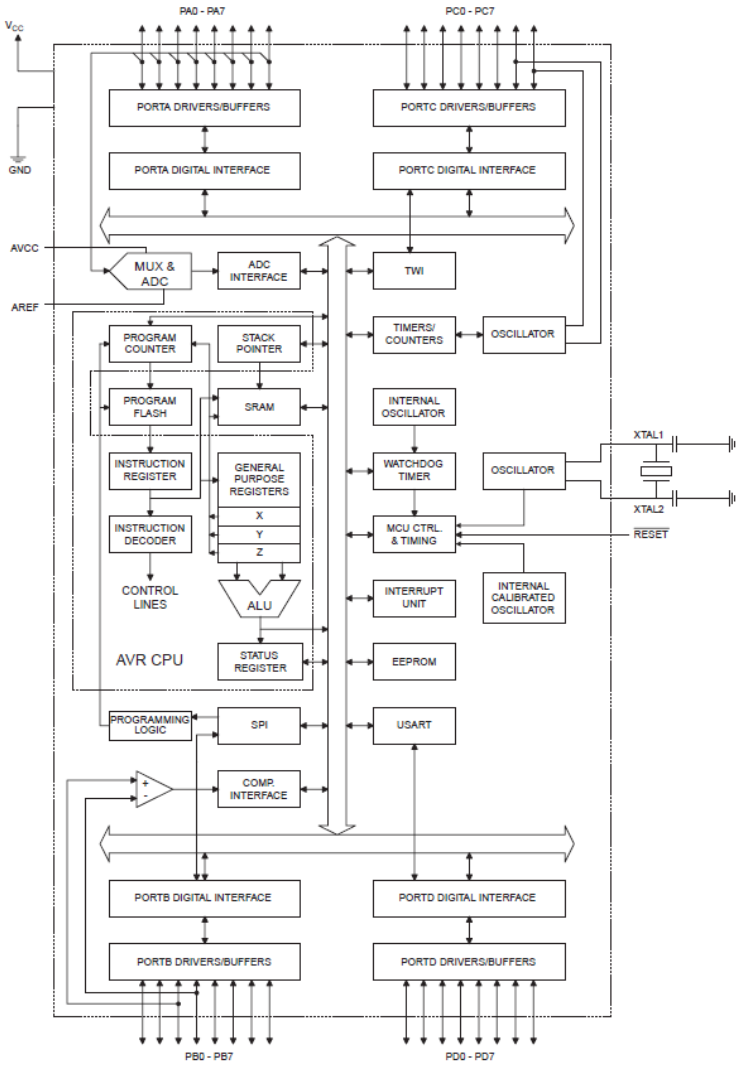
Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Overview

The ATmega8535 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the ATmega8535 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 2. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8535 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 512 bytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, an 8-channel, 10-bit ADC with optional differential input stage with programmable gain in TQFP package, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption. In Extended Standby mode, both the main Oscillator and the asynchronous timer continue to run.

The device is manufactured using Atmel's high density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8535 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega8535 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

AT90S8535 Compatibility

The ATmega8535 provides all the features of the AT90S8535. In addition, several new features are added. The ATmega8535 is backward compatible with AT90S8535 in most cases. However, some incompatibilities between the two microcontrollers exist. To solve this problem, an AT90S8535 compatibility mode can be selected by programming the S8535C fuse. ATmega8535 is pin compatible with AT90S8535, and can replace the AT90S8535 on current Printed Circuit Boards. However, the location of fuse bits and the electrical characteristics differs between the two devices.

AT90S8535 Compatibility Mode

Programming the S8535C fuse will change the following functionality:

- The timed sequence for changing the Watchdog Time-out period is disabled. See "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 43 for details.
- The double buffering of the USART Receive Register is disabled. See "AVR USART vs. AVR UART – Compatibility" on page 143 for details.

Pin Descriptions

V_{CC}	Digital supply voltage.
GND	Ground.
Port A (PA7..PA0)	Port A serves as the analog inputs to the A/D Converter. Port A also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port B (PB7..PB0)	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port B also serves the functions of various special features of the ATmega8535 as listed on page 58.
Port C (PC7..PC0)	Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port D (PD7..PD0)	Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port D also serves the functions of various special features of the ATmega8535 as listed on page 62.
$\overline{\text{RESET}}$	Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 35. Shorter pulses are not guaranteed to generate a reset.
XTAL1	Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.
XTAL2	Output from the inverting Oscillator amplifier.
AVCC	AVCC is the supply voltage pin for Port A and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.
AREF	AREF is the analog reference pin for the A/D Converter.

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	8
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	10
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	10
0x3C (0x5C)	OCR0	Timer/Counter0 Output Compare Register								83
0x3B (0x5B)	GICR	INT1	INT0	INT2	–	–	–	IVSEL	IVCE	47, 67
0x3A (0x5A)	GIFR	INTF1	INTF0	INTF2	–	–	–	–	–	68
0x39 (0x59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	83, 113, 131
0x38 (0x58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	84, 114, 132
0x37 (0x57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	225
0x36 (0x56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	178
0x35 (0x55)	MCUCR	SM2	SE	SM1	SM0	ISC11	ISC10	ISC01	ISC00	30, 66
0x34 (0x54)	MCUCSR	–	ISC2	–	–	WDRF	BORF	EXTRF	PORF	38, 67
0x33 (0x53)	TCCR0	FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	81
0x32 (0x52)	TCNT0	Timer/Counter0 (8 Bits)								83
0x31 (0x51)	OSCCAL	Oscillator Calibration Register								28
0x30 (0x50)	SFIOR	ADTS2	ADTS1	ADTS0	–	ACME	PUD	PSR2	PSR10	57,86,133,200,220
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	108
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	111
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								112
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								112
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High Byte								112
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low Byte								112
0x29 (0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High Byte								112
0x28 (0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low Byte								112
0x27 (0x47)	ICR1H	Timer/Counter1 – Input Capture Register High Byte								112
0x26 (0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low Byte								112
0x25 (0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	126
0x24 (0x44)	TCNT2	Timer/Counter2 (8 Bits)								128
0x23 (0x43)	OCR2	Timer/Counter2 Output Compare Register								129
0x22 (0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	129
0x21 (0x41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	40
0x20[1] (0x40)[1]	UBRRH	URSEL	–	–	–	UBRR[11:8]				166
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	164
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	17
0x1E (0x3E)	EEARL	EEPROM Address Register Low Byte								17
0x1D (0x3D)	EEDR	EEPROM Data Register								17
0x1C (0x3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	17
0x1B (0x3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	64
0x1A (0x3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	64
0x19 (0x39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	64
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	64
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	64
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	65
0x15 (0x35)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	65
0x14 (0x34)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	65
0x13 (0x33)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	65
0x12 (0x32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	65
0x11 (0x31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	65
0x10 (0x30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	65
0x0F (0x2F)	SPDR	SPI Data Register								140
0x0E (0x2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	140
0x0D (0x2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	138
0x0C (0x2C)	UDR	USART I/O Data Register								161
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	162
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	163
0x09 (0x29)	UBRRL	USART Baud Rate Register Low Byte								166
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	200
0x07 (0x27)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	216
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	218
0x05 (0x25)	ADCH	ADC Data Register High Byte								219
0x04 (0x24)	ADCL	ADC Data Register Low Byte								219
0x03 (0x23)	TWDR	Two-wire Serial Interface Data Register								180
0x02 (0x22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	180
0x01 (0x21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	180

Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x00 (0x20)	TWBR	Two-wire Serial Interface Bit Rate Register								178

Notes:
1. Refer to the USART description for details on how to access UBRRH and UCSRC.
2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.