LIST PROGRAM PENGUJI MCB PADA VB 6.0

```
Private Sub Apply_Click()

Timer3.Interval = 1000 / Val(speed_tension.Text)

End Sub


Private Sub connect_Click()

If MSComm1.PortOpen = False Then MSComm1.PortOpen = True

End Sub


Private Sub DISCONNECT_Click()

If MSComm1.PortOpen = True Then MSComm1.PortOpen = False

End Sub


Private Sub EXIT_Click()

End

End Sub


Private Sub Form_Load()

Timer1.Enabled = False

Timer2.Enabled = False

Timer3.Enabled = False

slewrate.Text = 1

End Sub


Private Sub Print_Click()

PrintForm

End Sub


Private Sub SEND_Click()

'If MSComm1.PortOpen = True Then MSComm1.Output = Chr(Val(Text3.Text) * 5)


'Text4.Text = Chr(Text3.Text)

End Sub

Private Sub speed_Change()

Timer1.Interval = Val(speed.Text) * 1000

End Sub


Private Sub Start_Click()

Timer1.Enabled = True

Timer2.Enabled = True

Timer3.Enabled = True

End Sub


Private Sub Stop_Click()

Timer1.Enabled = False

Timer2.Enabled = False

Timer3.Enabled = False

End Sub


Private Sub Timer1_Timer()

MSChart1.Data = (Text1.Text)

Force.AddItem (Val(Text1.Text))

Text2.Text = Time

Time.AddItem (Abs(Time_counter) / 2)

rtfText.Text = rtfText.Text + "," + Text1.Text + Chr$(13) + Text2.Text


If (Val(Time_counter) / 2) > 120 Then

Timer1.Enabled = False

Timer2.Enabled = False

End If

End Sub


Private Sub Timer2_Timer()
```

```
Time_counter = Val(Time_counter) + 1

If MSComm1.PortOpen = True Then MSComm1.Output = (Chr(Val(bufferslew.Text) * 5)+128)

Text5.Text = (Val(bufferslew.Text) * 50)

Text1.Text = Asc(MSComm1.Input) / 12

End Sub

Private Sub Timer3_Timer()

If Val(bufferslew.Text) < Val(Text3.Text) Then bufferslew.Text = Val(bufferslew.Text) + 0.01

End Sub
```

- # LIST PROGRAM PADA CODEVISION AVR (CLIENT)

```
/*****************************************************
This program was produced by the
CodeWizardAVR V1.25.3 Professional
Automatic Program Generator
© Copyright 1998-2007 Pavel Haiduc, HP InfoTech s.r.l.
http://www.hpinfotech.com

Project :
Version :
Date    : 1/29/2009
Author  : F4CG
Company : F4CG
Comments:


Chip type           : ATmega16
Program type        : Application
Clock frequency     : 11.059200 MHz
Memory model        : Small
External SRAM size  : 0
Data Stack size     : 256
*****************************************************/

#include <mega16.h>
#include <delay.h>
char getchar(void);

#define RXB8 1
#define TXB8 0
#define UPE 2
#define OVR 3
#define FE 4
#define UDRE 5
#define RXC 7

#define FRAMING_ERROR (1<<FE)
#define PARITY_ERROR (1<<UPE)
#define DATA_OVERRUN (1<<OVR)
#define DATA_REGISTER_EMPTY (1<<UDRE)
#define RX_COMPLETE (1<<RXC)

// USART Receiver buffer
#define RX_BUFFER_SIZE 8
char rx_buffer[RX_BUFFER_SIZE];

#if RX_BUFFER_SIZE<256
unsigned char rx_wr_index,rx_rd_index,rx_counter;
#else
unsigned int rx_wr_index,rx_rd_index,rx_counter;
#endif

// This flag is set on USART Receiver buffer overflow
bit rx_buffer_overflow;

// USART Receiver interrupt service routine
interrupt [USART_RXC] void usart_rx_isr(void)
{
char status,data;
status=UCSRA;
data=UDR;
if ((status & (FRAMING_ERROR | PARITY_ERROR | DATA_OVERRUN))==0)
  {
  rx_buffer[rx_wr_index]=data;
  if (++rx_wr_index == RX_BUFFER_SIZE) rx_wr_index=0;
  if (++rx_counter == RX_BUFFER_SIZE)
     {
     rx_counter=0;
     rx_buffer_overflow=1;
     };
  };
PORTC = data;
getchar();
}

#ifndef _DEBUG_TERMINAL_IO_
// Get a character from the USART Receiver buffer
#define _ALTERNATE_GETCHAR_
#pragma used+
char getchar(void)
{
char data;
while (rx_counter==0);
data=rx_buffer[rx_rd_index];
if (++rx_rd_index == RX_BUFFER_SIZE) rx_rd_index=0;
#asm("cli")
--rx_counter;
#asm("sei")
return data;
}
#pragma used-
#endif

// Standard Input/Output functions
#include <stdio.h>

#define ADC_VREF_TYPE 0xC0

// Read the AD conversion result
unsigned int read_adc(unsigned char adc_input)
{
ADMUX=adc_input | (ADC_VREF_TYPE & 0xff);
// Start the AD conversion
ADCSRA|=0x40;
// Wait for the AD conversion to complete
```

```
while ((ADCSRA & 0x10)==0);
ADCSRA|=0x10;
return ADCW;
}

// Declare your global variables here

void main(void)
{
// Declare your local variables here

// Input/Output Ports initialization
// Port A initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTA=0x00;
DDRA=0x00;

// Port B initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTB=0x00;
DDRB=0x00;

// Port C initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTC=0x00;
DDRC=0xFF;

// Port D initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTD=0x00;
DDRD=0x00;

// Timer/Counter 0 initialization
// Clock source: System Clock
// Clock value: Timer 0 Stopped
// Mode: Normal top=FFh
// OC0 output: Disconnected
TCCR0=0x00;
TCNT0=0x00;
OCR0=0x00;

// Timer/Counter 1 initialization
// Clock source: System Clock
// Clock value: Timer 1 Stopped
// Mode: Normal top=FFFFh
// OC1A output: Discon.
// OC1B output: Discon.
// Noise Canceler: Off
// Input Capture on Falling Edge
// Timer 1 Overflow Interrupt: Off
// Input Capture Interrupt: Off
// Compare A Match Interrupt: Off
// Compare B Match Interrupt: Off
TCCR1A=0x00;
TCCR1B=0x00;
TCNT1H=0x00;
TCNT1L=0x00;
ICR1H=0x00;
ICR1L=0x00;
OCR1AH=0x00;
OCR1AL=0x00;
OCR1BH=0x00;
OCR1BL=0x00;

// Timer/Counter 2 initialization
// Clock source: System Clock
// Clock value: Timer 2 Stopped
// Mode: Normal top=FFh
// OC2 output: Disconnected
ASSR=0x00;
TCCR2=0x00;
TCNT2=0x00;
OCR2=0x00;

// External Interrupt(s) initialization
// INT0: Off
// INT1: Off
// INT2: Off
MCUCR=0x00;
MCUCSR=0x00;

// Timer(s)/Counter(s) Interrupt(s) initialization
TIMSK=0x00;

// USART initialization
// Communication Parameters: 8 Data, 1 Stop, No Parity
// USART Receiver: On
// USART Transmitter: On
// USART Mode: Asynchronous
// USART Baud rate: 9600
UCSRA=0x00;
UCSRB=0x98;
UCSRC=0x86;
UBRRH=0x00;
UBRRL=0x47;

// Analog Comparator initialization
// Analog Comparator: Off
// Analog Comparator Input Capture by Timer/Counter 1: Off
ACSR=0x80;
SFIOR=0x00;

// ADC initialization
// ADC Clock frequency: 86.400 kHz
```

```
// ADC Voltage Reference: Int., cap. on
AREF
// ADC Auto Trigger Source: None
ADMUX=ADC_VREF_TYPE & 0xff;
ADCSRA=0x87;

// Global enable interrupts
#asm("sei")
```

```
while (1)
      {
      // Place your code here
delay_ms(100);
putchar((read_adc(0)/4));
       }
}
```

LAMPIRAN C

Datasheet 2N3055, DAC 0802, LM 833, C945, D313

DATASHEET 2N3055

MOSPEC

COMPLEMENTARY SILICON POWER TRANSISTORS

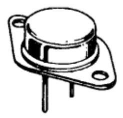
...designed for use in general-purpose amplifier and switching applications

FEATURES:

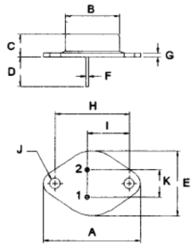
* Power Dissipation - P_D = 115W @ T_C = 25°C
* DC Current Gain hFE = 20 ~ 70 @ I_C = 4.0 A
* $V_{CE(sat)}$ = 1.1 V (Max.) @ I_C = 4.0 A, I_B = 400 mA

NPN	PNP
2N3055	MJ2955

15 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60 VOLTS
115 WATTS



TO-3



PIN 1.BASE
2.EMITTER
COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	38.75	39.96
B	19.28	22.23
C	7.96	9.28
D	11.18	12.19
E	25.20	26.67
F	0.92	1.09
G	1.38	1.62
H	29.90	30.40
I	16.64	17.30
J	3.88	4.36
K	10.67	11.18

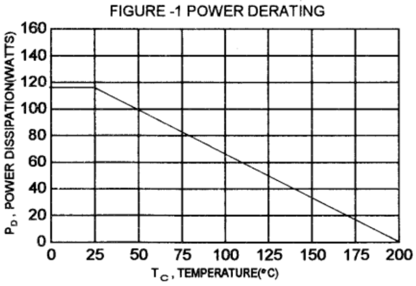
MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Collector-Emitter Voltage	V_{CEO}	60	V
Collector-Emitter Voltage	V_{CER}	70	V
Collector-Base Voltage	V_{CBO}	100	V
Emitter-Base Voltage	V_{EBO}	7.0	V
Collector Current-Continuous	I_C	15	A
Base Current	I_B	7.0	A
Total Power Dissipation @T_C=25°C Derate above 25°C	P_D	115 0.657	W W/°C
Operating and Storage Junction Temperature Range	T_J,T_{STG}	- 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	Rθjc	1.52	°C/W

FIGURE -1 POWER DERATING



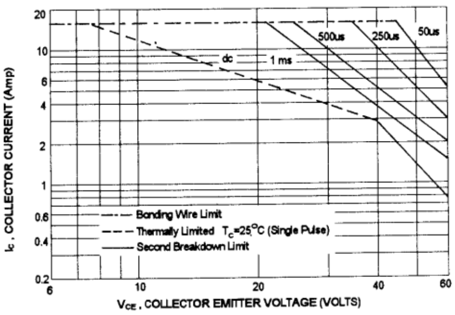
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector - Emitter Sustaining Voltage (1) (I_C = 200 mA, I_B = 0)	$V_{CEO(SUS)}$	60		V
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mA, R_{BE} = 100 Ohms)	$V_{CER(SUS)}$	70		V
Collector Cutoff Current (V_{CE} = 30 V, I_B = 0)	I_{CEO}		0.7	mA
Collector Cutoff Current (V_{CE} = 100 V, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 100 V, $V_{BE(off)}$ = 1.5 V ,T_C = 150°C)	I_{CEX}		1.0 5.0	mA
Emitter Cutoff Current (V_{EB} = 7.0 V , I_C = 0)	I_{EBO}		5.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 A , V_{CE} = 4.0 V) (I_C = 10 A , V_{CE} = 4.0 V)	hFE	20 5.0	70	
Collector - Emitter Saturation Voltage (I_C = 4.0 A , I_B = 0.4 A) (I_C = 10 A, I_B = 3.3 A)	$V_{CE(sat)}$		1.1 3.0	V
Base - Emitter On Voltage (I_C = 4.0 A, V_{CE} = 4.0 V)	$V_{BE(on)}$		1.5	V
DYNAMIC CHARACTERISTICS				
Current Gain - Bandwidth Product (2) (I_C = 500 mA, V_{CE} = 10 V , f = 1.0 MHz)	f_T	2.5		MHz
Small-Signal Current Gain (I_C = 1.0 A, V_{CE} = 4.0 V, f = 1 KHz)	h_{fe}	15	120	

(1) Pulse Test: Pulse width = 300 μs , Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \cdot f_{test}$

2N3055,MJ2955

ACTIVE REGION SAFE OPERATING AREA(SOA)



There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on $T_{J(PK)}$=200 °C;T_C is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)}$≤200°C, At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

DATASHEET DAC0802

![National Semiconductor] National Semiconductor

June 1999

DAC0800/DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

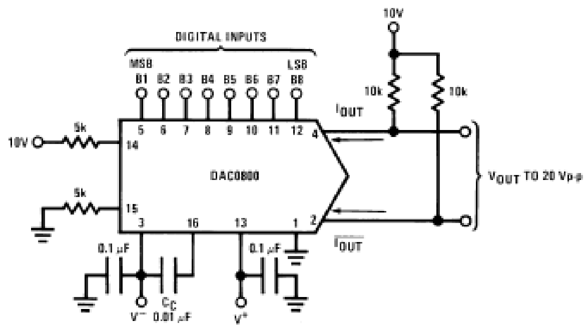
The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

Typical Applications



DS005686-1

FIGURE 1. ±20 V_{P-P} Output Digital-to-Analog Converter (Note 5)

Ordering Information

Non-Linearity	Temperature	Order Numbers				
	Range	J Package (J16A) (Note 1)		N Package (N16E) (Note 1)		SO Package (M16A)
±0.1% FS	0°C ≤ T_A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C ≤ T_A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (Note 3)	500 mW
Reference Input Differential Voltage	
(V14 to V15)	V^- to V^+
Reference Input Common-Mode	
Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs	
(V_S− = −15V)	4.25 mA
ESD Susceptibility (Note 4)	TBD V
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Conditions (Note 2)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	−55	+125	°C
DAC0800LC	0	+70	°C
DAC0802LC	0	+70	°C

Electrical Characteristics

The following specifications apply for V_S = ±15V, I_{REF} = 2 mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", T_A=25°C		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
tPLH, tPHL	Propagation Delay	T_A=25°C							
	Each Bit			35	60		35	60	ns
	All Bits Switched			35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50	ppm/°C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, R_{OUT}>20 MΩ Typ	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF}=10.000V, R14=5.000 kΩ R15=5.000 kΩ, T_A=25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4}-I_{FS2}$		±0.5	±4.0		±1	±8.0	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0	μA
I_{FSR}	Output Current Range	V^-=−5V	0	2.0	2.1	0	2.0	2.1	mA
		V^-=−8V to −18V	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels								
V_{IL}	Logic "0"	V_{LC}=0V			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			V
	Logic Input Current	V_{LC}=0V							
I_{IL}	Logic "0"	$-10V \le V_{IN} \le +0.8V$		−2.0	−10		−2.0	−10	μA
I_{IH}	Logic "1"	$2V \le V_{IN} \le +18V$		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	V^-=−15V	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S=±15V	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate	(*Figure 11*)	4.0	8.0		4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$4.5V \le V^+ \le 18V$		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		$-4.5V \le V^- \le 18V$ I_{REF}=1mA		0.0001	0.01		0.0001	0.01	%/%

Electrical Characteristics (Continued)

The following specifications apply for V_S = ±15V, I_{REF} = 2 mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Power Supply Current	V_S=±5V, I_{REF}=1 mA							
I+				2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8	mA
		V_S=5V, −15V, I_{REF}=2 mA							
I+				2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8	mA
		V_S=±15V, I_{REF}=2 mA							
I+				2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF}=1 mA		33	48		33	48	mW
		5V,−15V, I_{REF}=2 mA		108	136		108	136	mW
		±15V, I_{REF}=2 mA		135	174		135	174	mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

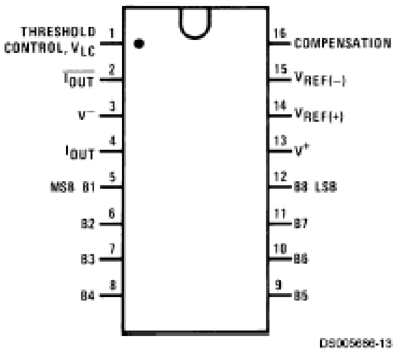
Note 3: The maximum junction temperature of the DAC0800 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded Dual-In-Line N package and 100°C/W for the Small Outline M package.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

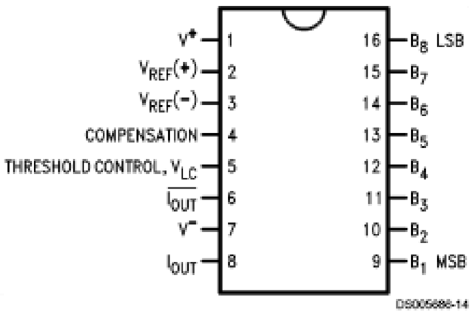
Connection Diagrams

Dual-In-Line Package



Top View

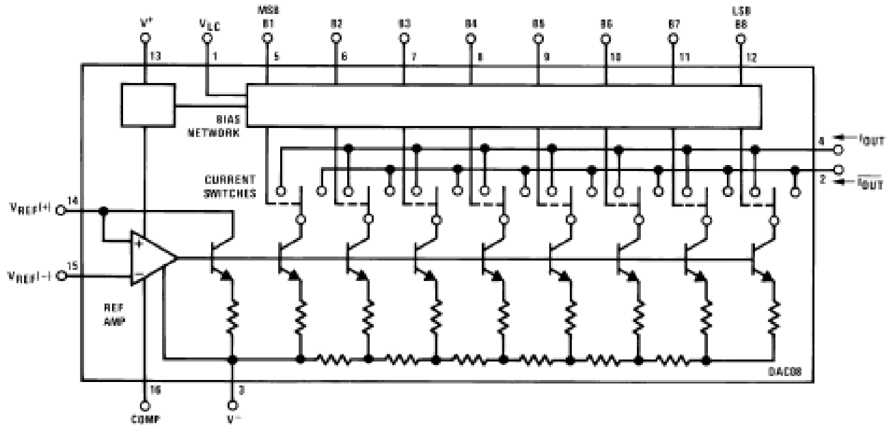
Small Outline Package



Top View

See Ordering Information

Block Diagram (Note 5)



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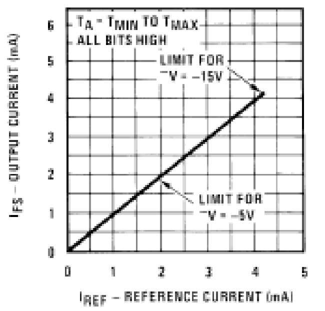
Typical Performance Characteristics

Full Scale Current vs Reference Current



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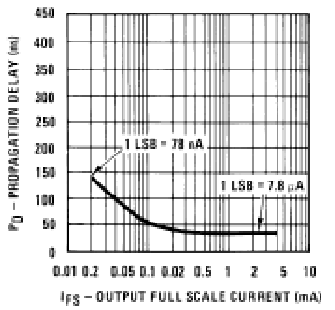
LSB Propagation Delay vs I_{FS}



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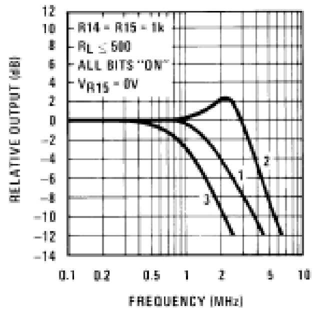
Reference Input Frequency Response



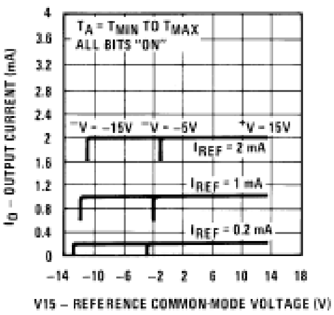
DS005686-24

Curve 1: C_C=15 pF, V_{IN}=2 Vp-p centered at 1V.

Curve 2: C_C=15 pF, V_{IN}=50 mVp-p centered at 200 mV.

Curve 3: C_C=0 pF, V_{IN}=100 mVp-p centered at 0V and applied through 50Ω connected to pin 14.2V applied to R14.

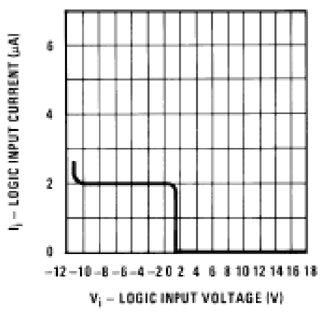
Reference Amp Common-Mode Range



DS005686-25

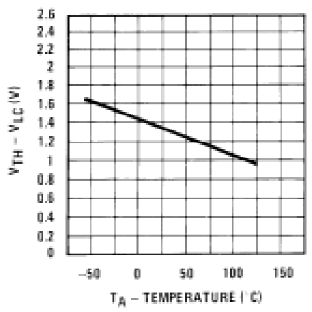
Note. Positive common-mode range is always (V+) − 1.5V.

Logic Input Current vs Input Voltage



DS005686-26

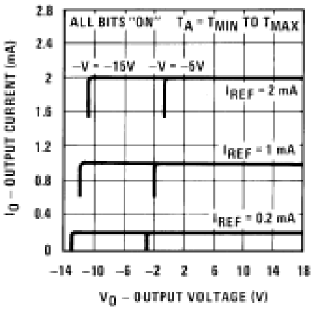
V_{TH} — V_{LC} vs Temperature



DS005686-27

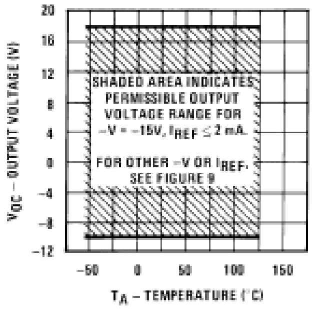
Typical Performance Characteristics (Continued)

Output Current vs Output Voltage (Output Voltage Compliance)



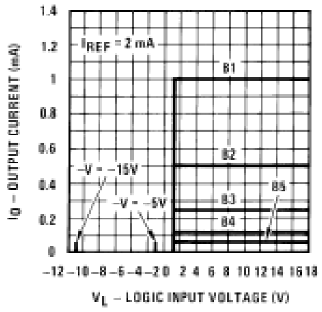
DS005686-28

Output Voltage Compliance vs Temperature



DS005686-29

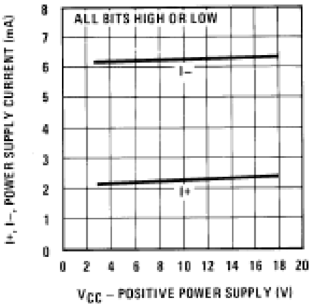
Bit Transfer Characteristics



DS005686-30

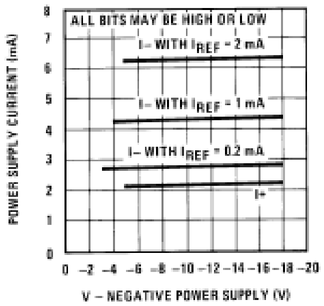
Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

Power Supply Current vs +V



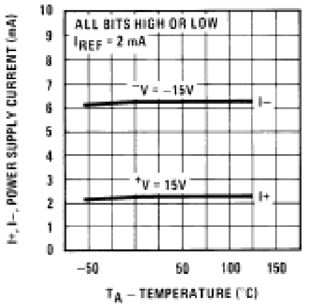
DS005686-31

Power Supply Current vs −V



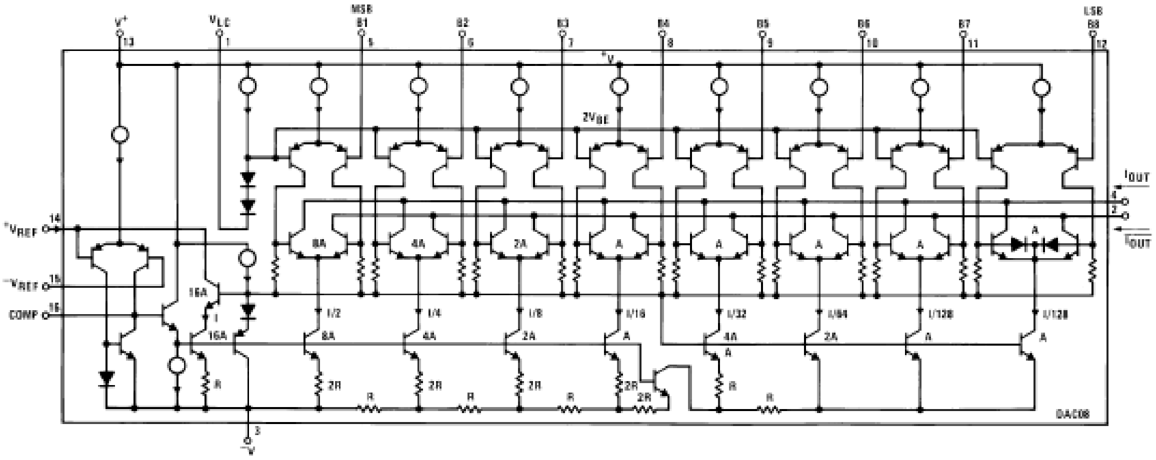
DS005686-32

Power Supply Current vs Temperature



DS005686-33

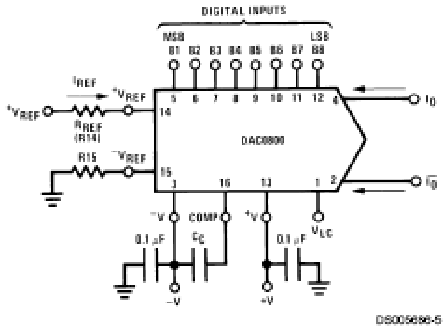
Equivalent Circuit



DS005686-15

FIGURE 2.

Typical Applications



$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$

$I_O + \bar{I}_O = I_{FS}$ for all logic states
For fixed reference, TTL operation, typical values are:
V_{REF} = 10.000V
R_{REF} = 5.000k
$R15 \approx R_{REF}$
C_C = 0.01 µF
V_{LC} = 0V (Ground)

FIGURE 3. Basic Positive Reference Operation (Note 5)

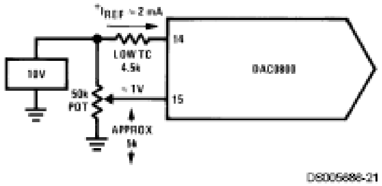
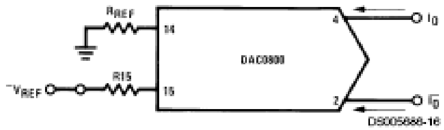


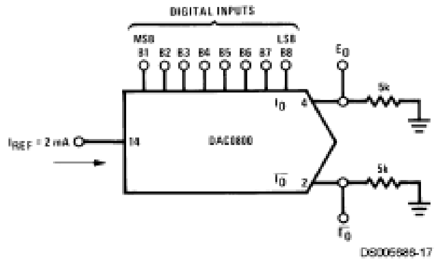
FIGURE 4. Recommended Full Scale Adjustment Circuit (Note 5)



$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

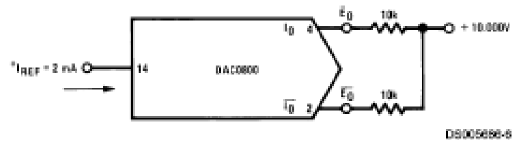
FIGURE 5. Basic Negative Reference Operation (Note 5)



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\bar{I}_O$mA	E_O	$\bar{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

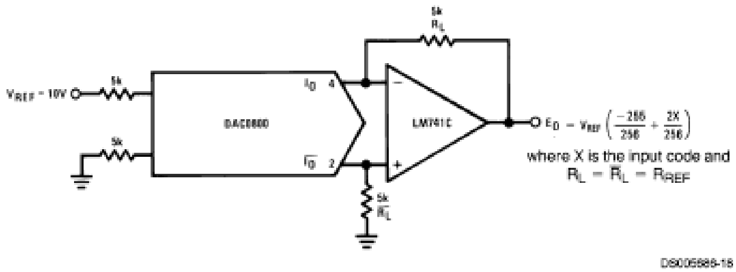
FIGURE 6. Basic Unipolar Negative Operation (Note 5)

Typical Applications (Continued)



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

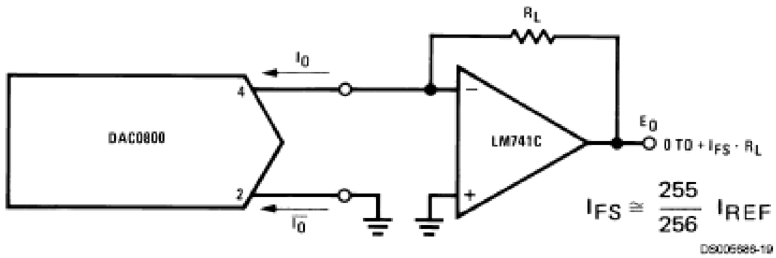
FIGURE 7. Basic Bipolar Output Operation (Note 5)



If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−)Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	−9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.960

FIGURE 8. Symmetrical Offset Binary Operation (Note 5)



For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

FIGURE 9. Positive Low Impedance Output Operation (Note 5)

DATASHEET LM 833

National Semiconductor

January 2003

LM833 Dual Audio Operational Amplifier

LM833
Dual Audio Operational Amplifier

General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

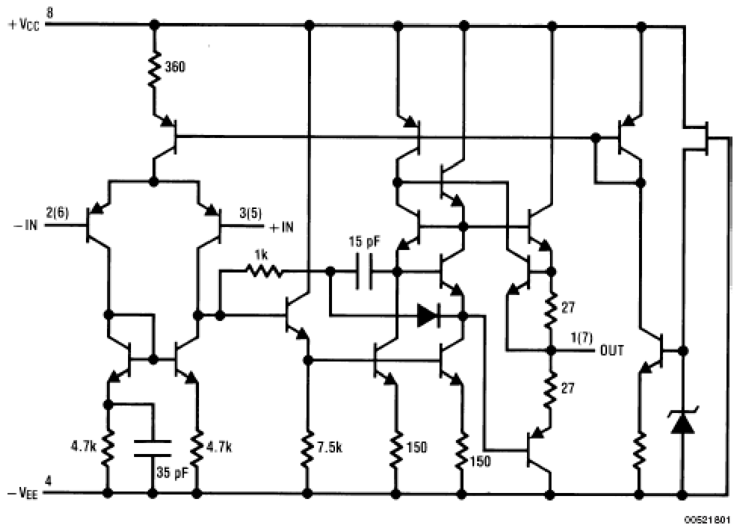
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide band-width without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

Features

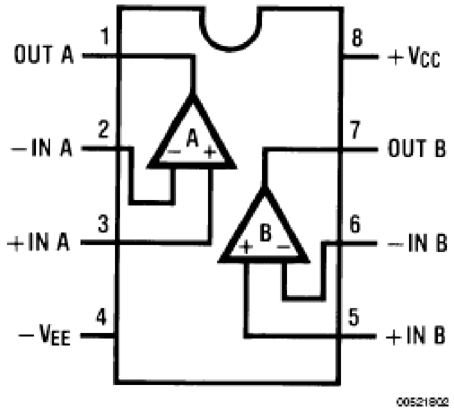
- Wide dynamic range: >140dB
- Low input noise voltage: 4.5nV/√Hz
- High slew rate: 7 V/µs (typ); 5V/µs (min)
- High gain bandwidth: 15MHz (typ); 10MHz (min)
- Wide power bandwidth: 120KHz
- Low distortion: 0.002%
- Low offset voltage: 0.3mV
- Large phase margin: 60°
- Available in 8 pin MSOP package

Schematic Diagram (1/2 LM833)



 DS005218 www.national.com

Connection Diagram



Order Number LM833M, LM833MX, LM833N, LM833MM or LM833MMX
See NS Package Number
M08A, N08E or MUA08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{CC}–V_{EE}	36V
Differential Input Voltage (Note 3) V_I	±30V
Input Voltage Range (Note 3) V_{IC}	±15V
Power Dissipation (Note 4) P_D	500 mW
Operating Temperature Range T_{OPR}	−40 ~ 85°C
Storage Temperature Range T_{STG}	−60 ~ 150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package (SOIC and MSOP)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD tolerance (Note 5)	1600V

DC Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ	±12	±13.5		V
		R_L = 2 kΩ	±10	±13.4		V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15~5V, −15~−5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

AC Electrical Characteristics

(T_A = 25°C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz	10	15		MHz

Design Electrical Characteristics

(T_A = 25°C, V_S = ±15V) The following parameters are not tested or guaranteed.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	μV/°C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1 kHz	4.5	$nV/\sqrt{Hz}$
i_n	Input Referred Noise Current	f = 1 kHz	0.7	$pA/\sqrt{Hz}$
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
ϕ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

DATASHEET C945

NPN general purpose transistor — 2PC945

FEATURES

- Low current (max. 100 mA)
- Low voltage (max. 50 V).

APPLICATIONS

- General purpose switching and amplification.

DESCRIPTION

NPN transistor in a TO-92 (SOT54) plastic package.
PNP complement: 2PA733.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter

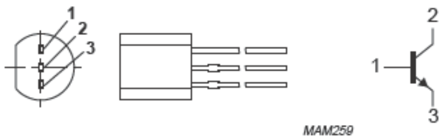


Fig.1 Simplified outline (TO-92; SOT54) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).s

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)		–	100	mA
I_{CM}	peak collector current		–	200	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.