LM124/LM224/LM324/LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage
- range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

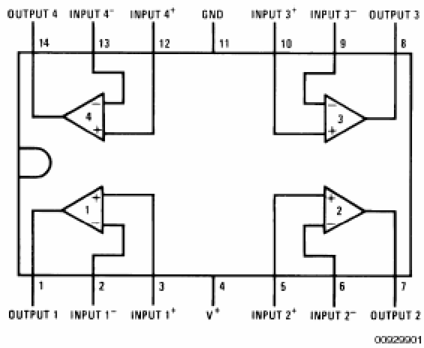
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range: Single supply 3V to 32V or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V_{+} - 1.5V

Connection Diagrams

Dual-In-Line Package

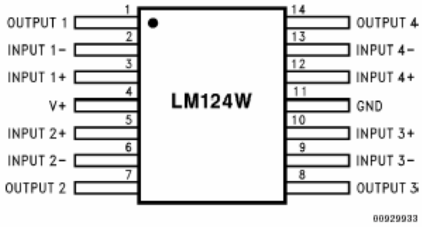


Top View

Order Number LM124J, LM124AJ, LM124J/883 (Note 2), **LM124AJ/883** (Note 1), **LM224J, LM224AJ, LM324J, LM324M, LM324MX, LM324AM, LM324AMX, LM2902M, LM2902MX, LM324N, LM324AN, LM324MT, LM324MTX or LM2902N LM124AJRQML and LM124AJRQMLV**(Note 3)

See NS Package Number J14A, M14A or N14A

Connection Diagrams (Continued)



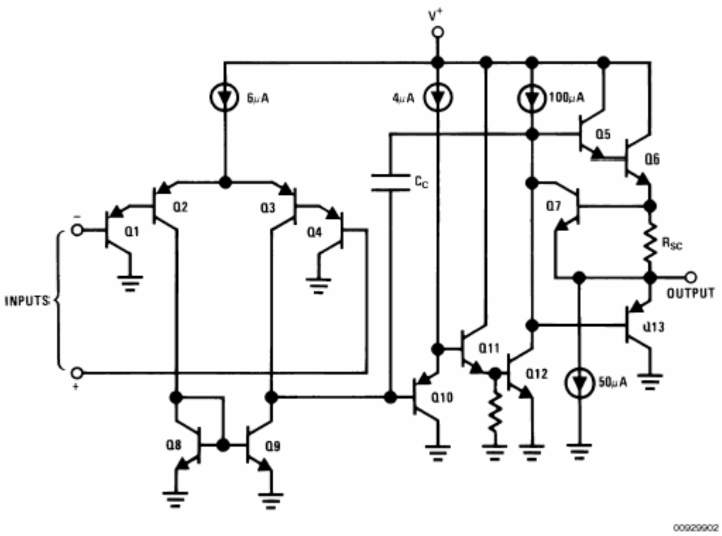
Order Number LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
LM124AWRQML and LM124AWRQMLV(Note 3)
See NS Package Number W14B
LM124AWGRQML and LM124AWGRQMLV(Note 3)
See NS Package Number WG14A

Note 1: LM124A available per JM38510/11006

Note 2: LM124 available per JM38510/11005

Note 3: See STD Mil DWG 5962R99504 for Radiation Tolerant Device

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Input Current		
($V_{IN} < -0.3V$) (Note 6)	50 mA	50 mA
Power Dissipation (Note 4)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND		
(One Amplifier) (Note 5)		
$V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 13)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) $T_A = 25°C$		1	2		1	3		2	3	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		20	50		40	80		45	100	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		2	15		5	30	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps										mA
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)		1.5	3		1.5	3		1.5	3	
	$V^+ = 5V$		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15V$, $R_L \geq 2k\Omega$, (V_O = 1V to 11V), $T_A = 25°C$	50	100		50	100		25	100		V/mV
Common-Mode	DC, V_{CM} = 0V to $V^+ - 1.5V$,	70	85		70	85		65	85		dB

Electrical Characteristics (Continued)

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124A Min	LM124A Typ	LM124A Max	LM224A Min	LM224A Typ	LM224A Max	LM324A Min	LM324A Typ	LM324A Max	Units
Rejection Ratio	$T_A = 25°C$										
Power Supply Rejection Ratio	$V^+ = 5V$ to 30V (LM2902, $V^+ = 5V$ to 26V), $T_A = 25°C$	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling (Note 11)	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120		dB
Output Current, Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		20	40		mA
Output Current, Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	10	20		10	20		10	20		mA
	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 200$ mV, $T_A = 25°C$	12	50		12	50		12	50		μA
Short Circuit to Ground	(Note 5) $V^+ = 15V$, $T_A = 25°C$		40	60		40	60		40	60	mA
Input Offset Voltage	(Note 8)			4			4			5	mV
V_{OS} Drift	$R_S = 0\Omega$		7	20		7	20		7	30	μV/°C
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			30			30			75	nA
I_{OS} Drift	$R_S = 0\Omega$		10	200		10	200		10	300	pA/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = +30V$ (LM2902, $V^+ = 26V$)	0		V^+-2	0		V^+-2	0		V^+-2	V
Large Signal Voltage Gain	$V^+ = +15V$ (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ	25			25			15			V/mV
Output Voltage Swing, V_{OH}	$V^+ = 30V$, $R_L = 2$ kΩ	26			26			26			V
	(LM2902, $V^+ = 26V$), $R_L = 10$ kΩ	27	28		27	28		27	28		V
Output Voltage Swing, V_{OL}	$V^+ = 5V$, $R_L = 10$ kΩ		5	20		5	20		5	20	mV
Output Current, Source	$V_O = 2V$, $V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$	10	20		10	20		10	20		mA
Output Current, Sink	$V_O = 2V$, $V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$	10	15		5	8		5	8		mA

Electrical Characteristics

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124/LM224 Min	LM124/LM224 Typ	LM124/LM224 Max	LM324 Min	LM324 Typ	LM324 Max	LM2902 Min	LM2902 Typ	LM2902 Max	Units
Input Offset Voltage	(Note 8) $T_A = 25°C$		2	5		2	7		2	7	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V

Electrical Characteristics (Continued)

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter		Conditions		LM124/LM224 Min	LM124/LM224 Typ	LM124/LM224 Max	LM324 Min	LM324 Typ	LM324 Max	LM2902 Min	LM2902 Typ	LM2902 Max	Units
Supply Current		Over Full Temperature Range $R_L = \infty$ On All Op Amps											mA
		$V^+ = 30V$ (LM2902 $V^+ = 26V$)			1.5	3		1.5	3		1.5	3	
		$V^+ = 5V$			0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain		$V^+ = 15V$, $R_L \geq 2k\Omega$, (V_O = 1V to 11V), $T_A = 25°C$		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio		DC, V_{CM} = 0V to $V^+ - 1.5V$, $T_A = 25°C$		70	85		65	85		50	70		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2902, V^+ = 5V to 26V), $T_A = 25°C$		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 11)		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$		20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$		10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 200$ mV, $T_A = 25°C$		12	50		12	50		12	50		μA
Short Circuit to Ground		(Note 5) $V^+ = 15V$, $T_A = 25°C$			40	60		40	60		40	60	mA
Input Offset Voltage		(Note 8)				7			9			10	mV
V_{OS} Drift		$R_S = 0\Omega$			7			7			7		μV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$				100			150		45	200	nA
I_{OS} Drift		$R_S = 0\Omega$			10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (Note 10)		$V^+ = +30V$ (LM2902, $V^+ = 26V$)		0		V^+-2	0		V^+-2	0		V^+-2	V
Large Signal Voltage Gain		$V^+ = +15V$ (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = 30V$	$R_L = 2$ kΩ	26			26			22			V
		(LM2902, $V^+ = 26V$)	$R_L = 10$ kΩ	27	28		27	28		23	24		V
	V_{OL}	$V^+ = 5V$, $R_L = 10$ kΩ			5	20		5	20		5	100	mV
Output Current	Source	$V_O = 2V$	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$	10	20		10	20		10	20		mA
	Sink		$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$	5	8		5	8		5	8		mA

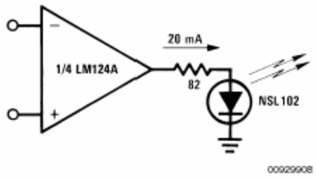
Note 4: For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 5: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

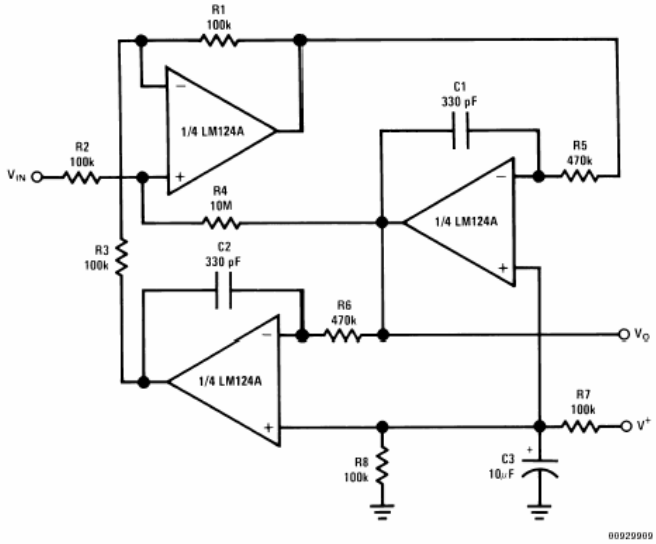
Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action

Typical Single-Supply Applications (V+ = 5.0 V_{DC}) (Continued)

LED Driver



"BI-QUAD" RC Active Bandpass Filter

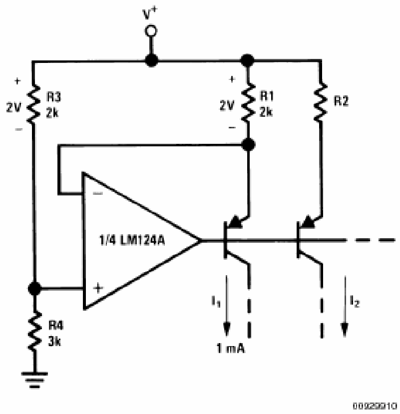


f_O = 1 kHz

Q = 50

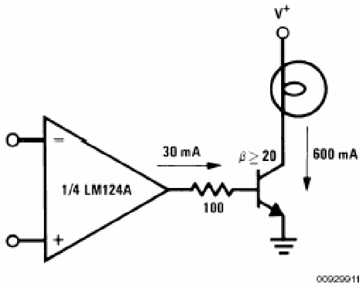
A_V = 100 (40 dB)

Fixed Current Sources



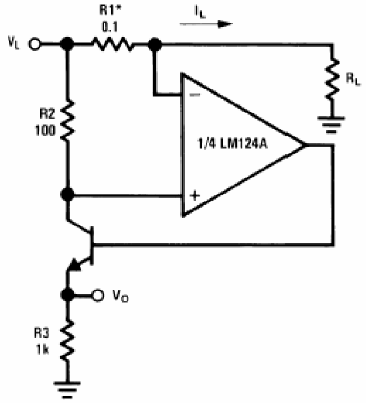
$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Lamp Driver



Typical Single-Supply Applications
($V^+ = 5.0\ V_{DC}$) (Continued)

Current Monitor



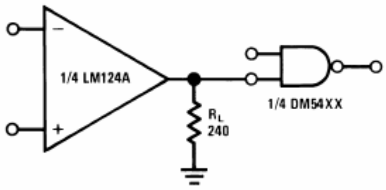
00929912

$$V_O = \frac{1V(I_L)}{1A}$$

$$V_L \leq V^+ - 2V$$

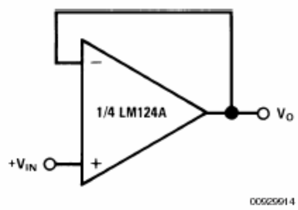
*(Increase R1 for I_L small)

Driving TTL



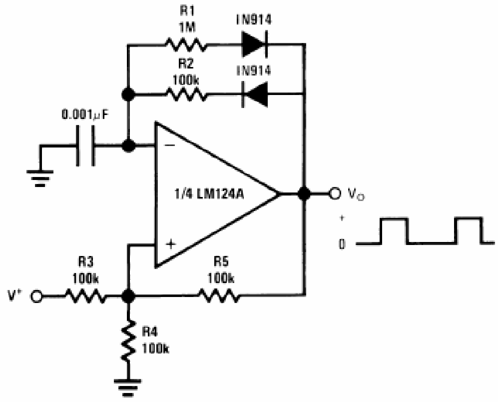
00929913

Voltage Follower



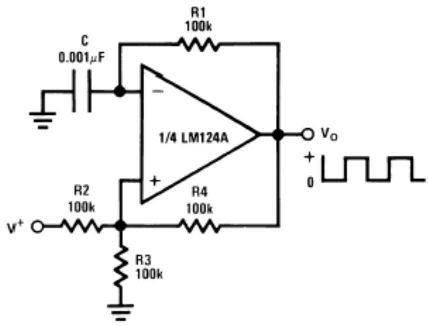
00929914

Pulse Generator



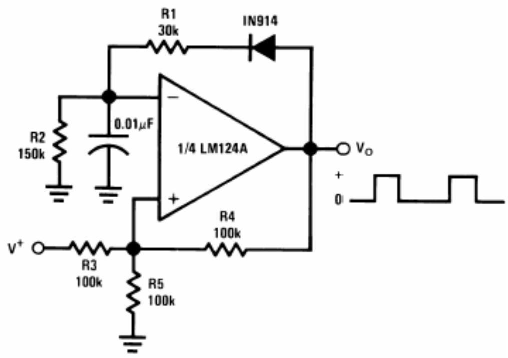
00929915

Squarewave Oscillator



00929916

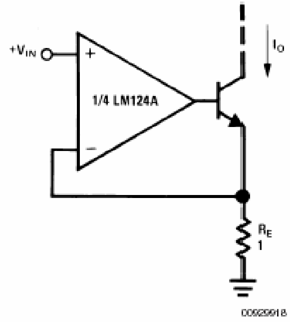
Pulse Generator



00929917

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

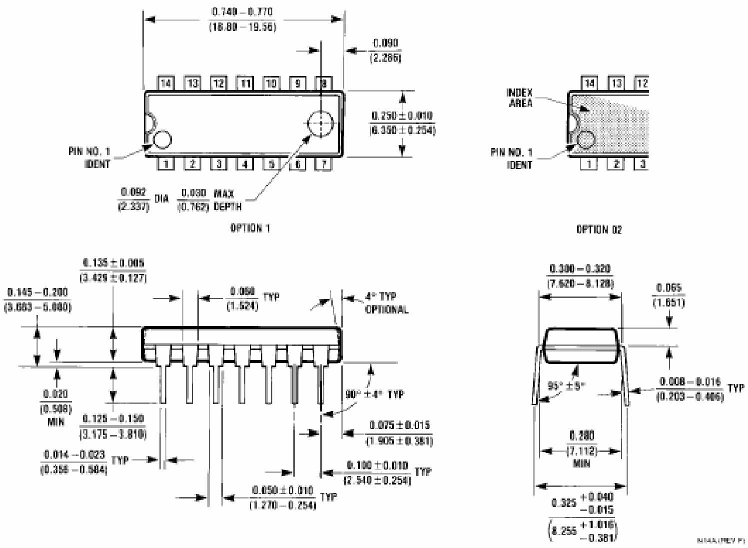
High Compliance Current Sink



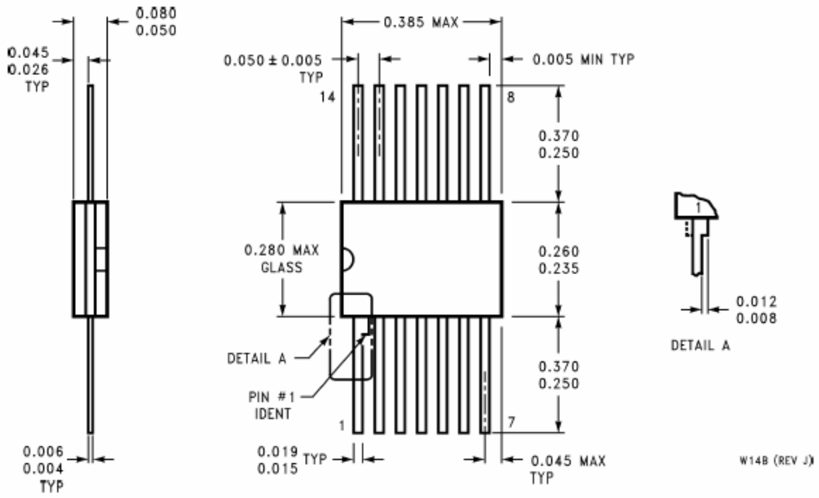
I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

Low Drift Peak Detector

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LM324N, LM324AN or LM2902N
NS Package Number N14A



Ceramic Flatpak Package
Order Number JL124ABDA, JL124ABZA, JL124ASDA, JL124BDA, JL124BZA, JL124SDA, LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
NS Package Number W14B

8-bit Microcontroller with 8K Bytes In-System Programmable Flash

AT89S52

Features

- Compatible with MCS-51® Products
- 8K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 1000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 256 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-bit Timer/Counters
- Eight Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag

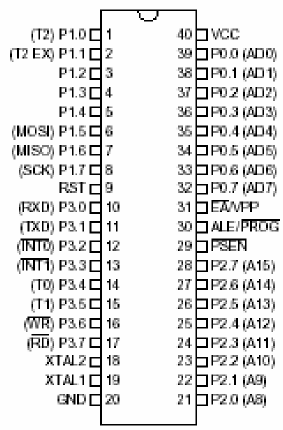
Description

The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

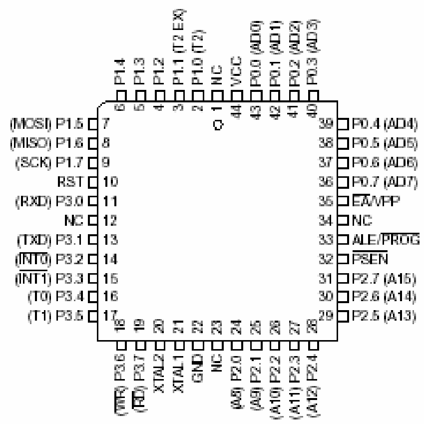
The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

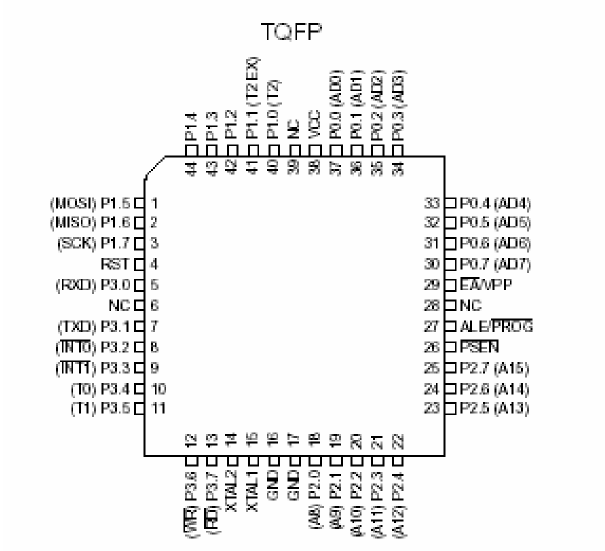
Pin Configurations

PDIP

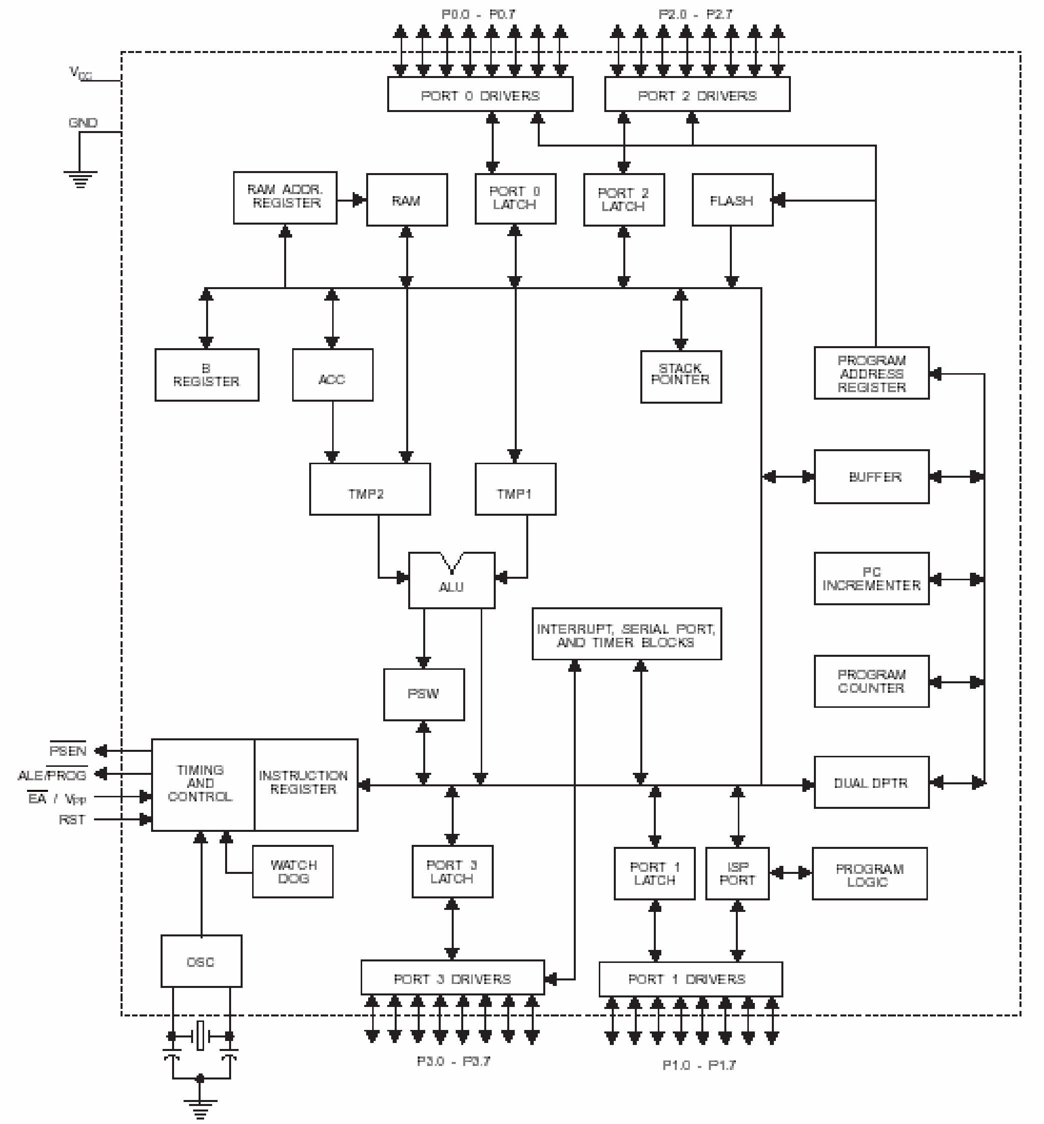


PLCC





Block Diagram



Pin Description

VCC
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)
P1.5	MOSI (used for In-System Programming)
P1.6	MISO (used for In-System Programming)
P1.7	SCK (used for In-System Programming)

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89S52, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 96 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/$\overline{\text{PROG}}$
Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable ($\overline{PSEN}$) is the read strobe to external program memory.

When the AT89S52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/VPP

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH.

Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Table 1. AT89S52 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111		AUXR1 XXXXXXX0				WDTRST XXXXXXXX		0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000	AUXR XXX00XX0		8FH
80H	P0 11111111	SP 00000111	DP0L 00000000	DP0H 00000000	DP1L 00000000	DP1H 00000000		PCON 0XXX0000	87H

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 3) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON – Timer/Counter 2 Control Register

T2CON Address = 0C8H Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
$C/\overline{T2}$	Timer or counter select for Timer 2. $C/\overline{T2}$ = 0 for timer function. $C/\overline{T2}$ = 1 for external event counter (falling edge triggered).
$CP/\overline{RL2}$	Capture/Reload select. $CP/\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. $CP/\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 3a. AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

	–	–	–	WDIDLE	DISRTO	–	–	DISALE
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion	
DISALE	Disable/Enable ALE	
	DISALE	Operating Mode
	0	ALE is emitted at a constant rate of 1/6 the oscillator frequency
	1	ALE is active only during a MOVX or MOVC instruction
DISRTO	Disable/Enable Reset out	
	DISRTO	
	0	Reset pin is driven High after WDT times out
	1	Reset pin is input only
WDIDLE	Disable/Enable WDT in IDLE mode	
	WDIDLE	
	0	WDT continues to count in IDLE mode
	1	WDT halts counting in IDLE mode

Dual Data Pointer Registers: To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should always initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag: The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Table 3b. AUXR1: Auxiliary Register 1

AUXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

	–	–	–	–	–	–	–	DPS
Bit	7	6	5	4	3	2	1	0

–	Reserved for future expansion	
DPS	Data Pointer Register Select	
	DPS	
	0	Selects DPTR Registers DP0L, DP0H
	1	Selects DPTR Registers DP1L, DP1H

Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 9. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit $C/\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Frequency}}{4 \times [65536-(\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

Interrupts

The AT89S52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 10.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. In the AT89S52, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

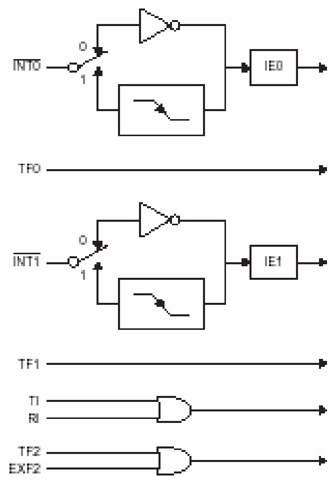
(MSB)							(LSB)
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

Figure 10. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 12. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

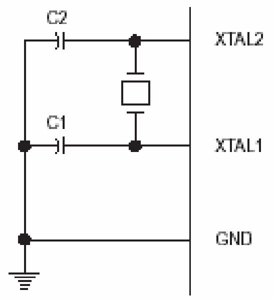
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by an enabled external interrupt. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 11. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 12. External Clock Drive Configuration

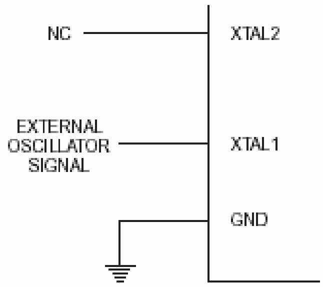


Table 6. Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89S52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Table 7. Lock Bit Protection Modes

Program Lock Bits	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled
3	P	P	U	Same as mode 2, but verify is also disabled
4	P	P	P	Same as mode 3, but external execution is also disabled

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash – Parallel Mode

The AT89S52 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S52 code memory array is programmed byte-by-byte.

Programming Algorithm: Before programming the AT89S52, the address, data, and control signals should be set up according to the Flash programming mode table and Figures 13 and 14. To program the AT89S52, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 μs.

Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{\text{Data}}$ Polling: The AT89S52 features $\overline{\text{Data}}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate BUSY. P3.0 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The status of the individual lock bits can be verified directly by reading them back.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 52H indicates 89S52
(200H) = 06H

Chip Erase: In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{PROG}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to V_{CC}. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

Serial Programming Algorithm

To program and verify the AT89S52 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:

   Apply power between VCC and GND pins.

   Set RST pin to "H".

   If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.
2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. The write cycle is self-timed and typically takes less than 1 ms at 5V.
4. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/P1.6.
5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

Set XTAL1 to "L" (if a crystal is not used).

Set RST to "L".

Turn V_{CC} power off.

$\overline{\text{Data}}$ Polling: The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in Table 10.

Order this document by ULN2803/D

MOTOROLA

ULN2803
ULN2804

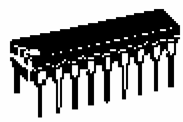
Octal High Voltage, High Current Darlington Transistor Arrays

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open–collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

OCTAL PERIPHERAL DRIVER ARRAYS

SEMICONDUCTOR TECHNICAL DATA



A SUFFIX
PLASTIC PACKAGE
CASE 707

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package, unless otherwise noted.)

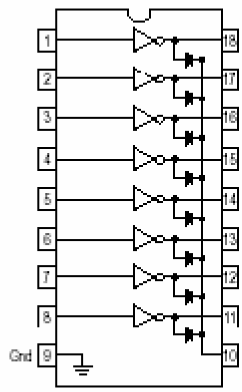
Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Junction Temperature	T_J	125	°C

$R_{\theta JA}$ = 55°C/W
Do not exceed maximum current limit per driver.

ORDERING INFORMATION

Device	Characteristics		
	Input Compatibility	V_{CE}(Max)/I_C(Max)	Operating Temperature Range
ULN2803A ULN2804A	TTL, 5.0 V CMOS 6 to 15 V CMOS, PMOS	50 V/500 mA	T_A = 0 to + 70°C

PIN CONNECTIONS



ULN2803 ULN2804

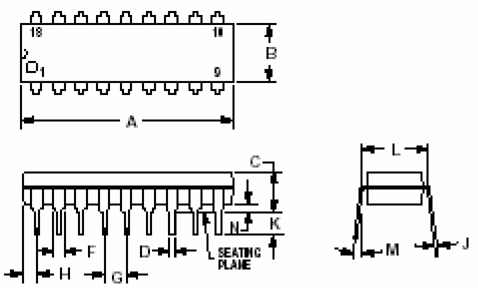
ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current (Figure 1)		I_{CEX}				µA
(V_O = 50 V, T_A = +70°C)	All Types		–	–	100	
(V_O = 50 V, T_A = +25°C)	All Types		–	–	50	
(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	ULN2802		–	–	500	
(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	ULN2804		–	–	500	
Collector–Emitter Saturation Voltage (Figure 2)		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 µA)	All Types		–	1.1	1.6	
(I_C = 200 mA, I_B = 350 µA)	All Types		–	0.95	1.3	
(I_C = 100 mA, I_B = 250 µA)	All Types		–	0.85	1.1	
Input Current – On Condition (Figure 4)		$I_{I(on)}$				mA
(V_I = 17 V)	ULN2802		–	0.82	1.25	
(V_I = 3.85 V)	ULN2803		–	0.93	1.35	
(V_I = 5.0 V)	ULN2804		–	0.35	0.5	
(V_I = 12 V)	ULN2804		–	1.0	1.45	
Input Voltage – On Condition (Figure 5)		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2802		–	–	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2803		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	ULN2803		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2803		–	–	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	ULN2804		–	–	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2804		–	–	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	ULN2804		–	–	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	ULN2804		–	–	8.0	
Input Current – Off Condition (Figure 3) (I_C = 500 µA, T_A = +70°C)	All Types	$I_{I(off)}$	50	100	–	µA
DC Current Gain (Figure 2) (V_{CE} = 2.0 V, I_C = 350 mA)	ULN2801	h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	25	pF
Turn–On Delay Time (50% E_I to 50% E_O)		t_{on}	–	0.25	1.0	µs
Turn–Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	0.25	1.0	µs
Clamp Diode Leakage Current (Figure 6) (V_R = 50 V)	T_A = +25°C	I_R	–	–	50	µA
	T_A = +70°C				100	
Clamp Diode Forward Voltage (Figure 7) (I_F = 350 mA)		V_F	–	1.5	2.0	V

ULN2803 ULN2804

OUTLINE DIMENSIONS

A SUFFIX
PLASTIC PACKAGE
CASE 707–02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

Instruksi-instruksi Keluarga MCS51

A. Operasi Aritmatika

1. ADD

ADD A,Rn

Tambahkan Akumulator A dengan Rn di mana n = 0…7 dan simpan hasil di Akumulator A

Contoh:

Add A,R7

Isi dari R7 akan ditambahkan dengan akumulator A dan hasilnya disimpan di Akumulator A

ADD A,direct

Tambahkan Akumulator A dengan data di alamat memori tertentu secara langsung.

Contoh:

Add A,00H

Isi dari Akumulator A akan ditambahkan dengan isi dari memori RAM Internal di alamat 00H

ADD A,@Ri

Tambahkan Akumulator A dengan data yang berada di alamat Ri (ditunjuk oleh Ri) dan hasilnya disimpan di Akumulator A. Ri adalah Register Index di mana pada MCS51 adalah berupa R0 atau R1

Contoh:

Add A,@R0

Isi dari Akumulator A akan ditambahkan dengan isi dari memori RAM Internal yang ditunjuk oleh R0. Apabila R0 berisi 05H maka, isi dari alamat 05H akan dijumlahkan dengan Akumulator A dan hasilnya disimpan di Akumulator A

ADD A,#data

Tambahkan Akumulator A dengan sebuah konstanta dan hasilnya disimpan dalam akumulator A.

Contoh:

Add A,#05H

Isi Akumulator A ditambah dengan data 05H dan hasilnya disimpan dalam Akumulator A

2. ADDC

ADDC A,Rn

Tambahkan Akumulator A dengan Rn di mana n = 0…7 dan simpan hasil di Akumulator A

Contoh:

Addc A,R7

Isi dari R7 akan ditambahkan dengan akumulator A beserta carry flag dan hasilnya disimpan di Akumulator A. Apabila carry flag set maka hasil yang tersimpan di Akumulator A adalah A + R7 + 1.

ADDC A,direct

Tambahkan Akumulator A dan carry flag dengan data di alamat memori tertentu secara langsung.

Contoh:

Addc A,00H

Isi dari Akumulator A akan ditambahkan dengan isi dari memori RAM Internal di alamat 00H beserta carry flag dan hasilnya disimpan di Akumulator A, Apabila carry flag set maka hasil yang tersimpan di Akumulator A adalah A + isi alamat 00H + 1

ADDC A,@Ri

Tambahkan Akumulator A beserta carry flag dengan data yang berada di alamat Ri (ditunjuk oleh Ri) dan hasilnya disimpan di Akumulator A. Ri adalah Register Index di mana pada MCS51 adalah berupa R0 atau R1

ADDC A,#data

Tambahkan Akumulator A beserta carry flag dengan sebuah konstanta dan hasilnya disimpan dalam akumulator A.

Contoh:

Addc A,#05H Isi Akumulator A beserta carry flag ditambah dengan data 05H dan hasilnya disimpan dalam Akumulator A. Apabila carry flag set maka hasil di Akumulator A adalah A + 5H+ 1.

3. SUBB

SUBB A,Rn

Lakukan pengurangan data di Akumulator A dengan Rn (n = 0…7) dan simpan hasilnya di Akumulator A

Contoh:

Subb A,R0

Data di akumulator A beserta carry flagnya dikurangi dengan isi R0 dan hasilnya disimpan di Akumulator A

SUBB A,direct

Lakukan pengurangan data di Akumulator A dengan data di memori tertentu yang ditunjuk secara langsung.

Contoh:

Subb A,00H

Data di Akumulator A beserta carry flagnya dikurangi dengan data dialamat 00H dari RAM Internal dan hasilnya disimpan di Akumulator A

SUBB A,@Ri

Lakukan pengurangan data di Akumulator A beserta carry flag dengan data yang ditunjuk oleh Ri (Register Index) di mana Ri dapat berupa R0 atau R1

Contoh:

SUBB A,@R0

Data di Akumulator A beserta carry flagnya dikurangi dengan data yang ditunjuk oleh R0 dan hasilnya disimpan di Akumulator A

SUBB A,#data

Lakukan pengurangan data di Akumulator A beserta carry flag dengan sebuah konstanta dan hasilnya disimpan di Akumulator A

Contoh:

SUBB A,#05H

Data di Akumulator A beserta carry flag dikurangi dengan data 05H dan hasilnya disimpan di Akumulator A

4. INC

INC A

Tambahkan nilai Akumulator A dengan 1 dan hasilnya disimpan di Akumulator A

INC Rn

Tambahkan nilai Rn (n= 0…7) dengan 1 dan hasilnya disimpan di Rn tersebut

INC direct

Tambahkan data yang di RAM Internal yang alamatnya ditunjuk secara langsung dengan 1 dan hasilnya disimpan di alamat tersebut.

Contoh:

Inc 00H

Data di alamat 00H ditambah dengan 1 dan hasilnya disimpan di alamat 00H.

INC @Ri

Tambahkan data yang alamatnya ditunjuk oleh Ri (Register Index) dengan 1 dan simpan hasilnya di alamat tersebut.

Contoh:

Inc @R1

Data di alamat yang ditunjuk oleh R1 dan hasilnya disimpan di alamat tersebut, apabila R1 berisi 10H maka data di alamat 10H ditambah dengan 1 dan simpan kembali di alamat 10H.

INC DPTR

5. DEC

DEC A

Lakukan pengurangan pada nilai Akumulator A dengan 1 dan hasilnya disimpan di Akumulator A

DEC Rn

Lakukan pengurangan pada nilai Rn (n= 0…7) dengan 1 dan hasilnya disimpan di Rn tersebut

DEC direct

Lakukan pengurangan pada data yang di RAM Internal yang alamatnya ditunjuk secara langsung dengan 1 dan hasilnya disimpan di alamat tersebut.

Contoh:

Dec 00H

Data di alamat 00H dikurangi dengan 1 dan hasilnya disimpan di alamat 00H.

DEC @Ri

Lakukan pengurangan pada data yang alamatnya ditunjuk oleh Ri (Register Index) dengan 1 dan simpan hasilnya di alamat tersebut.

Contoh:

DEC @R1

Data di alamat yang ditunjuk oleh R1 dan hasilnya disimpan di alamat tersebut, apabila R1 berisi 10H maka data di alamat 10H dikurangi dengan 1 dan simpan kembali di
alamat 10H.

B. Operasi Logika dan Manipulasi Bit

1. ANL

ANL A,Rn

Melakukan operasi AND antara akumulator A dan Rn (R0…R7) dan hasilnya disimpan di akumulator A

ANL A,direct

Melakukan operasi AND antara akumulator A dan alamat langsung dan hasilnya disimpan di akumulator A.

Contoh:

ANL A,05H

Akumulator A di AND dengan data di alamat 05H dan hasilnya disimpan di akumulator A

ANL A,@Ri

Melakukan operasi AND antara akumulator A dan data yang ditunjuk oleh Register Index (R0 atau R1) serta hasilnya disimpan di akumulator A.

Contoh:

ANL A,@R0

Akumulator A di AND dengan data yang ditunjuk oleh R0, misalkan R0 berisi 50H, maka akumulator A di AND dengan data yang tersimpan di alamat 50H dan hasilnya disimpan di akumulator A.

ANL A,#data

Melakukan operasi AND antara akumulator A dan immediate data serta hasilnya disimpan di akumulator A

ANL direct,A

Melakukan operasi AND antara alamat langsung dengan akumulator A serta hasilnya disimpan di alamat langsung tersebut.

Contoh:

ANL 07H,A

Data di alamat 07H di AND dengan akumulator A dan hasilnya kembali disimpan di alamat 07H

ANL direct,#data

Melakukan operasi AND antara alamat langsung dengan immediate data serta hasilnya disimpan di alamat langsung tersebut.

2. ORL

ORL A,Rn

Melakukan operasi OR antara akumulator A dan Rn (R0…R7) dan hasilnya disimpan di akumulator A

ORL A,direct

Melakukan operasi OR antara akumulator A dan alamat langsung dan hasilnya disimpan di akumulator A.

Contoh:

ORL A,05H

Akumulator A di OR dengan data di alamat 05H dan hasilnya disimpan di akumulator A

ORL A,@Ri

Melakukan operasi OR antara akumulator A dan data yang ditunjuk oleh Register Index (R0 atau R1) serta hasilnya disimpan di akumulator A.

Contoh:

ORL A,@R0

Akumulator A di OR dengan data yang ditunjuk oleh R0, misalkan R0 berisi 50H, maka akumulator A di OR dengan data yang tersimpan di alamat 50H dan hasilnya disimpan di akumulator A.

ORL A,#data

Melakukan operasi OR antara akumulator A dan immediate data serta hasilnya disimpan di akumulator A

ORL direct,A

Melakukan operasi OR antara alamat langsung dengan akumulator A serta hasilnya disimpan di alamat langsung tersebut.

Contoh:

ORL 07H,A

Data di alamat 07H di OR dengan akumulator A dan hasilnya kembali disimpan di alamat 07H

ORL direct,#data

Melakukan operasi OR antara akumulator A dan immediate data serta hasilnya disimpan di akumulator A

3. CLR

CLR A

Memberikan nilai 0 pada 8 bit Akumulator A

4. CPL

CPL A

Melakukan komplemen pada setiap bit dalam akumulator A.

Contoh :

Bila nilai akumulator A adalah 55H atau 01010101b, maka setelah terjadi proses komplemen nilai akumulator A berubah menjadi AAH atau 10101010b.

5. RL

RL A

Melakukan pergeseran ke kiri 1 bit untuk setiap bit dalam akumulator A

Contoh:

Nilai Akumulator A adalah 05H atau 00000101b, setelah dilakukan proses pergeseran maka nilai Akumulator A akan berubah menjadi 00001010b atau 0AH.

6. RR

RR A

Melakukan pergeseran ke kanan 1 bit untuk setiap bit dalam akumulator A

Contoh:

Nilai Akumulator A adalah 05H atau 00000101b, setelah dilakukan proses pergeseran maka nilai Akumulator A akan berubah menjadi 10000010b atau 0AH.

7. SWAP

SWAP A

Melakukan operasi penukaran nibble tinggi dan nibble rendah di akumulator A

Contoh:

Isi akumulator A adalah 51H, setelah instruksi SWAP A dilakukan maka data 5 di nibble tinggi akan ditukar dengan data 1 di nibble rendah menadi 15H

8. SETB

SETB bit

Set bit atau mengubah bit-bit pada RAM Internal maupun register yang dapat dialamat secara bit (bit addressable) menjadi 1

9. JC

JC rel

Melakukan lompatan ke suatu alamat yang didefinisikan apabila carry flag set. Apabila carry flag clear maka program akan menjalankan instruksi selanjutnya.

Contoh:

Jc Alamat1

Mov A,#05H

Alamat1: Mov R1,#00H

Apabila carry flag set, maka program akan lompat label alamat 1 dan menjalankan instruksi Mov R1,#00H, namun bila carry flag clear maka program akan menjalankan instruksi Mov A,#05H terlebih dahulu sebelum menjalankan instruksi di label alamat 1.

10 JNC

JNC rel

Melakukan lompatan ke suatu alamat yang didefinisikan apabila carry flag clear. Apabila carry flag set maka program akan menjalankan instruksi selanjutnya.

Contoh:

Jnc Alamat1

Mov A,#05H

Alamat1: Mov R1,#00H

Apabila carry flag clear, maka program akan lompat label alamat 1 dan menjalankan instruksi Mov R1,#00H, namun bila carry flag set maka program akan menjalankan instruksi Mov A,#05H terlebih dahulu sebelum menjalankan instruksi di label alamat 1.

C. Transfer Data

1. MOV

MOV A,Rn

Melakukan pemindahan data dari Rn (R0…R7) menuju ke akumulator A

MOV A,direct

Melakukan pemindahan data dari alamat langsung ke akumulator A

Mov A,@Ri

Melakukan pemindahan data dari alamat yang ditunjuk oleh Register Index (R0 atau R1) menuju ke akumulator A

Mov A,#data

Melakukan pemindahan data dari immediate menuju ke akumulator A

Contoh:

Data EQU 05H

Mov A,#Data

Konstanta Data yang dideklarasikan sebagai 05H dipindah ke akumulator A sehingga nilai akumulator A menjadi 05H

Mov Rn,A

Melakukan pemindahan data dari akumulator A menuju ke Rn (R0…R7)

Mov Rn,direct

Melakukan pemindahan data dari alamat langsung menuju ke Rn (R0…R7)

Contoh:

Mov R7,10H

Data di alamat 10H dipindah ke dalam R7

Mov Rn,#data

Melakukan pemindahan data dari immediate menuju ke Rn (R0…R7)

Contoh:

Mov R7,#05H

Data 05H dipindah ke dalam R7

Mov direct,A

Melakukan pemindahan data dari akumulator A menuju ke alamat langsung

Contoh:

Mov 10H,A

Data di akumulator A dipindah ke alamat 10H

Mov direct,Rn

Melakukan pemindahan data dari Rn (R0…R7) menuju ke alamat langsung

Mov direct,direct

Melakukan pemindahan data dari alamat langsung menuju ke alamat langsung.

Mov direct,@Ri

Melakukan pemindahan data dari alamat yang ditunjuk oleh Register Index (R0 atau R1) ke alamat langsung

Contoh:

Mov 05H,@R0

Bila R0 sebelumnya berisi 20H, maka nilai atau data yang tersimpan di alamat 20H akan dipindah ke alamat 05H.

Mov direct,#data

Melakukan pemindahan data dari immediate ke alamat langsung.

Mov @Ri,A

Melakukan pemindahan data dari akumulator A menuju ke alamat yang ditunjuk oleh Register Index (R0 atau R1).

Mov @Ri,direct

Melakukan pemindahan data dari alamat langsung menuju ke alamat yang ditunjuk oleh Register Index (R0 atau R1)

Mov @Ri,#data

Melakukan pemindahan data immediate menuju ke alamat yang ditunjuk oleh Register Index (R0 atau R1)

Mov DPTR,#data16

Melakukan pemindahan data immediate 16 bit menuju ke DPTR.

Contoh:

Mov DPTR,#2000H

Data 2000H dalam bentuk 16 bit dipindah ke alamat Register DPTR

Movc A,@A+DPTR

Contoh:

Mov A,#50H

Mov DPTR,#2000H

Movc A,@A+DPTR

Data yang terletak di komponen memori di luar AT89S51 dan terletak pada alamat 2000H + 50H akan dibaca dan hasilnya disimpan di akumulator A

D. Percabangan

1. ACALL

ACALL addr11

Melakukan lompatan ke suatu subroutine yang ditunjuk oleh alamat pada addr11. Lompatan yang dapat dilakukan berada di area sebesar 2K byte.

2.RET

RET

Instruksi ini digunakan pada saat kembali dari subroutine yang dipanggil dengan instruksi ACALL atau LCALL.

RETI

Instruksi ini digunakan untuk melompat ke alamat tempat akhir instruksi yang sedang dijalankan ketika.

3. JUMP

LJMP addr16

Long Jump, melompat dan menjalankan program yang berada di alamat yang ditentukan oleh addr16.

Contoh:

LJMP Lompatan2

Mov A,#05H

Lompatan2: Mov R0,#00H

Program akan melompat ke alamat lompatan 2 dan menjalankan instruksi Mov R0,#00H, tanpa melalui instruksi MOV A,#05H

JZ rel

Melakukan lompatan ke alamat yang ditentukan apabila akumulator A adalah 00H dan langsung meneruskan instruksi dibawahnya bila akumulator A tidak 00H.

Contoh:

JZ Lompat1

MOV A,#07H

Lompat1: MOV B,#00H

Apabila nilai akumulator A tidak 00H maka program akan langsung meneruskan instruksi dibawahnya yaitu MOV A,#07H dan program akan menjalankan instruksi di alamat Lompat1 yaitu MOV B,#00H apabila nilai akumulator A adalah 00H.

JNZ rel

Melakukan lompatan ke alamat yang ditentukan apabila akumulator A adalah bukan 00H dan langsung meneruskan instruksi dibawahnya bila akumulator A adalah 00H.

Contoh:

JNZ Lompat1

MOV A,#07H

Lompat1: MOV B,#00H

Apabila nilai akumulator A adalah 00H maka program akan langsung meneruskan instruksi dibawahnya yaitu MOV A,#07H dan program akan menjalankan instruksi di alamat Lompat1 yaitu MOV B,#00H apabila nilai akumulator A adalah bukan 00H.

4. CJNE

Instruksi ini melakukan perbandingan antara data tujuan dan data sumber serta melakukan lompatan ke alamat yang ditentukan apabila hasil perbandingan tidak sama.

CJNE A,#data,rel

Melakukan perbandingan antara akumulator A dan data immediate serta melakukan lompatan ke alamat yang ditentukan apabila hasil perbandingan tidak sama.

Contoh:

CJNE A,#00H,lompat1

Program akan menuju ke alamat lompat 1 apabila data akumulator A tidak sama dengan data 00H..

5. DJNZ

DJNZ Rn,rel

Melakukan pengurangan pada Rn (R0…R7) dengan 1 dan lompat ke alamat yang ditentukan apabila hasilnya bukan 00.

Apabila hasilnya telah mencapai 00, maka program akan terus menjalankan instruksi di bawahnya.

Contoh:

Tunggu: DJNZ R7,Tunggu

RET

Selalu melakukan lompatan ke alamat tunggu dan mengurangi R7 dengan 1 selama nilai R7 belum mencapai 00

6. NOP

NOP

Instruksi ini berfungsi untuk melakukan tundaan pada program sebesar 1 cycle tanpa mempengaruhi register-register maupun flag.