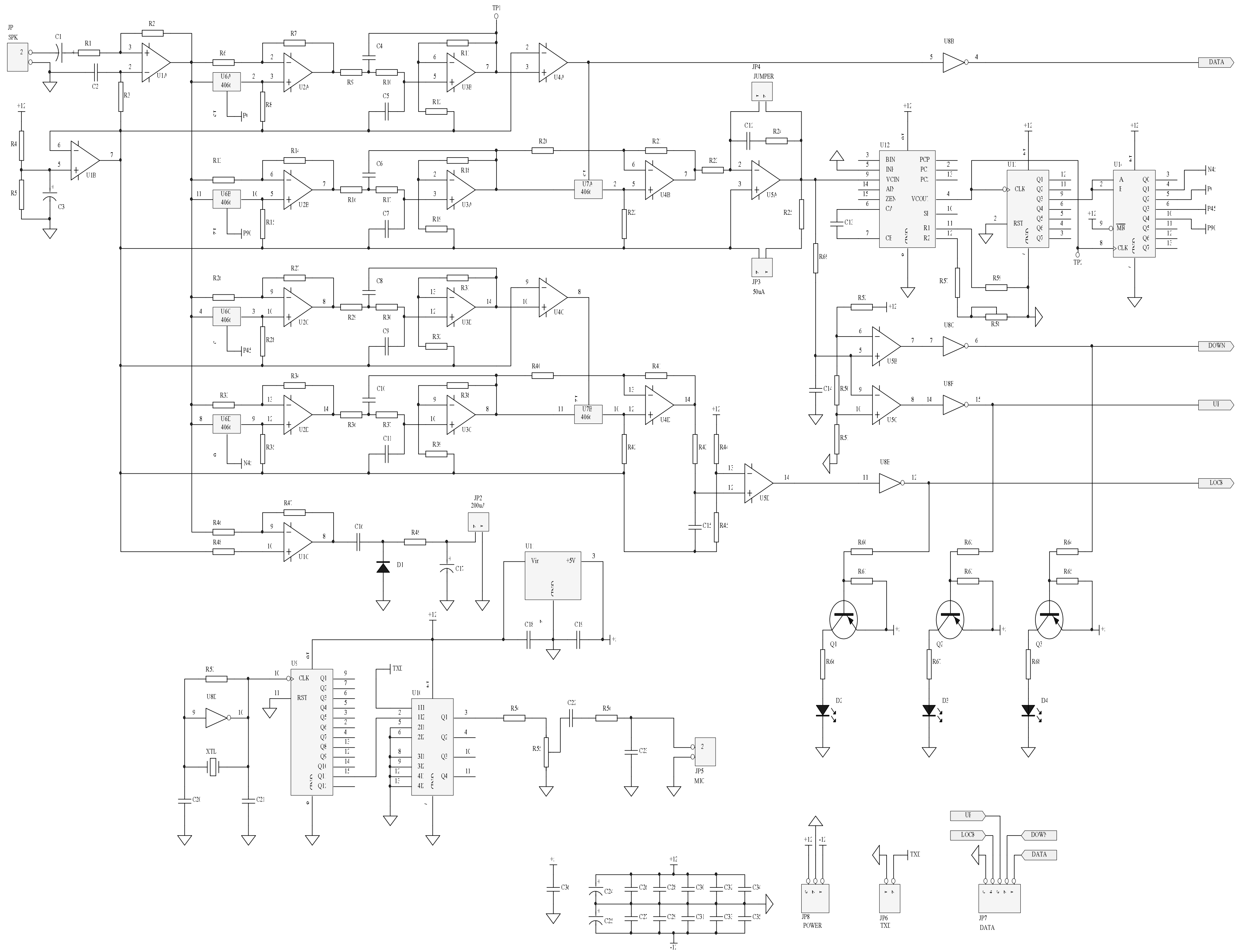
Lampiran A

Rangkaian Modem PSK 1200 Bps



JP
SPK
TP1
DATA
JP4
JUMPER
JP3
50uA
DOWN
LOCK
JP2
200uA
XTL
JP5
MIC
JP8
POWER
JP7
DATA

Lampiran B

IC – IC Yang Digunakan

Lampiran C

Tabel Parameter Design Filter Sallen and Key

HARRIS SEMICONDUCTOR

CA124, CA224, CA324, LM324, LM2902

Quad, 1MHz, Operational Amplifiers for Commercial, Industrial, and Military Applications

November 1996

Features

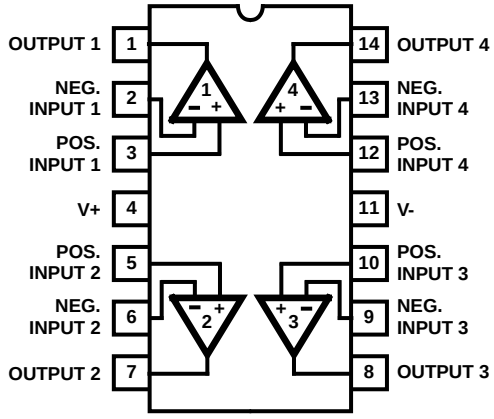
- **Operation from Single or Dual Supplies**
- **Unity-Gain Bandwidth . . . . . 1MHz (Typ)**
- **DC Voltage Gain . . . . . 100dB (Typ)**
- **Input Bias Current . . . . . 45nA (Typ)**
- **Input Offset Voltage . . . . . 2mV (Typ)**
- **Input Offset Current**
  - **CA224, CA324, LM324, LM2902 . . . . . 5nA (Typ)**
  - **CA124 . . . . . 3nA (Typ)**
- **Replacement for Industry Types 124, 224, 324**

Applications

- **Summing Amplifiers**
- **Multivibrators**
- **Oscillators**
- **Transducer Amplifiers**
- **DC Gain Blocks**

Pinout

CA124, CA224, CA324, LM2902 (PDIP, SOIC)
LM324 (PDIP)
TOP VIEW



Description

The CA124, CA224, CA324, LM324, and LM2902 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specially to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range from 0V to V+ -1.5V (single-supply operation) make these devices suitable for battery operation.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CA0124E	-55 to 125	14 Ld PDIP	E14.3
CA0124M (124)	-55 to 125	14 Ld SOIC	M14.15
CA0124M96 (124)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15
CA0224E	-40 to 85	14 Ld PDIP	E14.3
CA0224M (224)	-40 to 85	14 Ld SOIC	M14.15
CA0224M96 (224)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15
CA0324E	0 to 70	14 Ld PDIP	E14.3
CA0324M (324)	0 to 70	14 Ld SOIC	M14.15
CA0324M96 (324)	0 to 70	14 Ld SOIC Tape and Reel	M14.15
LM324N	0 to 70	14 Ld PDIP	E14.3
LM2902N	-40 to 85	14 Ld PDIP	E14.3
LM2902M (2902)	-40 to 85	14 Ld SOIC	M14.15
LM2902M96 (2902)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **796.3**

Absolute Maximum Ratings

Supply Voltage . . . . . 32V or ±16V
Differential Input Voltage. 32V
Input Voltage. . . . . -0.3V to 32V
Input Current (V_I < -0.3V, Note 1) 50mA
Output Short Circuit Duration (V+ ≤ 15V, Note 2). . . . . Continuous

Operating Conditions

Temperature Range
CA124. . . . . -55°C to 125°C
CA224, LM2902 . . . . . -40°C to 85°C
CA324, LM324 . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	100
SOIC Package	175

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

NOTES:

1. This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
2. The maximum output current is approximately 40mA independent of the magnitude of V+. Continuous short circuits at V+ > 15V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V+ can cause overheating and eventual destruction of the device.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	CA124			CA224, CA324, LM324			LM2902			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 6)		25	-	2	5	-	2	7	-	-	-	mV
		Full	-	-	7	-	-	9	-	-	10	mV
Average Input Offset Voltage Drift	R_S = 0Ω	Full	-	7	-	-	7	-	-	7	-	µV/°C
Differential Input Voltage (Note 5)		Full	-	-	V+	-	-	V+	-	-	V+	V
Input Common Mode Voltage Range (Note 5)	V+ = 30V	25	0	-	V+ -1.5	0	-	V+ -1.5	-	-	-	V
	V+ = 30V	Full	0	-	V+ -2	0	-	V+ -2	-	-	-	V
	V+ = 26V	Full	-	-	-	-	-	-	0	-	V+ -2	V
Common Mode Rejection Ratio	DC	25	70	85	-	65	70	-	-	-	-	dB
Power Supply Rejection Ratio	DC	25	65	100	-	65	100	-	-	-	-	dB
Input Bias Current (Note 4)	I_I+ or I_I-	25	-	45	150	-	45	250	-	-	-	nA
	I_I+ or I_I-	Full	-	-	300	-	-	500	-	40	500	nA
Input Offset Current	I_I+ - I_I-	25	-	3	30	-	5	50	-	-	-	nA
	I_I+ - I_I-	Full	-	-	100	-	-	150	-	45	200	nA
Average Input Offset Current Drift		Full	-	10	-	-	10	-	-	10	-	pA/°C

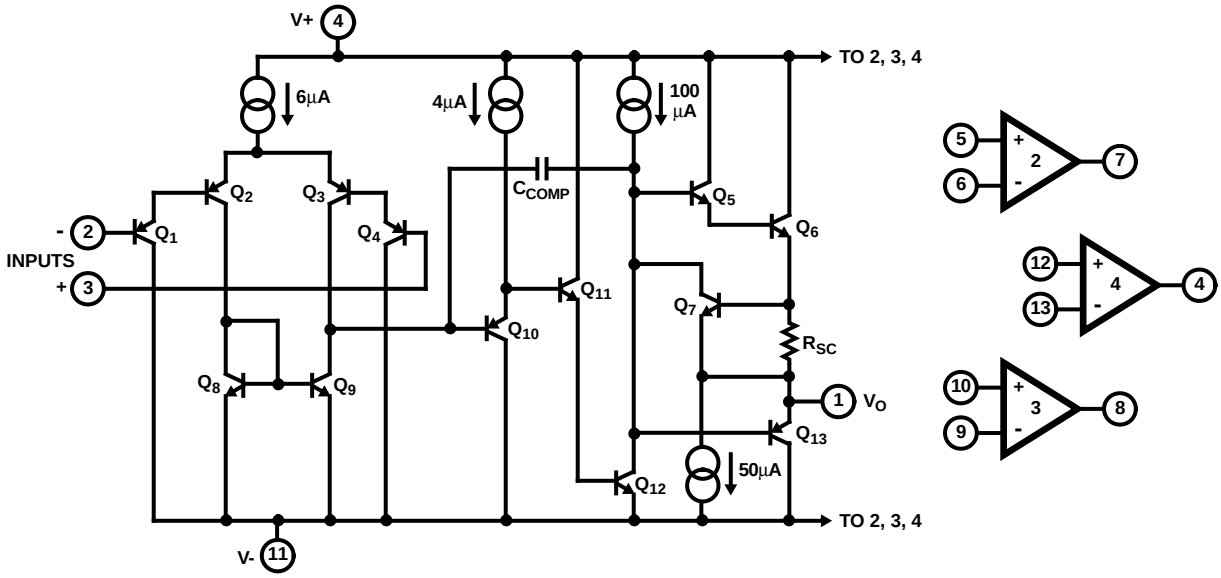
Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage V+ = 5V, V- = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEST CONDITIONS	TEMP. (^{O}C)	CA124			CA224, CA324, LM324			LM2902			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V+ = 15V (For Large V_O Swing)	25	94	100	-	88	100	-	-	-	-	dB
		$R_L \geq 2k\Omega$, V+ = 15V (For Large V_O Swing)	Full	88	-	-	83	-	-	83	-	-	dB
Output Voltage Swing		$R_L = 2k\Omega$	25	0	-	V+ -1.5	0	-	V+ -1.5	-	-	-	V
	High Level	$R_L = 2k\Omega$, V+ = 30V	Full	26	-	-	26	-	-	-	-	-	V
		$R_L = 2k\Omega$, V+ = 26V	Full	-	-	-	-	-	-	22	-	-	V
		$R_L = 10k\Omega$, V+ = 30V	Full	27	28	-	27	28	-	23	28	-	V
	Low Level	$R_L = 10k\Omega$	Full	-	5	20	-	5	20	-	5	100	mV
Output Current	Source	$V_I+ = +1V$, $V_I- = 0V$, V+ = 15V	25	20	40	-	20	40	-	-	-	-	mA
		$V_I+ = 1V$, $V_I- = 0$, V+ = 15V	Full	10	20	-	10	20	-	10	20	-	mA
	Sink	$V_I+ = 0V$, $V_I- = 1V$, V+ = 15V	25	10	20	-	10	20	-	-	-	-	mA
		$V_I+ = 0V$, $V_I- = 1V$, V_O = 200mV	25	12	50	-	12	50	-	-	-	-	µA
		$V_I- = 1V$, $V_I+ = 0$, V+ = 15V	Full	5	8	-	5	8	-	5	8	-	mA
Crosstalk		f = 1 to 20kHz (Input Referred)	25	-	-120	-	-	-120	-	-	-	-	dB
Total Supply Current		$R_L = \infty$	Full	-	0.8	2	-	0.8	2	-	0.7	1.2	mA
		$R_L = \infty$, V+ = 26V	Full	-	-	-	-	-	-	-	1.5	3	mA

NOTES:

4. Due to the PNP input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
5. The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is V+ - 1.5V, but either or both inputs can go to +32V without damage.
6. V_O = 1.4V, $R_S = 0\Omega$ with V+ from 5V to 30V, and over the full input common mode voltage range (0V to V+ - 1.5V).

Schematic Diagram (One of Four Operational Amplifiers)



Typical Performance Curves

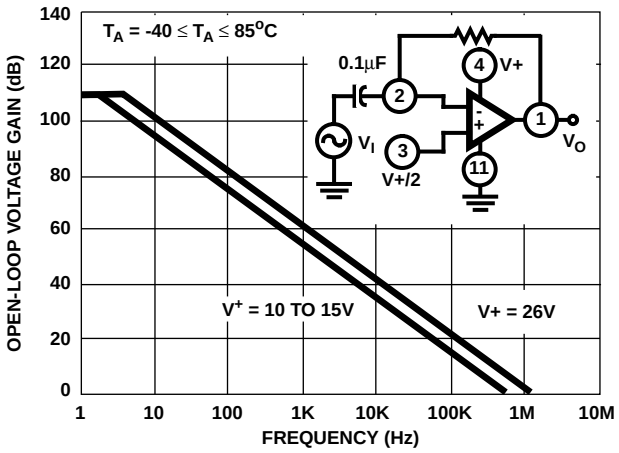


FIGURE 1. OPEN LOOP FREQUENCY RESPONSE

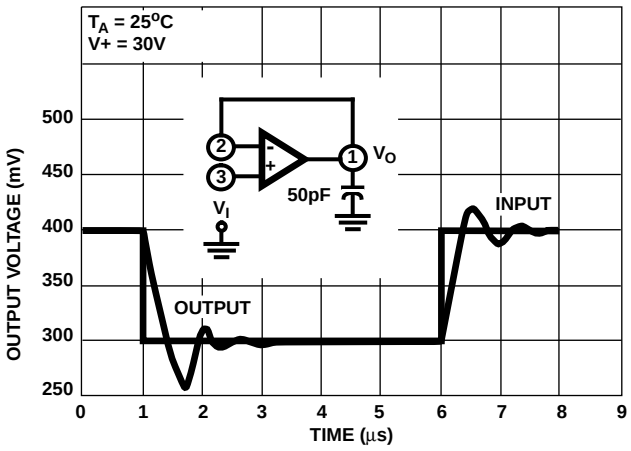


FIGURE 2. VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

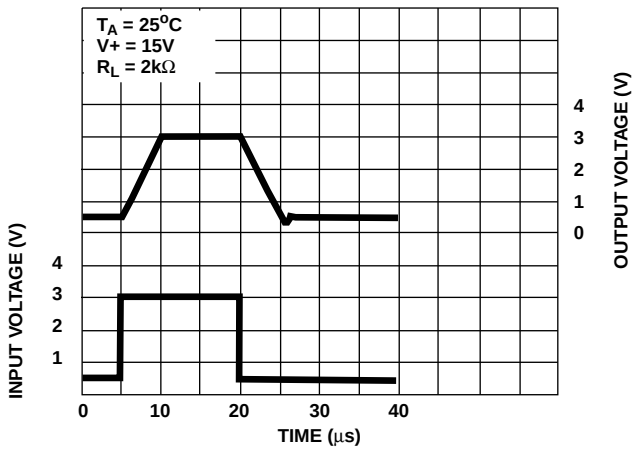


FIGURE 3. VOLTAGE FOLLOWER PULSE RESPONSE (LARGE SIGNAL)

Typical Performance Curves (Continued)

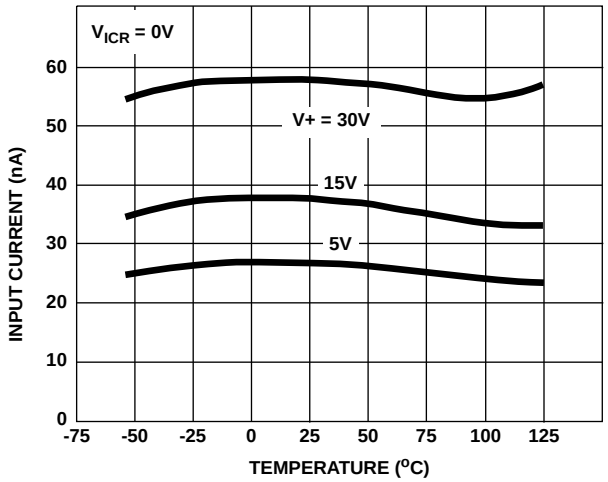


FIGURE 4. INPUT CURRENT vs AMBIENT TEMPERATURE

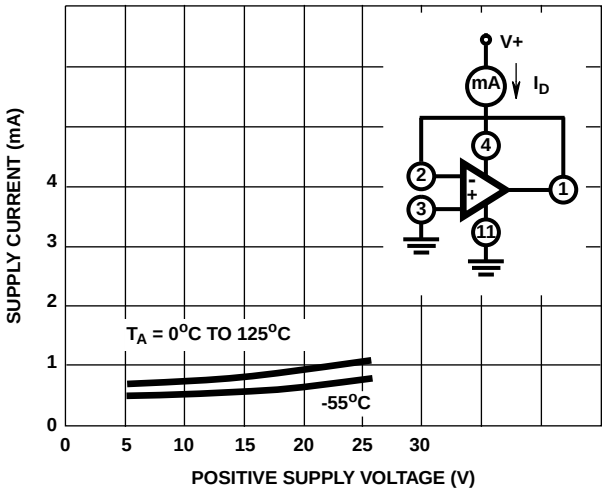


FIGURE 5. SUPPLY CURRENT vs SUPPLY VOLTAGE

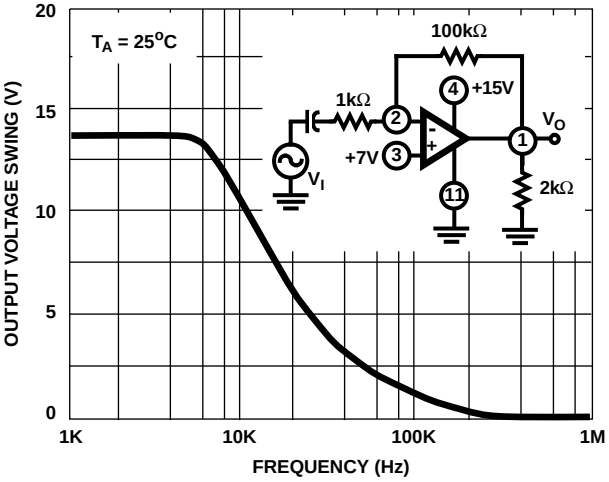


FIGURE 6. LARGE SIGNAL FREQUENCY RESPONSE

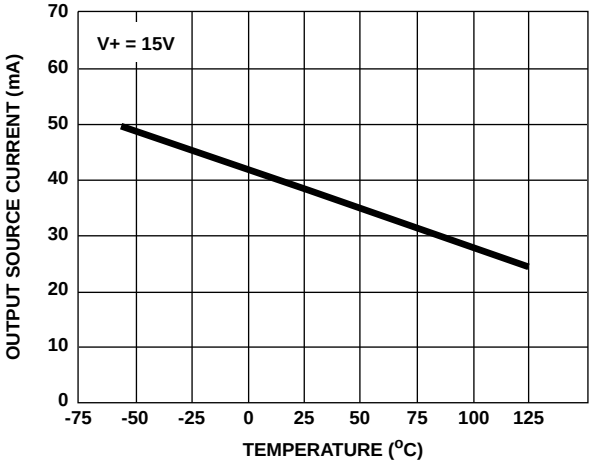


FIGURE 7. OUTPUT CURRENT vs AMBIENT TEMPERATURE

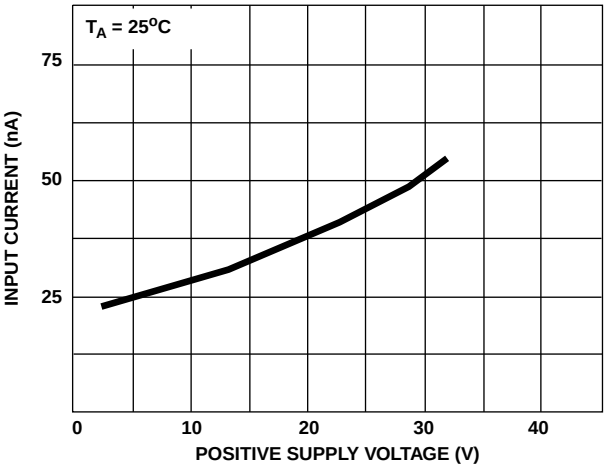


FIGURE 8. INPUT CURRENT vs SUPPLY VOLTAGE

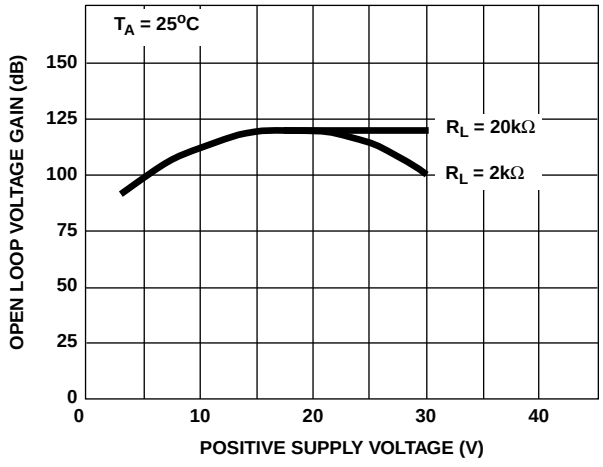


FIGURE 9. VOLTAGE GAIN vs SUPPLY VOLTAGE

CD4020B, CD4024B, CD4040B Types

CMOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4020B – 14 Stage
CD4024B – 7 Stage
CD4040B – 12 Stage

■ CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020B and CD4040B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

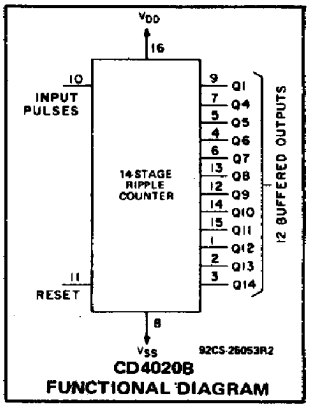
The CD4024B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

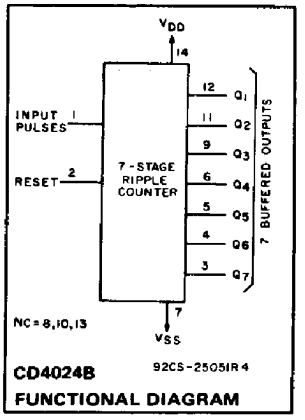
- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- Fully static operation
- Common reset
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

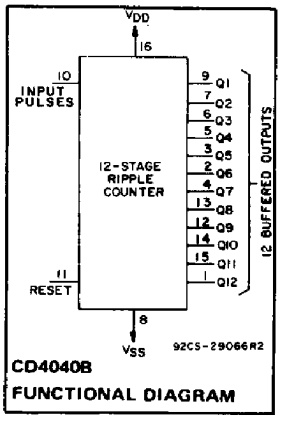
- Control counters
- Timers
- Frequency dividers
- Time-delay circuits



CD4020B
FUNCTIONAL DIAGRAM



CD4024B
FUNCTIONAL DIAGRAM



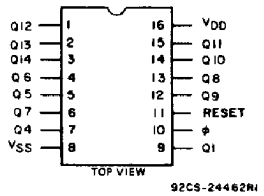
CD4040B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

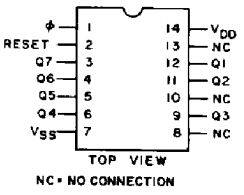
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

TERMINAL ASSIGNMENTS

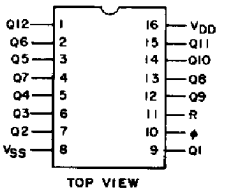
CD4020B



CD4024B



CD4040B



RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Input-Pulse Frequency,	f_ϕ	5 10 15	– – –	3.5 8 12	MHz
Input-Pulse Width,	t_W	5 10 15	140 60 40	– – –	ns
Input-Pulse Rise or Fall Time,	$t_{r\phi}$, $t_{f\phi}$	5 10 15	Unlimited		μs
Reset Pulse Width,	t_W	5 10 15	200 80 60	–	ns
Reset Removal Time,	t_{REM}	5 10 15	350 150 100	– – –	ns

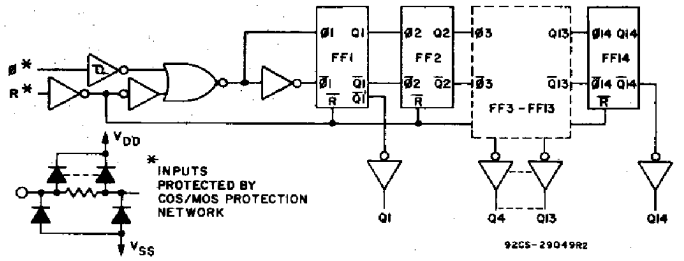


Fig. 1 – Logic diagram for CD4020B.

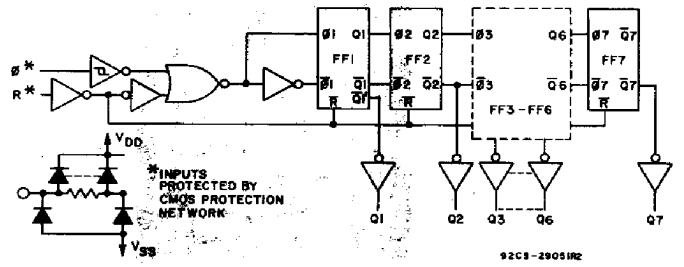


Fig. 2 – Logic diagram for CD4024B.

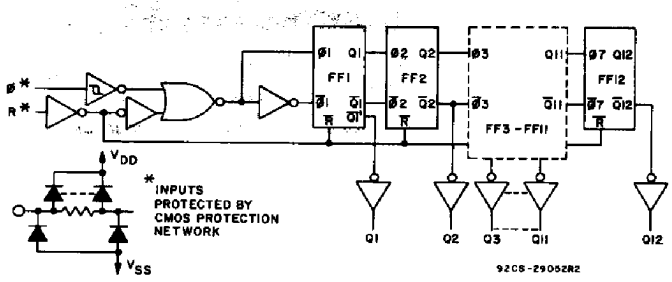


Fig. 3 – Logic diagram for CD4040B.

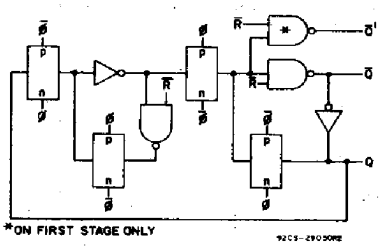


Fig. 4 – Detail of typical flip-flop stage.

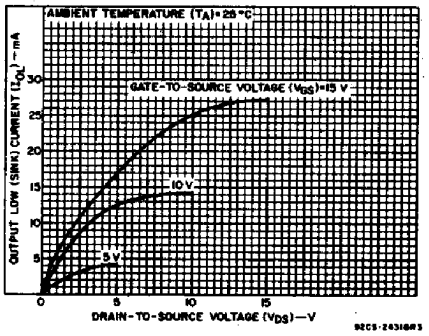


Fig. 5 – Typical output low (sink) current characteristics.

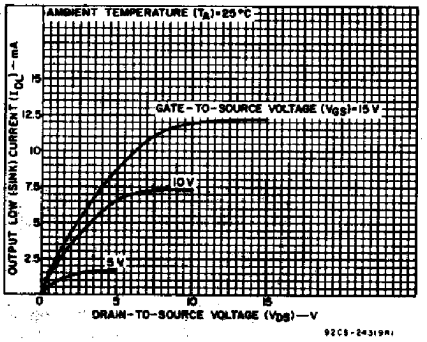


Fig. 6 – Minimum output low (sink) current characteristics.

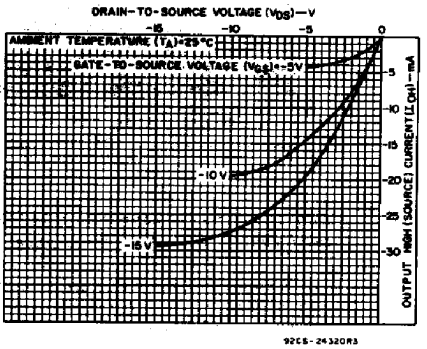


Fig. 7 – Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

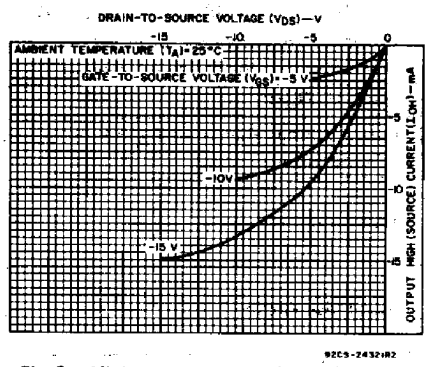


Fig. 8 – Minimum output high (source) current characteristics.

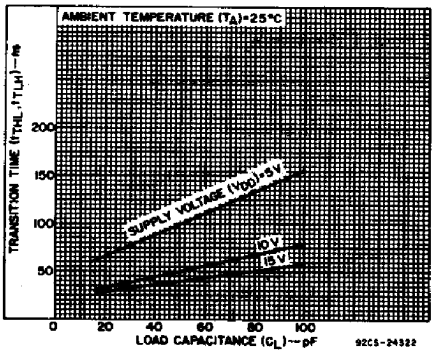
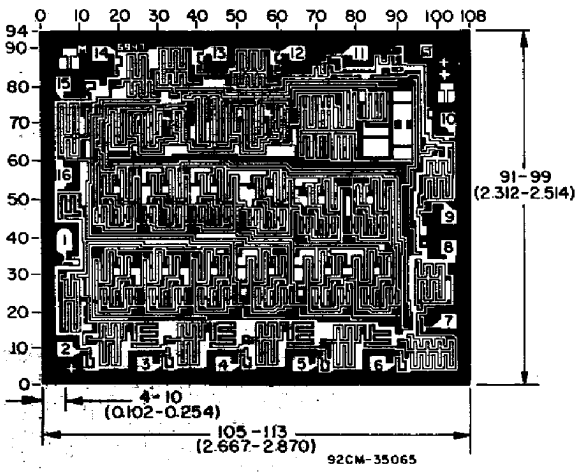
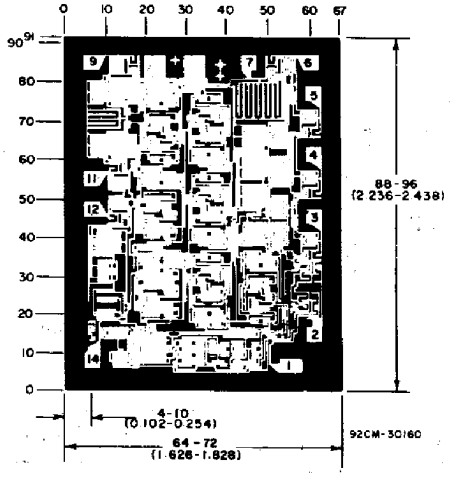


Fig. 9 – Typical transition time as a function of load capacitance.



Dimensions and Pad Layout for CD4020BH. Dimensions and pad layout for CD4040BH are identical.



Dimensions and Pad Layout for CD4024BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input-Pulse Operation						
Propagation Delay Time, ϕ to Q_1 Out; t_{PHL}, t_{PLH}		5	–	180	360	ns
		10	–	80	160	
		15	–	65	130	
Q_n to Q_n + 1; t_{PHL}, t_{PLH}		5	–	100	330	ns
		10	–	40	80	
		15	–	30	60	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Minimum Input-Pulse Width, t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Input-Pulse Rise or Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited			μs
		10				
		15				
Maximum Input-Pulse Frequency, f_ϕ		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Input Capacitance, C_I	Any Input		–	5	7.5	pF
Reset Operation						
Propagation Delay Time, t_{PHL}		5	–	140	280	ns
		10	–	60	120	
		15	–	50	100	
Minimum Reset Pulse Width, t_W		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Reset Removal Time, t_{REM}		5	–	175	350	ns
		10	–	75	150	
		15	–	50	100	

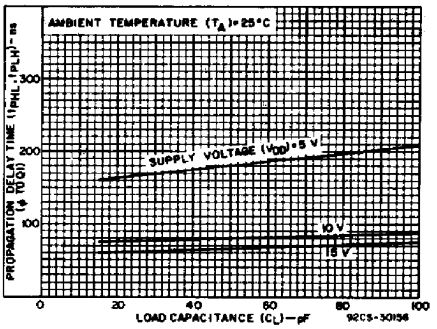


Fig. 10 – Typical propagation delay time as a function of load capacitance (ϕ to Q_1).

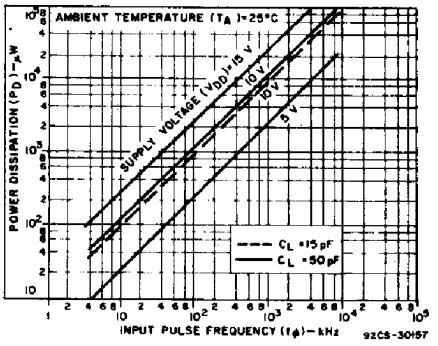


Fig. 11 – Typical dynamic power dissipation as a function of input pulse frequency for CD4020B.

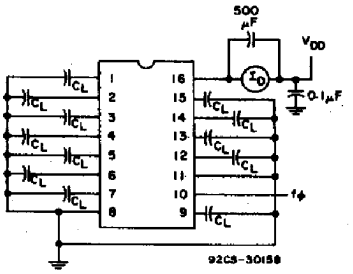


Fig. 12 – Dynamic power dissipation test circuit for CD4020B.

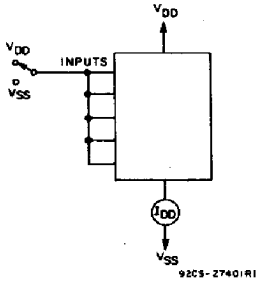


Fig. 13 – Quiescent device current test circuit.

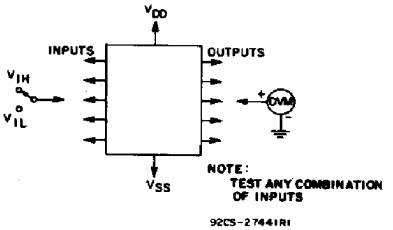


Fig. 14 – Input voltage test circuits.

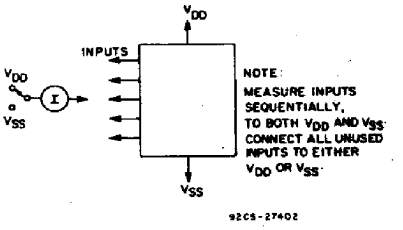


Fig. 15 – Input current test circuit.

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

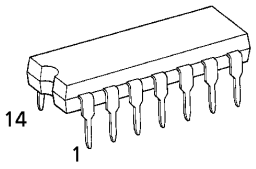
TC4030BP, TC4030BF, TC4030BFN

(Note) The JEDEC SOP (FN) is not available in Japan.

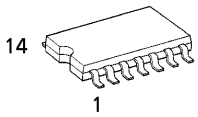
TC4030B QUAD EXCLUSIVE – OR GATE

TC4030B contains four circuits of exclusive OR gates. Since the buffers of two stage inverters are provided for all the outputs, the input / output voltage characteristic has been improved and the noise immunity has been also improved. And increase of transmission time due to load capacity increase is kept minimum.

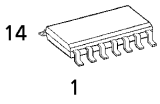
Wide variety of applicaitons are offerred, such as digital comparators and parity circuits.



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)

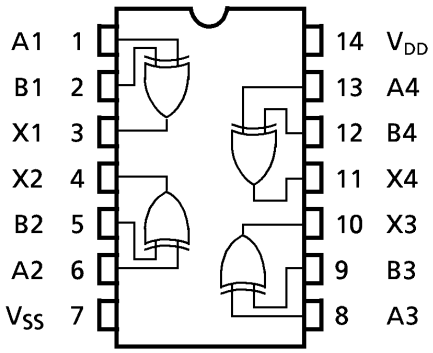


FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	T_{opr}	– 40~85	°C
Storage Temperature Range	T_{stg}	– 65~150	°C

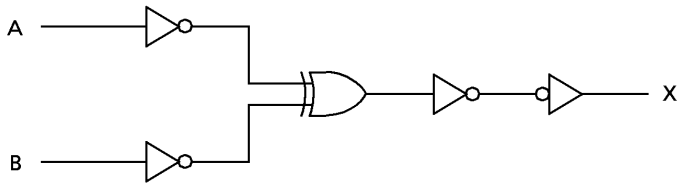
PIN ASSIGNMENT



(TOP VIEW)

CIRCUIT DIAGRAM

1/4 TC4030B



TRUTH TABLE

INPUTS		OUTPUT
A	B	X
L	L	L
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	—	18	V
Input Voltage	V_{IN}		0	—	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	−40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.00 10.00 15.00	— — —	4.95 9.95 14.95	— — —	V
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	— — —	0.05 0.05 0.05	— — —	0.00 0.00 0.00	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
Output High Current	I_{OH}	V_{OH} = 4.6V V_{OH} = 2.5V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN} = V_{SS}, V_{DD}$	5 5 10 15	−0.61 −2.50 −1.50 −4.00	— — — —	−0.51 −2.10 −1.30 −3.40	−1.0 −4.0 −2.2 −9.0	— — — —	−0.42 −1.70 −1.10 −2.80	— — — —	mA
Output Low Current	I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}, V_{DD}$	5 10 15	0.61 1.50 4.00	— — —	0.51 1.30 3.40	1.2 3.2 12.0	— — —	0.42 1.10 2.80	— — —	
Input High Voltage	V_{IH}	V_{OUT} = 0.5V, 4.5V V_{OUT} = 1.0V, 9.0V V_{OUT} = 1.5V, 13.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	3.5 7.0 11.0	— — —	3.5 7.0 11.0	2.75 5.50 8.25	— — —	3.5 7.0 11.0	— — —	V
Input Low Voltage	V_{IL}	V_{OUT} = 0.5V, 4.5V V_{OUT} = 1.0V, 9.0V V_{OUT} = 1.5V, 13.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	
Input Current "H" Level	I_{IH}	V_{IH} = 18V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL} = 0V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$*	5 10 15	— — —	1 2 4	— — —	0.001 0.001 0.002	1 2 4	— — —	7.5 15.0 30.0	

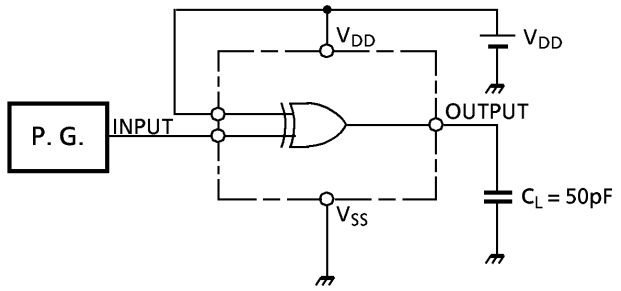
* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, C_L = 50pF)

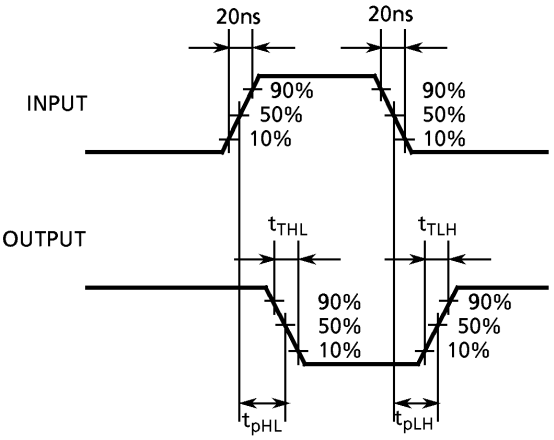
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time (High to Low)	t_{THL}		5	—	70	200	
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time	t_{pLH} t_{pHL}		5	—	90	280	ns
			10	—	45	130	
			15	—	35	100	
Input Capacitance	C_{IN}			—	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

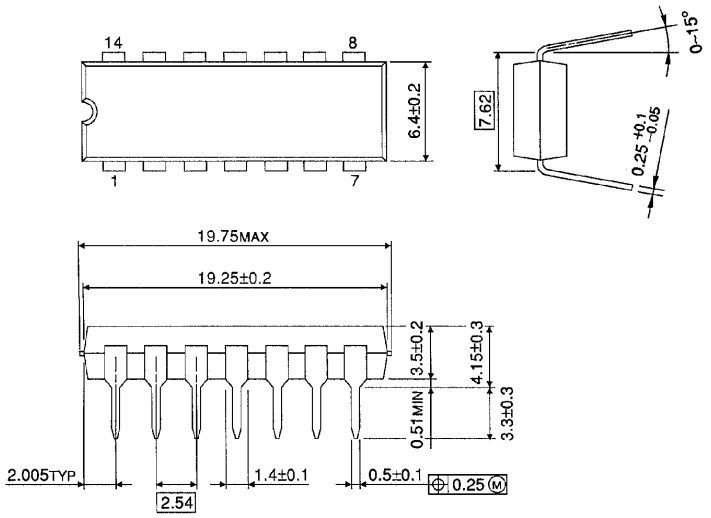
CIRCUIT



WAVEFORM

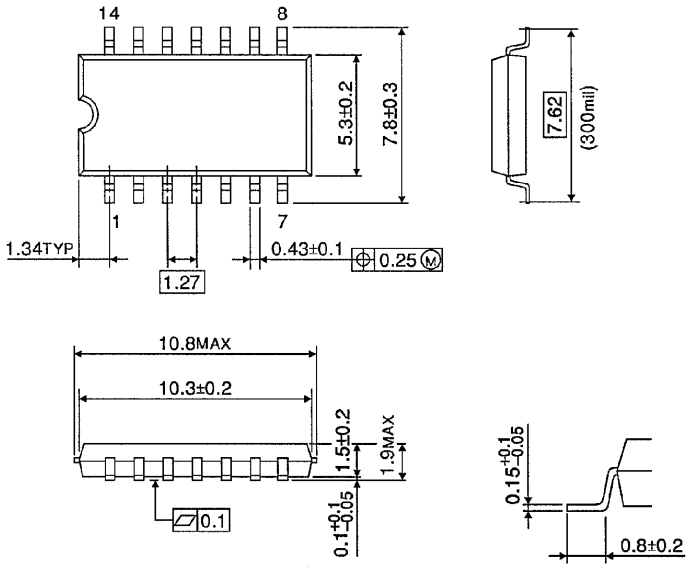


DIP 14PIN PACKAGE DIMENSIONS (DIP14-P-300-2.54) Unit in mm



Weight : 0.96g (Typ.)

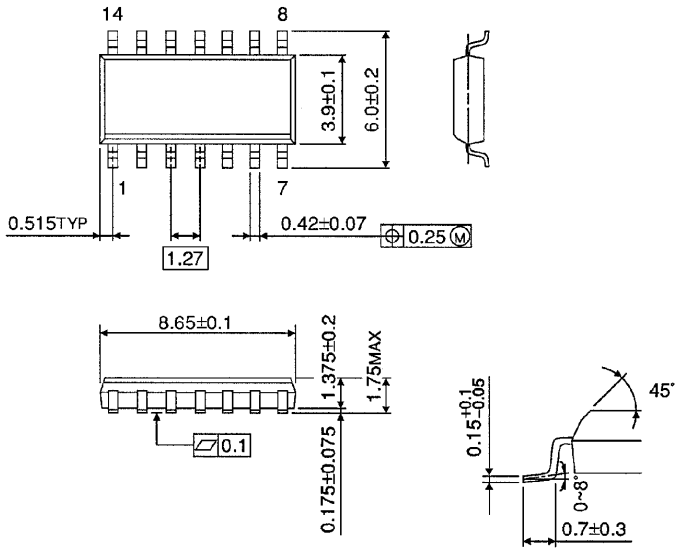
SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOL14-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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National Semiconductor

March 1988

CD4049UBM/CD4049UBC Hex Inverting Buffer
CD4050BM/CD4050BC Hex Non-Inverting Buffer

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

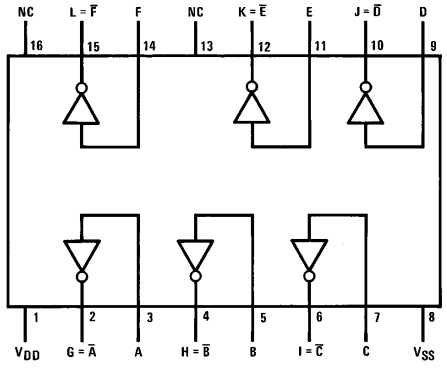
- Wide supply voltage range 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic level converter

Connection Diagrams

CD4049UBM/CD4049UBC
Dual-In-Line Package

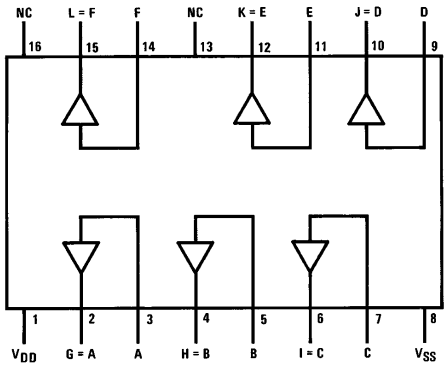


TL/F/5971–1

Top View

Order Number CD4049UB or CD4049B

CD4050BM/CD4050BC
Dual-In-Line Package



TL/F/5971–2

Top View

Order Number CD4050UB or CD4050B

CD4049UBM/CD4049UBC Hex Inverting Buffer
CD4050BM/CD4050BC Hex Non-Inverting Buffer

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to +18V
Voltage at Any Output Pin (V_{OUT})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to 15V
Voltage at Any Output Pin (V_{OUT})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4049UBM, CD4050BM	−55°C to +125°C
CD4049UBC, CD4050BC	−40°C to +85°C

DC Electrical Characteristics CD4049M/CD4050BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		30	μA
		V_{DD} = 10V		2.0		0.01	2.0		60	μA
		V_{DD} = 15V		4.0		0.03	4.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049UBM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049UBM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	5.6		4.6	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	12		9.8	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	35		29	40		20		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4049M/CD4050BM (Note 2) (Continued)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−1.3		−1.1	−1.6		−0.72		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−2.6		−2.2	−3.6		−1.5		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−8.0		−7.2	−12		−5.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4049UBC/CD4050BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		4		0.03	4.0		30	μA
		$V_{DD} = 10V$		8		0.05	8.0		60	μA
		$V_{DD} = 15V$		16		0.07	16.0		120	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0V$, $\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0V$, $\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BC Only)	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049UBC Only)	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 4.5V$		1.0		1.5	1.0		1.0	V
		$V_{DD} = 10V$, $V_O = 9V$		2.0		2.5	2.0		2.0	V
		$V_{DD} = 15V$, $V_O = 13.5V$		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BC Only)	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049UBC Only)	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$	4.0		4.0	3.5		4.0		V
		$V_{DD} = 10V$, $V_O = 1V$	8.0		8.0	7.5		8.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$	12.0		12.0	11.5		12.0		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4049UBC/CD4050BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	4.6		4.0	5		3.2		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	9.8		8.5	12		6.8		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	29		25	40		20		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−1.0		−0.9	−1.6		−0.72		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−2.1		−1.9	−3.6		−1.5		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−7.1		−6.2	−12		−5		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	−0.3		−0.3	-10^{-5}			−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$	0.3		0.3	10^{-5}			1.0	μA

AC Electrical Characteristics* CD4049UBM/CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		30	65	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		45	85	ns
		$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4050BM/CD4050BC

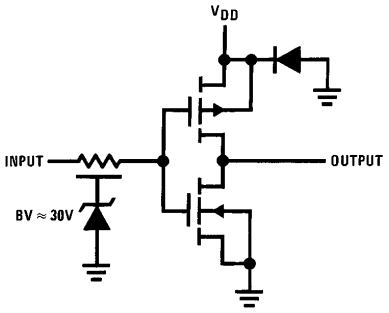
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		60	110	ns
		$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Schematic Diagrams

CD4049UBM/CD4049UBC
1 of 6 Identical Units



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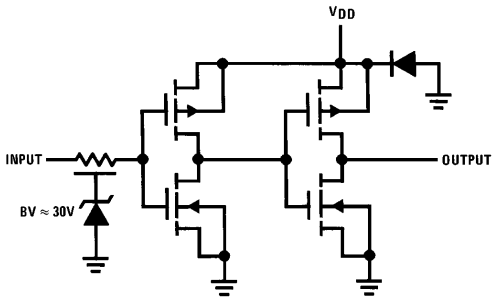
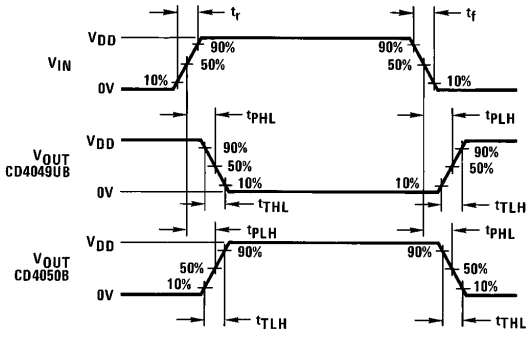
CD4050BM/CD4050BC
1 of 6 Identical Units



TL/F/5971–4

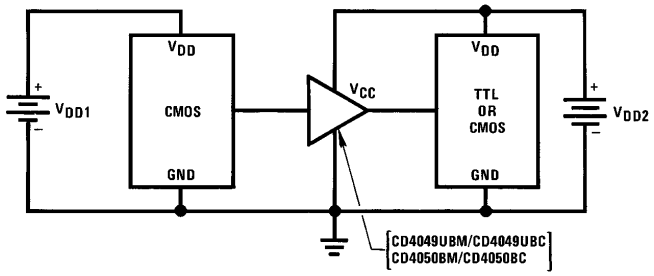
Switching Time Waveforms



TL/F/5971–5

Typical Applications

CMOS to TTL or CMOS at a Lower V_{DD}

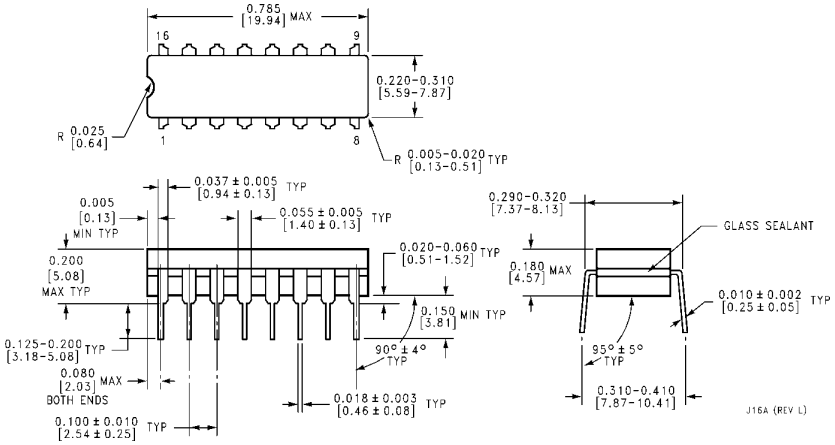


TL/F/5971–6

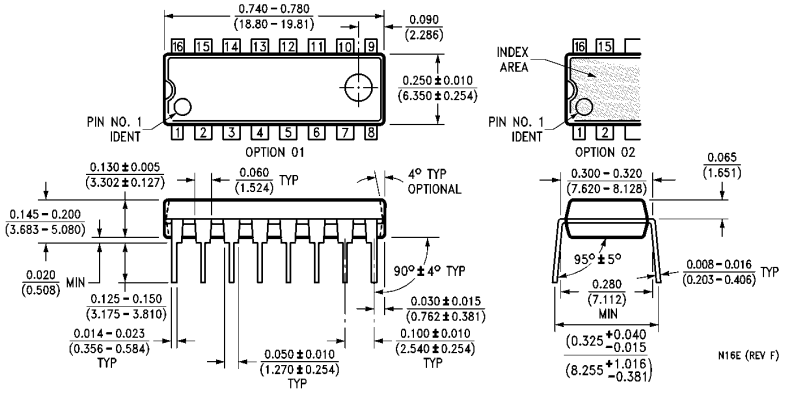
Note: $V_{DD1} \geq V_{DD2}$

Note: In the case of the CD4049UBM/CD4049UBC the output drive capability increases with increasing input voltage. E.g., If $V_{DD1} = 10V$ the CD4049UBM/CD4049UBC could drive 4 TTL loads.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4049UBMJ, CD4049UBCJ, CD4049BMJ or CD4049BCJ
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number CD4050BMN, CD4050BCN, CD4050BMN or CD4050BCN
NS Package Number N16E

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FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4046BC
Micropower Phase-Locked Loop

General Description

The CD4046BC micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

Features

- Wide supply voltage range: 3.0V to 18V
- Low dynamic power consumption: 70 μW (typ.) at f_o = 10 kHz, V_{DD} = 5V
- VCO frequency: 1.3 MHz (typ.) at V_{DD} = 10V
- Low frequency drift: 0.06%/°C at V_{DD} = 10V with temperature
- High VCO linearity: 1% (typ.)

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

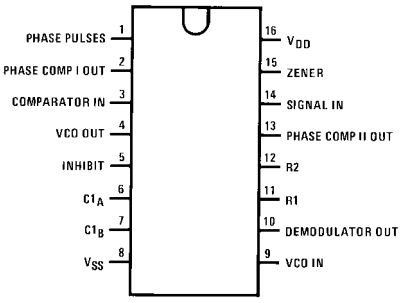
Ordering Code:

Order Number	Package Number	Package Description
CD4046BCM	M16A	16-Lead Small Outline integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4046BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for SOIC and DIP



Top View

Block Diagram

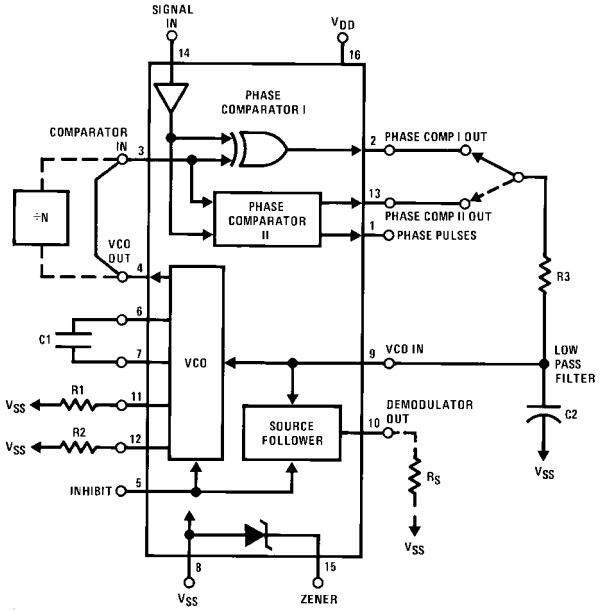


FIGURE 1.

Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	Pin 5 = V_{DD}, Pin 14 = V_{DD},								
		Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		20		0.005	20		150	µA
		V_{DD} = 10V		40		0.01	40		300	µA
		V_{DD} = 15V		80		0.015	80		600	µA
		Pin 5 = V_{DD}, Pin 14 = Open,								
		Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		70		5	55		205	µA
		V_{DD} = 10V		530		20	410		710	µA
		V_{DD} = 15V		1500		50	1200		1800	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	Comparator and Signal In	V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	Comparator and Signal In	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	LOW Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	(Note 4)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	(Note 4)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA
C_{IN}	Input Capacitance	Any Input (Note 3)					7.5			pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ,								
		R2 = ∞, $\varsigma XO_{IN} = \varsigma_{\Delta\Delta}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5)

$T_A = 25°C$, $C_L = 50$ pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCO SECTION						
I_{DD}	Operating Current	f_o = 10 kHz, R1 = 1 MΩ,				
		R2 = ∞, $\varsigma XO_{IN} = \varsigma_{\Delta\Delta}/2$				
		V_{DD} = 5V		20		µA
		V_{DD} = 10V		90		µA
		V_{DD} = 15V		200		µA
f_{MAX}	Maximum Operating Frequency	C1 = 50 pF, R1 = 10 kΩ,				
		R2 = ∞, $\varsigma XO_{IN} = \varsigma_{\Delta\Delta}$				
		V_{DD} = 5V	0.4	0.8		MHz
		V_{DD} = 10V	0.6	1.2		MHz
		V_{DD} = 15V	1.0	1.6		MHz
	Linearity	VCO_{IN} = 2.5V ±0.3V,				
		R1 ≥ 10 kΩ, V_{DD} = 5V		1		%
		VCO_{IN} = 5V ±2.5V,				
		R1 ≥ 400 kΩ, V_{DD} = 10V		1		%
		VCO_{IN} = 7.5V ±5V,				
		R1 ≥ 1 MΩ, V_{DD} = 15V		1		%
	Temperature-Frequency Stability	%/°C∝1/ϕ. $\varsigma_{\Delta\Delta}$				
	No Frequency Offset, $f_{MIN} = 0$	R2 = ∞				
		V_{DD} = 5V		0.12–0.24		%/°C
		V_{DD} = 10V		0.04–0.08		%/°C
		V_{DD} = 15V		0.015–0.03		%/°C
	Frequency Offset, $f_{MIN} \neq 0$	V_{DD} = 5V		0.06–0.12		%/°C
		V_{DD} = 10V		0.05–0.1		%/°C
		V_{DD} = 15V		0.03–0.06		%/°C
VCO_{IN}	Input Resistance	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
VCO	Output Duty Cycle	V_{DD} = 5V		50		%
		V_{DD} = 10V		50		%
		V_{DD} = 15V		50		%
t_{THL}	VCO Output Transition Time	V_{DD} = 5V		90	200	ns
t_{THL}		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		45	80	ns
PHASE COMPARATORS SECTION						
R_{IN}	Input Resistance					
	Signal Input	V_{DD} = 5V	1	3		MΩ
		V_{DD} = 10V	0.2	0.7		MΩ
		V_{DD} = 15V	0.1	0.3		MΩ
	Comparator Input	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
	AC-Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000 pF				
		f = 50 kHz				
		V_{DD} = 5V		200	400	mV
		V_{DD} = 10V		400	800	mV
		V_{DD} = 15V		700	1400	mV

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DEMODULATOR OUTPUT						
$VCO_{IN}-V_{DEM}$	Offset Voltage	RS ≥ 10 kΩ, V_{DD} = 5V		1.50	2.2	V
		RS ≥ 10 kΩ, V_{DD} = 10V		1.50	2.2	V
		RS ≥ 50 kΩ, V_{DD} = 15V		1.50	2.2	V
	Linearity	RS ≥ 50 kΩ				
		VCO_{IN} = 2.5V ±0.3V, V_{DD} = 5V		0.1		%
		VCO_{IN} = 5V ±2.5V, V_{DD} = 10V		0.6		%
		VCO_{IN} = 7.5V ±5V, V_{DD} = 15V		0.8		%
ZENER DIODE						
V_Z	Zener Diode Voltage	I_Z = 50 µA	6.3	7.0	7.7	V
R_Z	Zener Dynamic Resistance	I_Z = 1 mA		100		Ω

Note 5: AC Parameters are guaranteed by DC correlated testing.

Phase Comparator State Diagrams

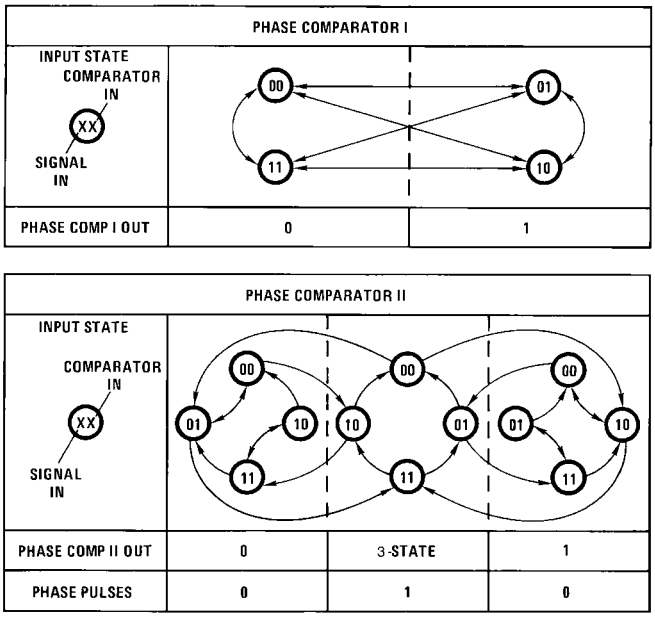


FIGURE 2.

Typical Waveforms

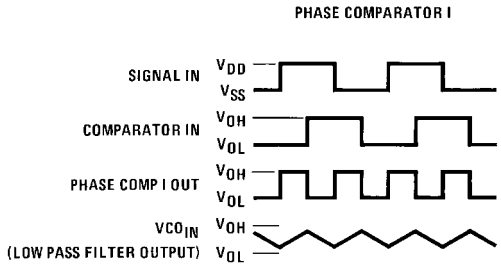


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

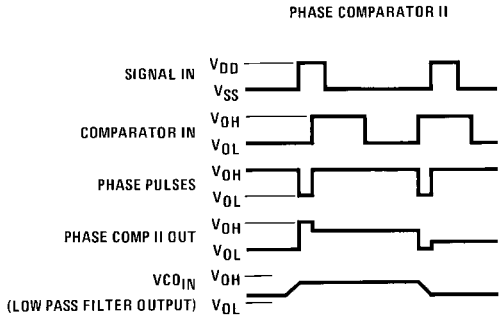


FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

Typical Center Frequency vs C1
for R1 = 10 kΩ, 100 kΩ and 1 MΩ

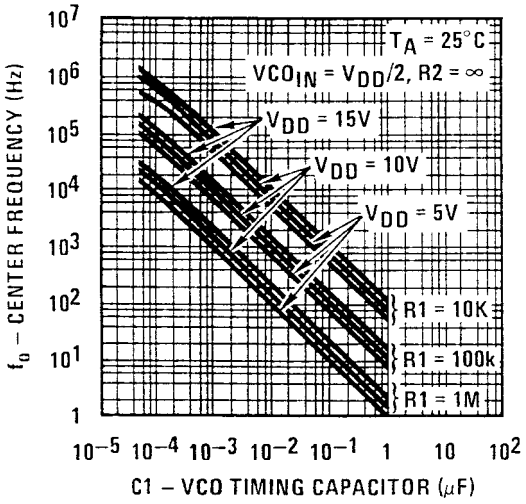


FIGURE 5.

Typical Frequency vs C1
for R2 = 10 kΩ, 100 kΩ and 1 MΩ

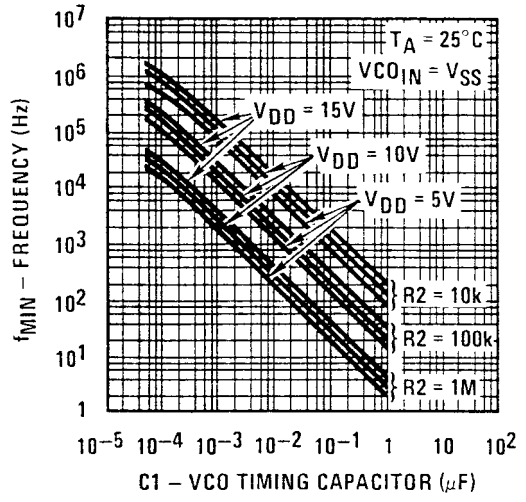


FIGURE 6.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_0) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Typical f_{MAX}/f_{MIN} vs R2/R1

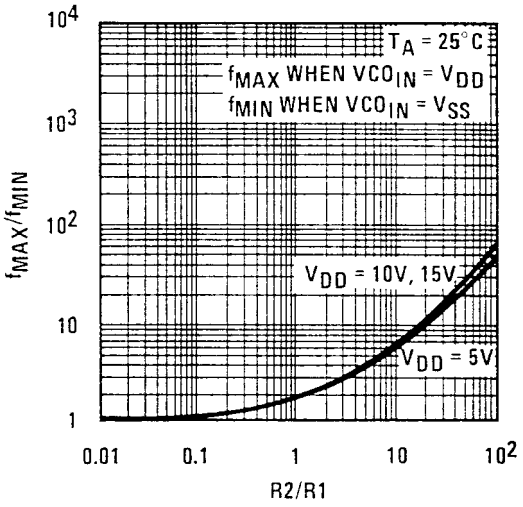


FIGURE 7.

Typical VCO Power Dissipation at Center Frequency vs R1

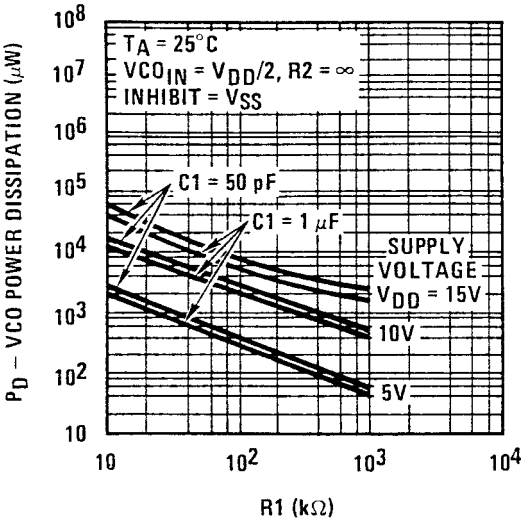


FIGURE 8.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Typical VCO Power Dissipation at f_{MIN} vs R2

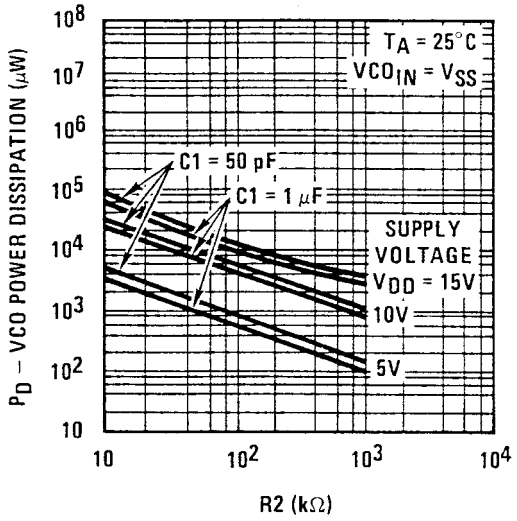


FIGURE 9.

Typical Source Follower Power Dissipation vs R_S

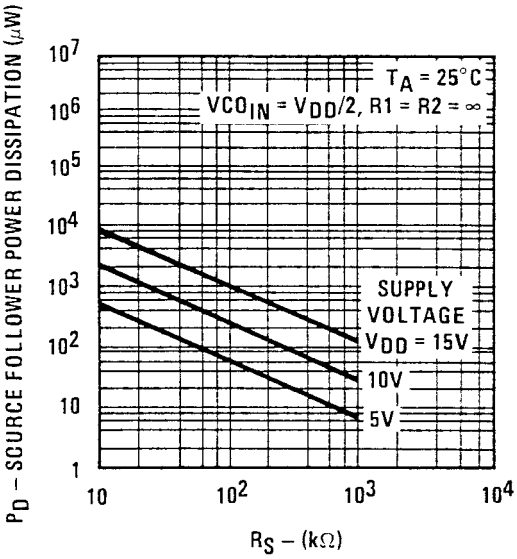


FIGURE 10.

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

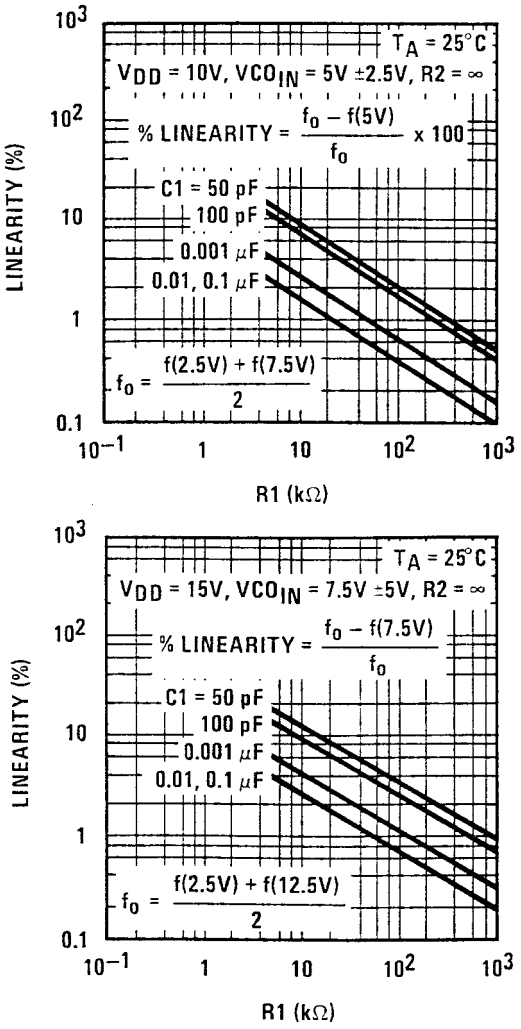


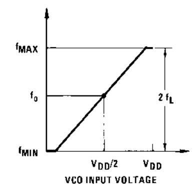
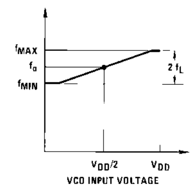
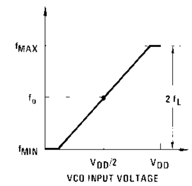
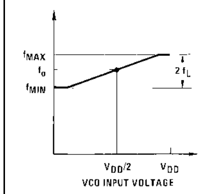
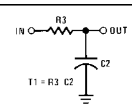
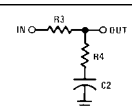
FIGURE 11. Typical VCO Linearity vs R1 and C1

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: R1, R2 ≥ 10 kΩ, R_S ≥ 10 kΩ, C1 ≥ 50 pF.

In addition to the given design information, refer to Figure 5, Figure 6, Figure 7 for R1, R2 and C1 component selections.

Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset R2 = ∞	**VCO With Offset**	**VCO Without Offset R2 = ∞**	**VCO With Offset**
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, 2 f_L	2 f_L = full VCO frequency range 2 $f_L = f_{max} - f_{min}$			
Frequency Capture Range, 2 f_C		$2 f_C \approx \frac{1}{\pi}\sqrt{\frac{2 \pi f_L}{\tau 1}}$	$f_C = f_L$	
Loop Filter Component Selection		For 2 f_C, see Ref.		
Phase Angle Between Single and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range (2 f_L)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

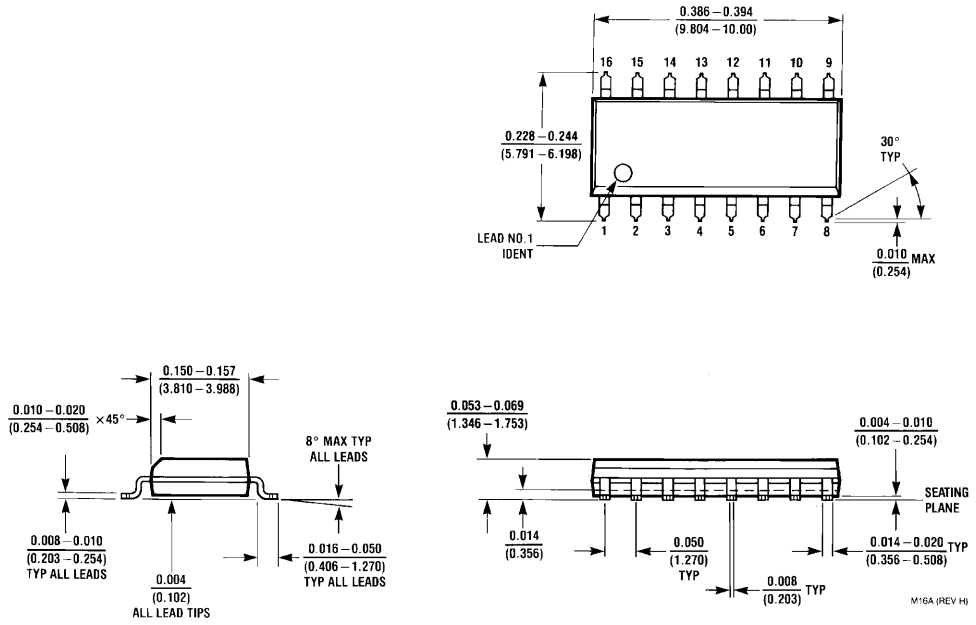
Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset **R2** = ∞	VCO With Offset	VCO Without Offset **R2** = ∞	VCO With Offset
VCO Component Selection	Given: f_o. Use f_o with Figure 5 to determine R1 and C1.	Given: f_o and f_L. Calculate f_{min} from the equation $f_{min} = f_o - f_L$. Use f_{min} with Figure 6 to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$. Use $\frac{f_{max}}{f_{min}}$ with Figure 7 to determine ratio R2/R1 to obtain R1.	Given: f_{max}. Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$. Use f_o with Figure 5 to determine R1 and C1.	Given: f_{min} and f_{max}. Use f_{min} with Figure 6 to to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ Use $\frac{f_{max}}{f_{min}}$ with Figure 7 to determine ratio R2/R1 to obtain R1.

References

G.S. Moschytz, “Miniaturized RC Filters Using Phase-Locked Loop”, BSTJ, May, 1965.

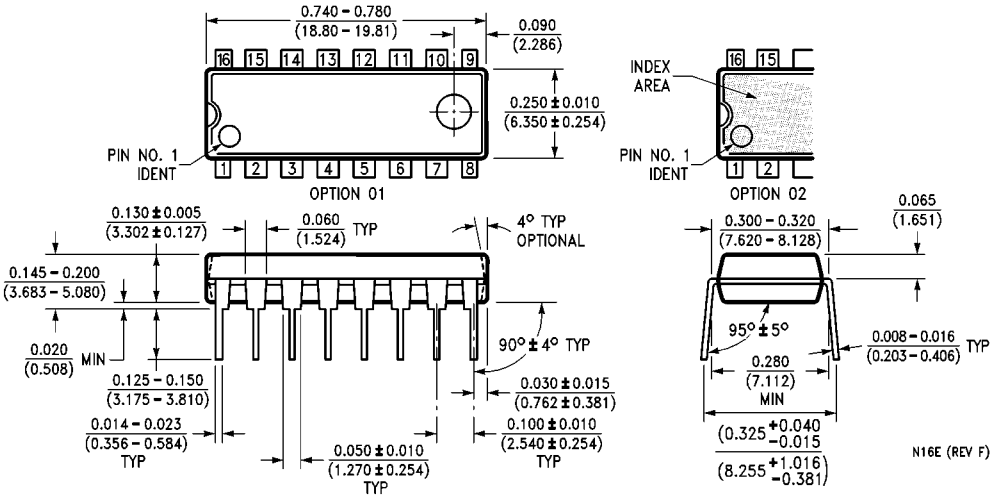
Floyd Gardner, “Phaselock Techniques”, John Wiley & Sons, 1966.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow Body
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

CD4024BC
7-Stage Ripple Carry Binary Counter

General Description

The CD4024BC is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical "0" stage by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- High speed: 12 MHz (typ.)
  input pulse rate $V_{DD} - V_{SS} = 10V$
- Fully static operation

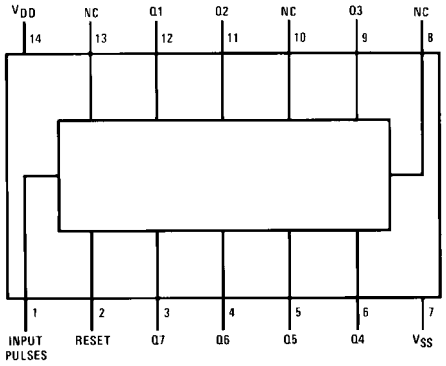
Ordering Code:

Order Number	Package Number	Package Description
CD4024BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
CD4024BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

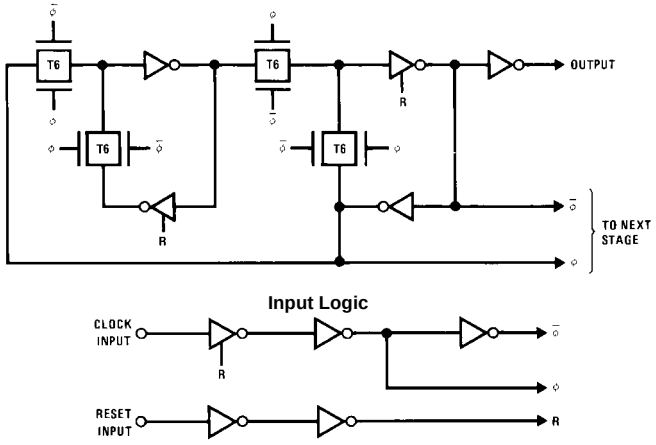
Connection Diagram

Pin Assignments for DIP and SOIC



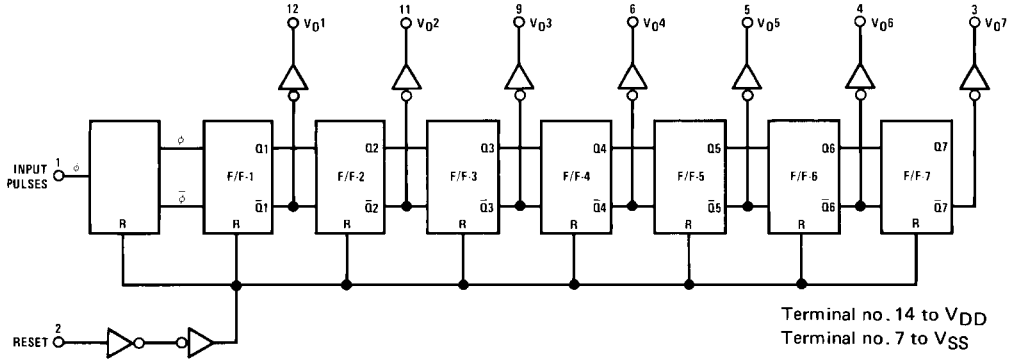
Top View

Logic Diagrams



Flip-flop logic (1 of 7 identical stages).

Block Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature	
(Soldering, 10 seconds) (T_L)	260°C

Recommended Operating Conditions (Note 1)

DC Supply Voltage (V_{DD})	+3 to +15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.3	20		150	µA
		V_{DD} = 10V		40		0.5	40		300	µA
		V_{DD} = 15V		60		0.7	80		600	µA
V_{OL}	LOW Level Output Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	$\|I_O\|$<1 µA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	LOW Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	µA

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

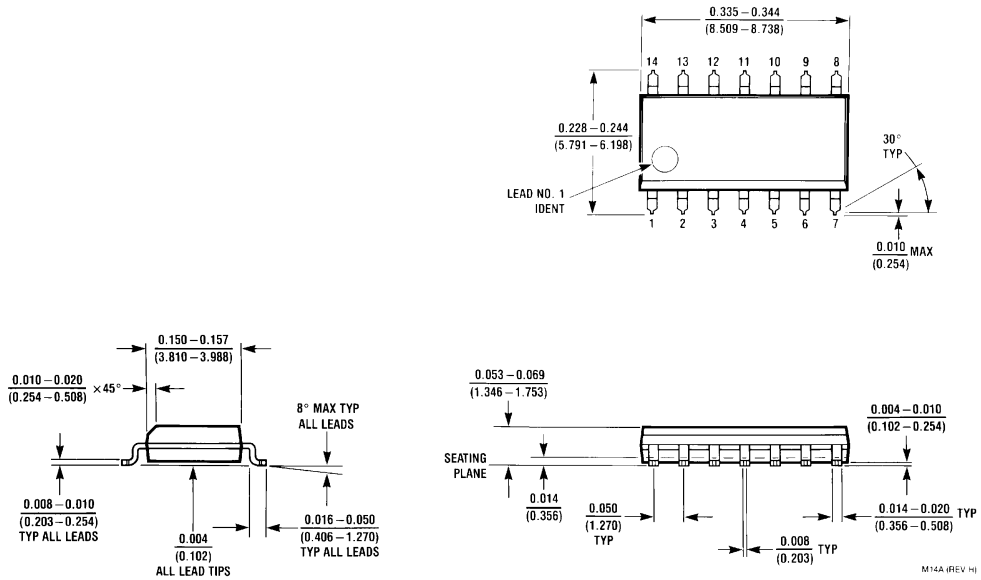
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, t_r and $t_f = 20$ ns unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		185	350	ns
	to Q1 Output	$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width	$V_{DD} = 5V$		75	200	ns
		$V_{DD} = 10V$		40	110	ns
		$V_{DD} = 15V$		35	90	ns
t_{RCL}, t_{FCL}	Input Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			10	μs
		$V_{DD} = 15V$			8	μs
f_{CL}	Maximum Input Pulse Frequency	$V_{DD} = 5V$	1.5	5		MHz
		$V_{DD} = 10V$	4	12		MHz
		$V_{DD} = 15V$	5	15		MHz
t_{PHL}	Reset Propagation Delay Time	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
t_{WH}	Reset Minimum Pulse Width	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
C_{IN}	Input Capacitance (Note 5)	Any Input		5	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

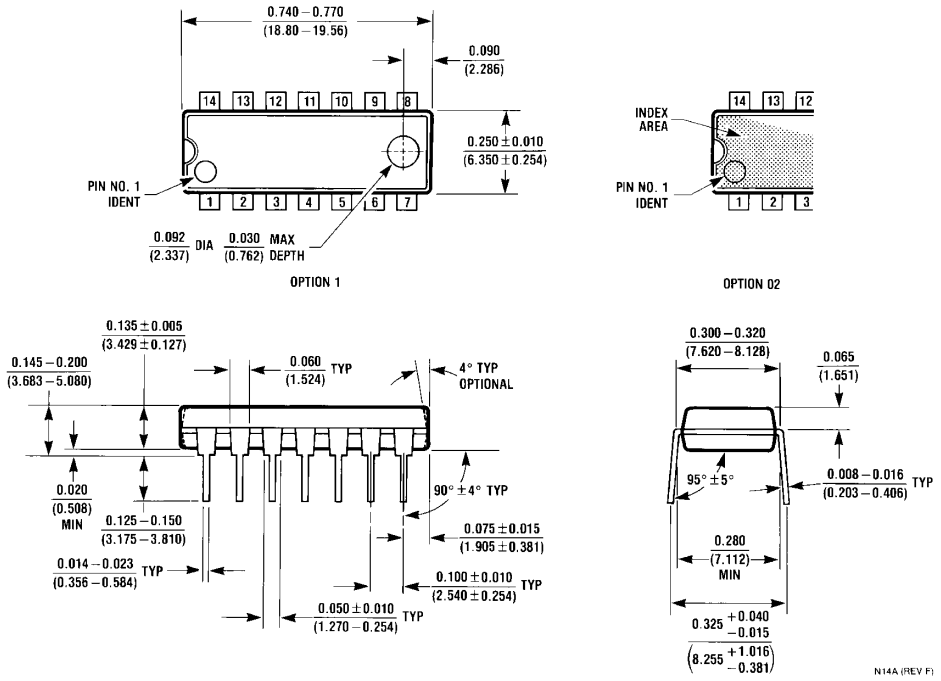
Note 5: Capacitance is guaranteed by periodic testing.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS051

CD4066B Types

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

■ CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

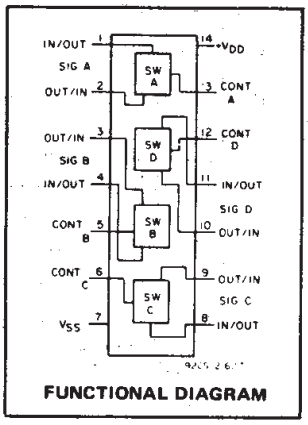
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig.1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), and in chip form (H suffix).

Features:

- 15-V digital or ±7.5-V peak-to-peak switching
- 125Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 5 Ω over 15-V signal-input range
- On-state resistance flat over full peak-to-peak signal range
- High on/off output-voltage ratio: 80 dB typ. @ f_{is} = 1 kHz, R_L = 1 kΩ
- High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: −50 dB typ. @ f_{is} = 8 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Analog signal switching/multiplexing
  Signal gating — Modulator
  Squelch control — Demodulator
  Chopper — Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

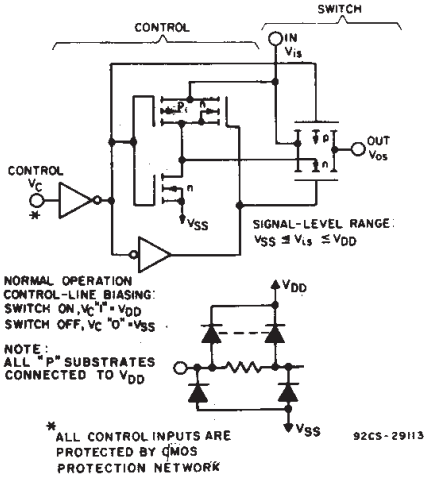


Fig. 1 — Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) −55	−40	+85	+125	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD}		0,5	5	0.25	0.25	7.5	7.5	0.01	0.25	μA
		0,10	10	0.5	0.5	15	15	0.01	0.5	
		0,15	15	1	1	30	30	0.01	1	
		0,20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Output (V_{os})										
On-State Resistance, r_{on} Max.	$V_C = V_{DD}$, R_L = 10 kΩ returned to $\frac{V_{DD}-V_{SS}}{2}$, $V_{is} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
			10	310	330	500	550	180	400	
			15	200	210	300	320	125	240	
ΔOn-State Resistance Between Any 2 Switches, Δr_{on}	R_L=10 kΩ, $V_C = V_{DD}$		5	–	–	–	–	15	–	Ω
			10	–	–	–	–	10	–	
			15	–	–	–	–	5	–	
Total Harmonic Distortion, THD	V_C=V_{DD} = 5 V, V_{SS} = −5 V, $V_{is(p-p)}$ = 5 V (Sine wave centered on 0 V) R_L=10 kΩ, f_{is}=1 kHz sine wave			–	–	–	–	0.4	–	%
−3dB Cutoff Frequency (Switch on)	V_C=V_{DD}=5 V, V_{SS} = −5 V, $V_{is(p-p)}$ =5 V (Sine wave centered on 0 V R_L = 1 kΩ,			–	–	–	–	40	–	MHz
−50dB Feed-through Frequency (Switch off)	V_C=V_{SS}= −5 V, $V_{is(p-p)}$ = 5 V Sine wave centerd on 0 V R_L = 1 kΩ			–	–	–	–	1	–	MHz
Input/Output Leakage Current (Switch off) I_{is} Max.	V_C = 0 V V_{is} = 18 V; V_{os} = 0 V, V_{is} = 0V; V_{os} = 18 V		18	±0.1	±0.1	±1	±1	$±10^{-5}$	±0.1	μA
−50 dB Crosstalk Frequency	V_C(A) = V_{DD} = +5 V, V_C(B) = V_{SS} = −5 V, V_{is}(A) = 5 V_{p-p}, 50 Ω source R_L = 1 kΩ			–	–	–	–	8	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	R_L = 200 kΩ V_C = V_{DD}, V_{SS} = GND, C_L = 50 pF V_{is} = 10 V (Square wave centered on 5 V t_r, t_f = 20 ns		5	–	–	–	–	20	40	ns
			10	–	–	–	–	10	20	
			15	–	–	–	–	7	15	
Capacitance: Input, C_{is}	V_{DD} = +5 V V_C = V_{SS} = −5 V			–	–	–	–	8	–	pF
Output, C_{os}				–	–	–	–	8	–	
Feedthrough, C_{ios}				–	–	–	–	0.5	–	

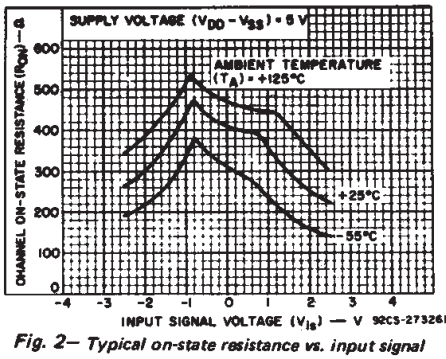


Fig. 2— Typical on-state resistance vs. input signal voltage (all types).

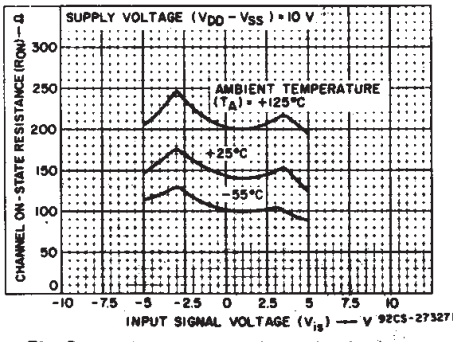


Fig. 3— Typical on-state vs. input signal voltage (all types).

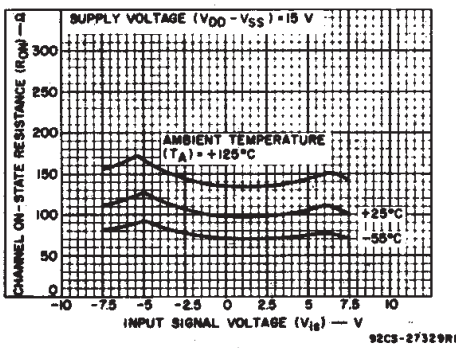


Fig. 4— Typical on-state resistance vs. input signal voltage (all types).

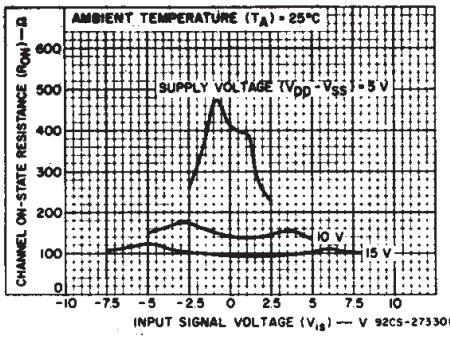


Fig. 5— on-state resistance vs. input signal voltage (all types).

3 COMMERCIAL CMOS HIGH VOLTAGE ICs

ELECTRICAL CHARACTERISTICS (cont'd)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) –55	–40	+85	+125	+25 Typ.	+25 Max.	UNITS
Control (V_C)									
Control Input Low Voltage, V_{ILC} Max.	$\lvert I_{is}\rvert < 10\,\mu A$ $V_{is} = V_{SS}, V_{OS} = V_{DD}$ and $V_{is} = V_{DD}, V_{OS} = V_{SS}$	5	1	1	1	1	–	1	V
		10	2	2	2	2	–	2	
		15	2	2	2	2	–	2	
Control Input High Voltage, V_{IHC}	See Fig. 6	5	3.5 (Min.)						V
		10	7 (Min.)						
		15	11 (Min.)						
Input Current, I_{IN} Max.	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 18$ V $V_{CC} \leq V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	$\pm 10^{-5}$	±0.1	μA
Crosstalk (Control Input to Signal Output)	V_C = 10 V (Sq. Wave) t_r, t_f = 20 ns R_L = 10 kΩ	10	–	–	–	–	50	–	mV
Turn-On and Turn-Off Propagation Delay	$V_{IN} = V_{DD}$ t_r, t_f = 20 ns C_L = 50 pF R_L = 1 kΩ	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Control Input Repetition Rate	$V_{is} = V_{DD}$, V_{SS} = GND, R_L = 1 kΩ to gnd, C_L = 50 pF, V_C = 10 V (Square wave centered on 5 V) t_r, t_f = 20 ns, V_{os} = ½ V_{os} @ 1 kHz	5	–	–	–	–	6	–	MHz
		10	–	–	–	–	9	–	
		15	–	–	–	–	9.5	–	
Input Capacitance, C_{IN}			–	–	–	–	5	7.5	pF

V_{DD} (V)	V_{is} (V)	Switch Input I_{is} (mA) –55°C	–40°C	+25°C	+85°C	+125°C	Switch Output, V_{os} (V) Min.	Max.
5	0	0.64	0.61	0.51	0.42	0.36	–	0.4
5	5	–0.64	–0.61	–0.51	–0.42	–0.36	4.6	–
10	0	1.6	1.5	1.3	1.1	0.9	–	0.5
10	10	–1.6	–1.5	–1.3	–1.1	–0.9	9.5	–
15	0	4.2	4	3.4	2.8	2.4	–	1.5
15	15	–4.2	–4	–3.4	–2.8	–2.4	13.5	–

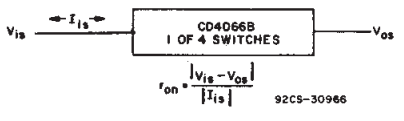


Fig. 6— Determination of r_{on} as a test condition for control input high voltage (V_{IHC}) specification.

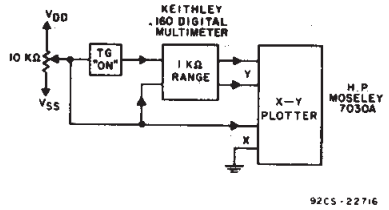


Fig. 7 — Channel on-state resistance measurement circuit.

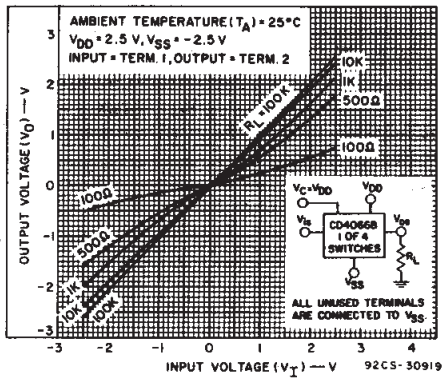


Fig. 8—Typical ON characteristics for 1 of 4 Channels.

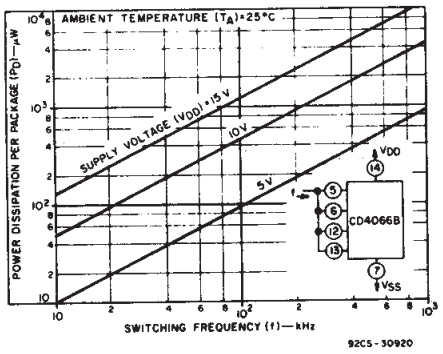


Fig. 9 — Power dissipation per package vs. switching frequency.

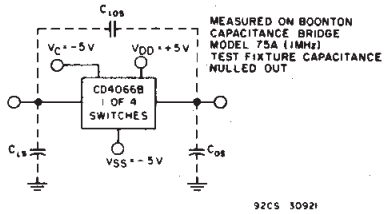


Fig. 10 — Capacitance test circuit.

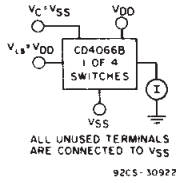


Fig. 11 – Off-switch input or output leakage.

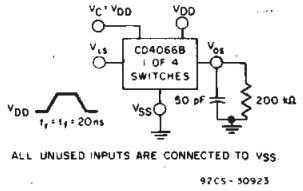


Fig. 12 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

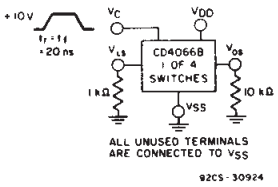


Fig. 13 – Crosstalk-control input to signal output.

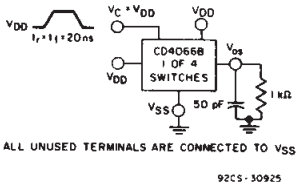


Fig. 14 – Propagation delay t_{PLH}, t_{PHL} control-signal output. Delay is measured at V_{OS} level of +10% from ground (turn-on) or on-state output level (turn-off).

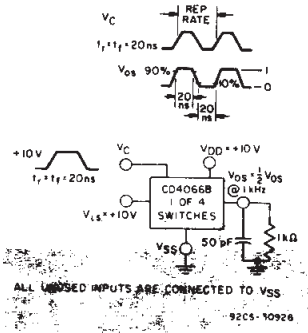


Fig. 15 – Maximum allowable control input repetition rate.

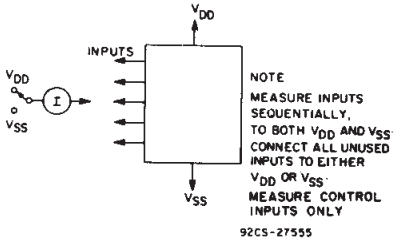


Fig. 16 – Input leakage current test circuit.

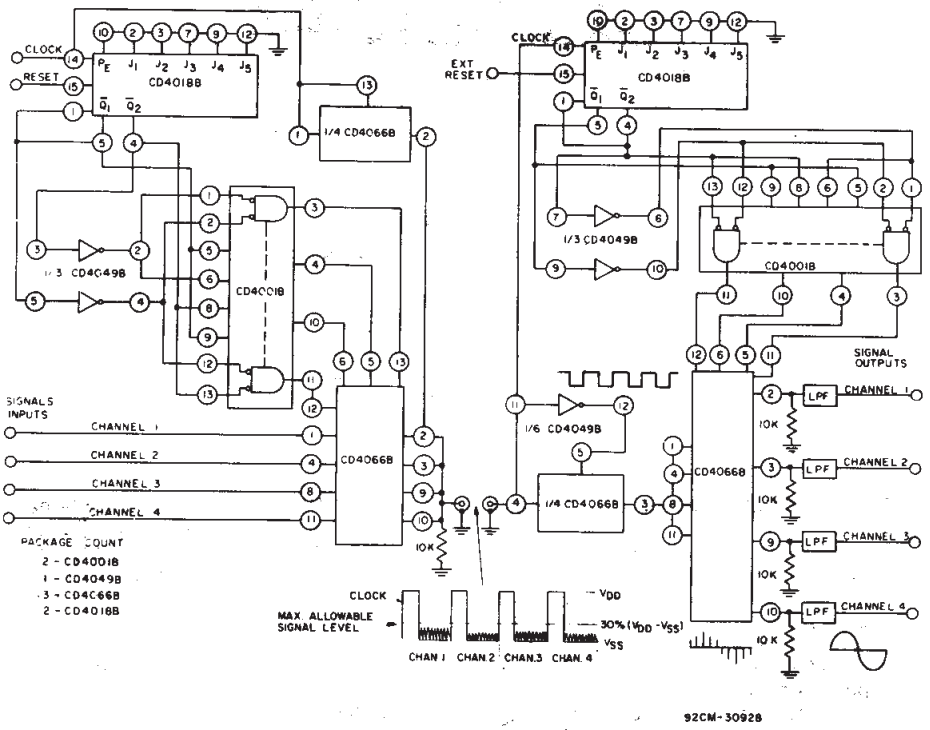


Fig. 17– 4-channel PAM multiplex system diagram.

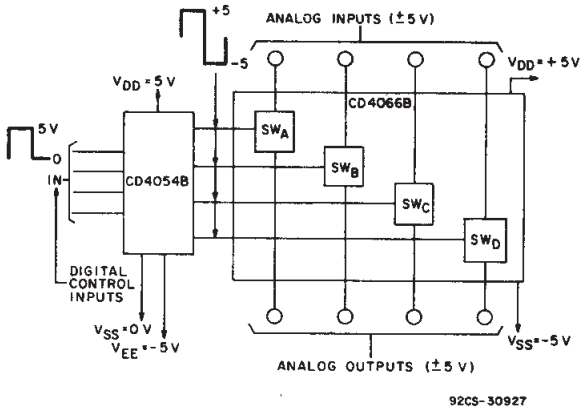
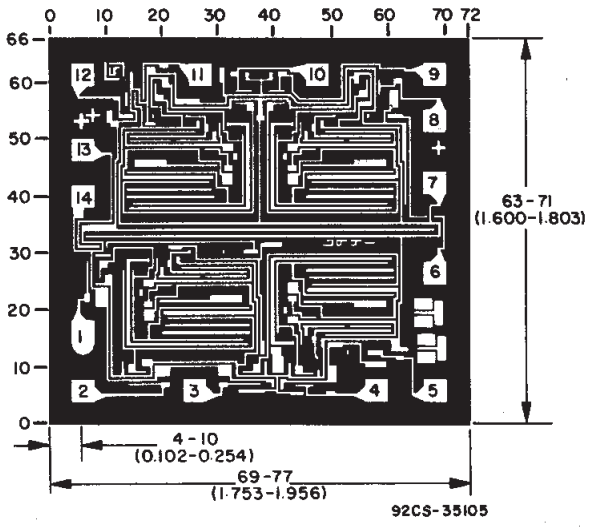


Fig. 18 – Bidirectional signal transmission via digital control logic.



CD4066BH
CHIP DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

SPECIAL CONSIDERATIONS — CD4066B

1. In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1,4,8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2,3,9, or 10.

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Orde	Butterworth	Bessel		Chebyshev (0,5 dB)		Chebyshev (2,0 dB)	
	Gain	Gain	fn	Gain	fn	Gain	fn
2	1,586	1,268	1,274	1,842	1,231	2,114	0,907
4	1,152	1,084	1,432	1,582	0,597	1,924	0,471
	2,235	1,759	1,606	2,660	1,031	2,782	0,964
6	1,068	1,040	1,607	1,537	0,396	1,891	0,316
	1,586	1,364	1,692	2,448	0,768	2,648	0,730
	2,483	2,023	1,908	2,846	1,011	2,904	0,983
8	1,038	1,024	1,781	1,522	0,297	1,879	0,238
	1,337	1,213	1,835	2,397	0,599	2,605	0,572
	1,889	1,593	1,956	2,711	0,861	2,821	0,842
	2,610	2,184	2,192	2,913	1,006	2,946	0,990