# LAMPIRAN A

# FOTO ALAT





Resistor





MCS-51



MCS-51

# LAMPIRAN B



Program LabVIEW Traffic Light



**Program LabVIEW Pada** Door Simulation



Program LabVIEW Pada Silo Simulation



Program LabVIEW Pada Parking Lot













```
Program Pada MCS-51
$mod51
     CSEG
     ORG 4000H
     LJMP START
interrupt penerimaan
     ORG 4023H
     CLR RI
     MOV A, SBUF
     MOV DPTR,#2001H
     MOVX
                 @DPTR, A
mengirimkan data ke PC
     MOV DPTR,#2000H
                 A, @DPTR
     MOVX
     mov p1,a
     MOV SBUF, A
           TI, $
     JNB
     CLR
           ΤI
     RETI
interrupt diaktifkan dan serial berada pada mode 1 dengan REN = 1
```

START: MOV SP, #30H MOV A, #90H MOV DPTR, #2003H MOVX @DPTR, A MOV SCON, #50H inisialisasi baud rate (9600 bps) MOV TMOD, #20H MOV TL1, #0FDH MOV TH1, #0FDH MOV PCON, #00H SETB TR1 SETB ES SETB EA pas: MOV R7, #10H LUPA: MOV R6, #0FFH LUPB: MOV R5, #0FFH DJNZ R5, \$ DJNZ R6, LUPB DJNZ R7, LUPA MOV DPTR,#2001H @DPTR, A MOVX mengirimkan data ke PC MOV DPTR,#2000H MOVX A, @DPTR mov p1,a MOV SBUF, A JNB TI, \$ CLR TI sjmp pas END

#### LabVIEW Tutorial on Spectral Analysis

With the LabVIEW graphical programming environment, you can quickly and easily create many different types of measurement analysis applications. LabVIEW has built-in functions for measurement analysis including RMS calculation, peak detection, harmonic analysis, filtering, and frequency analysis functions, as well as a large number of complex mathematical and statistical functions.

**Purpose:** In this tutorial, you will create a LabVIEW virtual instrument (VI) that generates a sine wave, uses one of the LabVIEW analysis functions to calculate the power spectrum of the signal with a Fast Fourier Transform (FFT), and creates a plot of the frequency spectrum.

Completion Time: This tutorial will take approximately 45 minutes.

**Programming Level:** This tutorial is designed for LabVIEW users of any level. However, if this is your first time using LabVIEW, consider starting out with our introductory tutorial entitled "Acquire, Analyze, and Present with LabVIEW". It contains detailed information about the fundamentals of graphical programming, so you can quickly become familiar with the LabVIEW environment. You can find it at http://www.ni.com/tutorials.

If you would like more in-depth technical information about spectral analysis, the National Instruments Web site offers a multimedia-based "FFT Interactive Tutorial" on the fundamentals of frequency domain measurements. It can also be found at <u>http://www.ni.com/tutorials</u>.

Follow these steps to create your own VI:

- 1.) Open your internet browser and enter <u>http://www.ni.com/info</u>. Enter "**trylvnow**" as the info code.
- 2.) If you have already created a profile, enter your e-mail address and password and click "Continue". If not, creating one will only take a few seconds; to begin, simply select "No. I need to create a profile" and click "Continue". Once you have created your profile, move on to step 3.
- 3.) Click on the "Start LabVIEW" button. A pop-up window will instruct you to do a one-time installation of a small client.
- 4.) From the LabVIEW 6.1 splash screen, choose New VI. This will open up two blank windows. The gray window titled "Untitled 1" is the front panel and will be your user interface, and the white window titled "Untitled 1 Diagram" is the block diagram, where you will create your graphical source code.
- 5.) Click on the front panel window and create the user interface shown below by performing steps 6-10.

**\*USAGE TIP:** You may also access the front panel by selecting Window»Show Panel from the block diagram menu bar.



6.) Click on the Controls palette window on the left side of the screen. The Controls palette contains objects (i.e. controls and indicators) that can be placed on the front panel to form the user interface. Mouse over the sub-palettes and you will see their descriptions in the top of the window.

**\*USAGE TIP:** If you cannot see the Controls palette, you can view it by selecting Window»Show Controls Palette from the menu or by right-clicking on a blank area on the front panel window.

**\*DEFINITION:** A **control** is a front panel object that serves as a data source, getting data from the user via the front panel and sending it to the block diagram code (e.g. a knob). An **indicator** is a front panel object that serves as a data sink, obtaining data from the block diagram code and displaying it to the front panel (e.g. a graph). A front panel object cannot be both a control and an indicator.

7.) From the Controls palette, select the Numeric sub-palette and click on the Dial control as shown in the figure below. Move the mouse to the front panel and click the left mouse button to drop the Dial onto the panel.



**\*USAGE TIP:** You can reposition the Dial control on the panel by clicking and dragging with the positioning tool, shown as an arrow on the Tools palette. To select the positioning tool, either click on it in the Tools palette or press the <TAB> key to switch the currently selected tool until the positioning tool is shown.

\*USAGE TIP: If you cannot see the Tools palette, select Window»Show Tools Palette from the menu.

- 8.) From the Numeric sub-palette, choose the Digital Control, and drop it onto the front panel.
- 9.) Click on the up arrow at the top of the Numeric sub-palette window to go back to the Controls palette, as shown below.



10.) From the Controls palette, select the Graph sub-palette and click on the Waveform Graph as shown below. Place it onto the front panel.



**\*DEFINITION:** The **Waveform Graph** is an indicator that accepts an array of data values and plots the entire array at once. This is different from the **Waveform Chart**, which scrolls data continuously, adding new data points to those already displayed.

The next step is to create the initial block diagram code. Build the block diagram pictured below by performing steps 11-28.



11.) Click on the block diagram window (behind the front panel). You should see three nodes on the block diagram. These nodes correspond to the three objects already placed on the front panel.

**\*INFO TIP**: The two control nodes (Dial and Numeric) have small black arrows on the right, and the Waveform Graph indicator has a similar arrow on the left. These arrows indicate the direction of data flow, either into or out of the node. All of the nodes are orange, indicating that they represent floating-point values, and they all contain the letters DBL, indicating that they are double precision.

12.) Note that after clicking on the block diagram window, the Controls palette has been replaced by the Functions palette. The Functions palette is used to

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build the block diagram. It contains all of the LabVIEW functions that can be combined to create your custom application.

13.) Reposition the Functions palette so that you can view the entire window on your screen.

**\*USAGE TIP:** If you cannot see the Functions palette, you may show it manually by selecting Window»Show Functions Palette from the menu.

14.) Within the Functions palette, select the Waveform sub-palette as shown below. This palette contains functions performed on the waveform data type. The waveform data type is a unique feature of LabVIEW. It is a special kind of cluster that succinctly contains both amplitude and timing information of a signal.



**\*DEFINITION**: A **cluster** is a data type that bundles together many different kinds of information, similar to several wires carrying various types of data wrapped together as one. This is also similar to the structure used in text-based programming languages.

**\*DEFINITION:** The **waveform data type** consists of a cluster of three elements. These three elements are an array of Y values containing the signal amplitude, a single value t0 that represents the start time of the signal, and a single value dt that represents the time interval between data points in the Y array. When the waveform data type is passed to the Waveform Graph, the graph interprets the data and plots the timing information on the X-axis along with the array of amplitudes on the Y-axis.

- 15.) Within the Waveform palette, select the Waveform Generation menu. The functions in this menu automatically generate many commonly used waveforms.
- 16.) Choose the Sine Wave.vi and drop it onto the block diagram.

**\*USAGE TIP:** If you would like more information on how Sine Wave.vi or any other VI works, simply activate the Context Help by selecting Help»Show Context Help or by pressing <CTRL><H>. Put the mouse pointer on any object in the block diagram, and the context help window will give a description of that VI or object. For additional in-depth information about a VI click on the "Click here for more help" button inside the Context Help window to open the LabVIEW Help page for that item. The LabVIEW Help page contains specific information about each input and output and about the function of the VI. You can also view the front panel and/or block diagram of the SineWave.vi by double-clicking on the node or right-clicking on it and selecting Open Front Panel.

- 17.) From the same Waveform Generation menu, choose the Uniform White Noise Waveform.vi and place it on the block diagram.
- 18.) Using the wiring tool (shown as a spool of wire in the Tools palette), place the mouse over the Sine Wave.vi and notice that the input and output terminals appear on the edges of the VI icon. The input or output terminal that the wiring tool is currently pointing to blinks on the block diagram as well as in the Context Help window (press <CTRL><H>), and its label is displayed in a tip-strip.
- 19.) Select the 'frequency' input by clicking on the upper left input terminal. A broken wire will now trail the mouse as you move it.
- 20.) Click on the Dial control and notice that a solid orange wire has been connected from the Dial control node to the Sine Wave.vi 'frequency' input. The orange color of the wire symbolizes a floating-point value.

\*USAGE TIP: You can click the left mouse button anytime during wiring to lock the current position of the wire onto the screen. Then you can move the mouse up or down to better control how the wire is placed. You can also move wires around by clicking and dragging them with the positioning tool (arrow). To cancel the placement of a wire, click the right mouse button during wiring or highlight the undesired wire and press <DELETE>. To eliminate all broken wires on the block diagram at once, press <CTRL><B>. The VI will not run if there are broken wires present in the block diagram.

- 21.) Rename the Dial control by double-clicking on the label with the labeling tool (capital "A"). This will highlight the label, allowing you to type in new text. Change the label to "Frequency (Hz)", since this dial has been wired to control the frequency input to the Sine Wave.vi.
- 22.) Using the same method explained in steps 19-21 above, wire the 'amplitude' input of the Sine Wave.vi to the Numeric digital control node and change the label of the Numeric control to "Amplitude."
- 23.) With the wiring tool, right-click on the 'amplitude' input of the Uniform White Noise Waveform.vi and select Create»Constant as shown below. The default amplitude of the noise is 1.00. You can change this value by doubleclicking on it with the labeling tool (capital "A") and typing in a new number. For this example, we will use the default value.



**\*DEFINITION:** A **constant** exists only on the block diagram and cannot be changed while the VI is running. This is different from a control, which exists on the front panel and can be changed at any time by the user.

- 24.) From the Waveform Generation palette, click the Up arrow at the top left of the window (described in step 9) to go back to the Waveform palette.
- 25.) From the Waveform palette, choose the Waveform Operations menu. Click on the Add Waveforms.vi and place it onto the block diagram.
- 26.) Using the wiring tool, connect the 'signal out' output of the Sine Wave.vi to the upper left 'waveform A' input of the Add Waveforms.vi
- 27.) Connect the 'signal out' output of the Uniform White Noise Waveform.vi to the 'waveform B' input of the Add Waveforms.vi.
- 28.) Connect the 'result' output terminal of the Add Waveforms.vi to the Waveform Graph indicator node. Notice that the wire used to connect these two is wide and brown in color. This type of wire represents a cluster, more specifically, the waveform data type cluster discussed previously.

At this point, you have created a working VI that generates a waveform containing a noisy sine wave and plots it on a Waveform Graph. If everything is wired correctly, you will see a white Run arrow button as the first button in the toolbar at the top of the front panel and block diagram windows. If the arrow is gray and broken, follow the debugging instructions in the tip below. If the Run arrow is solid white, there are no errors and you can now run your VI.

**\*DEBUGGING TIP:** If the Run arrow is broken, click on the broken Run arrow to view the error list. Click on an error description to highlight it and read the details given in the Details window to help solve the problem. Then, click the Show Error button. This will clearly show the problematic area on the block diagram.

29.) Go to the front panel and enter values for the frequency and amplitude of your sine wave using the operating tool (hand) to click and drag the dial and

to increment or decrement the digital control arrows. Set the frequency to 2.0 Hz and the amplitude to 5.00.

**\*USAGE TIP:** You can enter a value directly into the digital control by double-clicking the number in the field and typing in a new number.

**\*USAGE TIP:** To more precisely set the value of the frequency dial, right-click on the dial, select Visible Items and choose Digital Display. This will bring up a numeric window where you can view or change the dial value digitally.

30.) Run the VI by clicking the Run arrow. On the front panel you should see a noisy sine wave with the proper frequency and amplitude plotted on the Waveform Graph, as shown in the figure below. If you do not see this, be sure to check that you have entered non-zero values for the input frequency and amplitude and that your block diagram mimics the figure given above.



Now that we have generated the noisy sine wave, the next step is to perform the frequency spectrum analysis. LabVIEW makes this very easy by providing a built-in FFT Power Spectrum function. Create the block diagram code pictured below to calculate and plot the power spectrum of the noisy sine wave by performing steps 31-45.



- 31.) Switch to the block diagram and delete the wire connecting the Add Waveforms.vi to the Waveform Graph node by highlighting it with the positioning tool and pressing <DELETE>.
- 32.) Click the Up arrow on the Waveform Operations palette to go back to the Waveform palette. Choose the Waveform Measurements menu. Inside this menu, select the FFT Power Spectrum.vi as shown below, and drop it onto the block diagram.



**\*INFO TIP:** In general, the FFT Power Spectrum.vi accepts any waveform as an input and sends the computed power spectrum of the waveform to the output. The parameters used to determine the power spectrum are changeable, including the time-domain window type, the specific averaging method, and the units applied to the output. Use the Context Help window (<CTRL><H>) to read more about how this VI works, or look at the underlying code by double-clicking on the VI to view its contents.

- 33.) Place the wiring tool on the FFT Power Spectrum.vi icon to view the input and output terminals.
- 34.) Connect the 'time signal' input of the FFT Power Spectrum.vi to the 'result' output of the Add Waveforms.vi.
- 35.) Connect the 'power spectrum' output of the FFT Power Spectrum.vi to the Waveform Graph indicator node. Notice that the wire connecting the FFT Power Spectrum.vi to the Waveform Graph is pink. The pink color in this case denotes a general cluster data type.

**\*DEFINITION:** The Waveform Graph node itself has also changed from brown to pink. This graph is **polymorphic**, meaning that it accepts many different types of data, including waveforms, clusters, and arrays. The ability to use polymorphic functions is a feature of LabVIEW that provides versatility in your programming by not restricting you to traditional, explicit type casting rules.

Next, we will add a While Loop to run continuous iterations of the sine wave generation and frequency analysis. This is necessary in order to utilize the averaging features of the FFT Power Spectrum.vi.

- 36.) From the Waveform Measurements palette, click the Up arrow twice to go back to the general Functions palette.
- 37.) Select the Structures sub-palette and choose the While Loop structure. Then, place the While Loop around the existing code by clicking and holding down the mouse button at the upper left corner of the block diagram window and dragging the box to enclose the entire diagram.
- 38.) Go to the front panel. Click the Up arrow until you see the general Controls palette.
- 39.) Select the Boolean sub-palette, and choose the STOP button. Drop the STOP button onto the front panel.

**\*USAGE TIP:** It is important to always have a way to stop any loops that you create in LabVIEW. The STOP button is the best way to easily control while loops.

- 40.) Go back to the block diagram and locate the STOP button node. Use the positioning tool to drag this node into the while loop, if it is not already there.
- 41.) Right-click on the continuation terminal (green circular arrow) of the while loop in the bottom right corner and select Stop if True, as shown below. You will see the terminal change from a green arrow to a red stop sign.



- 42.) Wire the STOP button node to the continuation terminal with the wiring tool.
- 43.) Go to the front panel and change the range of the frequency dial to 0-500 Hz using the labeling tool (capital "A"). Double-click on the highest dial value marker and type "500." Press Enter or click on the check box at the upper left corner of the window to confirm your entry.
- 44.) With the labeling tool, double-click on the 'Time' label for the X-axis of the Waveform Graph and change it to 'Frequency.'
- 45.) Set the dial to 200 Hz using the operating tool.
- 46.) If the run arrow is solid white and there are no errors in the block diagram, run the VI and observe its behavior. You should see a plot of the power spectrum on the Waveform Graph, with a spike in the plot at the frequency designated by the Dial control, as shown below. Turn the dial and notice the movement of the frequency spike.
- 47.) Push the STOP button to stop the VI and continue editing.

**\*DEBUGGING TIP:** Note that the VI now must be stopped using the STOP button. If the Run arrow is solid black, the VI is still running and must be stopped before it can be edited.



The FFT Power Spectrum.vi has built-in averaging capabilities to display the running average of multiple power spectrum calculations. To add these averaging capabilities and other features to your spectral analysis VI, modify your block diagram as shown below by performing steps 48-53.



- 48.) Go to the block diagram and place the wiring tool over the 'window' input of the FFT Power Spectrum.vi.
- 49.) Right-click and select Create»Control. This will create a 'window' control node on the block diagram and will automatically wire it to the terminal

from which it was created. It will also place a new control on the front panel.

- 50.) Use the positioning tool to click on the 'window' node and move it away from the other input terminals. Be sure when you are moving objects to highlight the entire object, not just the label.
- 51.) Locate the new ring control on the front panel (it may be off the screen below). Use the positioning tool to click on the 'window' control and drag it to a better location near the other front panel objects.
- 52.) Repeat the above steps to create controls for the 'averaging parameters' input, and the 'dB On' input. Doing this will add to the front panel a cluster control with elements specifying the 'averaging parameters', as well as a vertical slide switch control for 'dB On'.



53.) Set the front panel to the parameters shown below and run the VI.

Congratulations! You have created a fully functional sine wave spectral analyzer virtual instrument. Try adjusting the different averaging methods, the number of averages, and the windowing properties to see how they affect the power spectrum output.

You can bring any signal type into the provided LabVIEW signal analysis functions, whether the signal is generated, like the noisy sine wave in this example, or measured with hardware and acquired through the PC for your particular application. This example gives a small sample of the many powerful tools that LabVIEW has to offer and demonstrates the ease with which you can create your own custom signal analysis applications.

## Features

- Compatible with MCS-51<sup>™</sup> Products
- 4K Bytes of In-System Reprogrammable Flash Memory

   Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

# Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.





8-bit Microcontroller with 4K Bytes Flash

# AT89C51

Not Recommended for New Designs. Use AT89S51.





## **Block Diagram**



AT89C51

The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

## **Pin Description**

#### VCC

Supply voltage.

#### GND

Ground.

#### Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed loworder address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

#### Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

## Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

#### Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ( $I_{IL}$ ) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

#### RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

#### ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE





pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

#### PSEN

Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, <u>PSEN</u> is activated twice each machine cycle, except that two <u>PSEN</u> activations are skipped during each access to external data memory.

#### EA/VPP

External Access Enable.  $\overline{EA}$  must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed,  $\overline{EA}$  will be internally latched on reset.

 $\overline{\text{EA}}$  should be strapped to  $V_{\text{CC}}$  for internal program executions.

This pin also receives the 12-volt programming enable voltage ( $V_{PP}$ ) during Flash programming, for parts that require 12-volt  $V_{PP}$ .

#### XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

#### XTAL2

Output from the inverting oscillator amplifier.

## **Oscillator Characteristics**

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

## **Idle Mode**

In idle mode, the CPU puts itself to sleep while all the onchip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

#### Figure 1. Oscillator Connections





## Status of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Note:

AT89C51

Figure 2. External Clock Drive Configuration



## **Power-down Mode**

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Regis-

## Lock Bit Protection Modes

ters retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before  $V_{CC}$  is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

## **Program Memory Lock Bits**

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the  $\overline{EA}$  pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of  $\overline{EA}$  be in agreement with the current logic level at that pin in order for the device to function properly.

	Program	Lock Bits		
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	Р	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the Flash is disabled
3	Р	Р	U	Same as mode 2, also verify is disabled
4	Р	Р	Р	Same as mode 3, also external execution is disabled





## **Programming the Flash**

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage ( $V_{CC}$ ) program enable signal. The low-voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third-party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V <sub>PP</sub> = 12V	V <sub>PP</sub> = 5V
Top-side Mark	AT89C51	AT89C51
	хххх	xxxx-5
	yyww	yyww
Signature	(030H) = 1EH	(030H) = 1EH
	(031H) = 51H	(031H) = 51H
	(032H) =F FH	(032H) = 05H

The AT89C51 code memory array is programmed byte-bybyte in either programming mode. *To program any nonblank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.* 

**Programming Algorithm:** Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figure 3 and Figure 4. To program the AT89C51, take the following steps.

- 1. Input the desired memory location on the address lines.
- 2. Input the appropriate data byte on the data lines.
- 3. Activate the correct combination of control signals.
- 4. Raise  $\overline{EA}/V_{PP}$  to 12V for the high-voltage programming mode.
- 5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address

and data for the entire array or until the end of the object file is reached.

**Data Polling:** The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

**Ready/Busy:** The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase:** The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

- (030H) = 1EH indicates manufactured by Atmel
- (031H) = 51H indicates 89C51
- (032H) = FFH indicates 12V programming
- (032H) = 05H indicates 5V programming

## **Programming Interface**

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is selftimed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

## **Flash Programming Modes**

Mode		RST	PSEN	ALE/PROG	EA/V <sub>PP</sub>	P2.6	P2.7	P3.6	P3.7
Write Code Data		н	L	~	H/12V	L	н	Н	Н
Read Code Data		Н	L	Н	н	L	L	н	Н
Write Lock	Bit - 1	н	L	~	H/12V	н	н	Н	Н
	Bit - 2	н	L	~	H/12V	н	н	L	L
	Bit - 3	Н	L	~	H/12V	н	L	Н	L
Chip Erase		н	L	(1)	H/12V	н	L	L	L
Read Signature Byte		Н	L	Н	Н	L	L	L	L

Note: 1. Chip Erase requires a 10 ms PROG pulse.

#### Figure 3. Programming the Flash



#### Figure 4. Verifying the Flash





## Flash Programming and Verification Waveforms - High-voltage Mode ( $V_{PP} = 12V$ )



Flash Programming and Verification Waveforms - Low-voltage Mode (V<sub>PP</sub> = 5V)



# AT89C51

## **Flash Programming and Verification Characteristics**

 $T_{A}$  = 0°C to 70°C,  $V_{CC}$  = 5.0  $\pm 10\%$ 

Symbol	Parameter	Min	Max	Units
V <sub>PP</sub> <sup>(1)</sup>	Programming Enable Voltage	11.5	12.5	V
I <sub>PP</sub> <sup>(1)</sup>	Programming Enable Current		1.0	mA
1/t <sub>CLCL</sub>	Oscillator Frequency	3	24	MHz
t <sub>AVGL</sub>	Address Setup to PROG Low	48t <sub>CLCL</sub>		
t <sub>GHAX</sub>	Address Hold after PROG	48t <sub>CLCL</sub>		
t <sub>DVGL</sub>	Data Setup to PROG Low	48t <sub>CLCL</sub>		
t <sub>GHDX</sub>	Data Hold after PROG	48t <sub>CLCL</sub>		
t <sub>EHSH</sub>	P2.7 ( $\overline{\text{ENABLE}}$ ) High to V <sub>PP</sub>	48t <sub>CLCL</sub>		
t <sub>SHGL</sub>	V <sub>PP</sub> Setup to PROG Low	10		μs
t <sub>GHSL</sub> <sup>(1)</sup>	V <sub>PP</sub> Hold after PROG	10		μs
t <sub>GLGH</sub>	PROG Width	1	110	μs
t <sub>AVQV</sub>	Address to Data Valid		48t <sub>CLCL</sub>	
t <sub>ELQV</sub>	ENABLE Low to Data Valid		48t <sub>CLCL</sub>	
t <sub>EHQZ</sub>	Data Float after ENABLE	0	48t <sub>CLCL</sub>	
t <sub>GHBL</sub>	PROG High to BUSY Low		1.0	μs
t <sub>wc</sub>	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.





## **Absolute Maximum Ratings\***

Operating Temperature55°C to +125°C
Storage Temperature65°C to +150°C
Voltage on Any Pin with Respect to Ground1.0V to +7.0V
Maximum Operating Voltage6.6V
DC Output Current

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **DC Characteristics**

 $T_A = -40^{\circ}C$  to 85°C,  $V_{CC} = 5.0V \pm 20\%$  (unless otherwise noted)

Symbol	Parameter	Condition	Min	Мах	Units
V <sub>IL</sub>	Input Low-voltage	(Except EA)	-0.5	0.2 V <sub>CC</sub> - 0.1	V
V <sub>IL1</sub>	Input Low-voltage (EA)		-0.5	0.2 V <sub>CC</sub> - 0.3	V
V <sub>IH</sub>	Input High-voltage	(Except XTAL1, RST)	0.2 V <sub>CC</sub> + 0.9	V <sub>CC</sub> + 0.5	V
V <sub>IH1</sub>	Input High-voltage	(XTAL1, RST)	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low-voltage <sup>(1)</sup> (Ports 1,2,3)	I <sub>OL</sub> = 1.6 mA		0.45	V
V <sub>OL1</sub>	Output Low-voltage <sup>(1)</sup> (Port 0, ALE, PSEN)	I <sub>OL</sub> = 3.2 mA		0.45	V
		$I_{OH}$ = -60 µA, $V_{CC}$ = 5V ±10%	2.4		V
V <sub>OH</sub>	Output High-voltage (Ports 1,2,3, ALE, PSEN)	I <sub>OH</sub> = -25 μA	0.75 V <sub>CC</sub>		V
		I <sub>OH</sub> = -10 μA	0.9 V <sub>CC</sub>		V
V <sub>OH1</sub>	Output High-voltage	$I_{OH}$ = -800 µA, $V_{CC}$ = 5V ±10%	2.4		V
		I <sub>OH</sub> = -300 μA	0.75 V <sub>CC</sub>		V
		I <sub>OH</sub> = -80 μA	0.9 V <sub>CC</sub>		V
IIL	Logical 0 Input Current (Ports 1,2,3)	V <sub>IN</sub> = 0.45V		-50	μA
$I_{TL}$	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2V$ , VCC = 5V ±10%		-650	μΑ
ILI	Input Leakage Current (Port 0, $\overline{EA}$ )	0.45 < V <sub>IN</sub> < V <sub>CC</sub>		±10	μA
RRST	Reset Pull-down Resistor		50	300	KΩ
C <sub>IO</sub>	Pin Capacitance	Test Freq. = 1 MHz, T <sub>A</sub> = 25°C		10	pF
		Active Mode, 12 MHz		20	mA
	Power Supply Current	Idle Mode, 12 MHz		5	mA
I <sub>CC</sub>	Devices device Marda (2)	$V_{CC} = 6V$		100	μA
		$V_{CC} = 3V$		40	μA

Notes: 1. Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows:

Maximum I<sub>OL</sub> per port pin: 10 mA

Maximum I<sub>OL</sub> per 8-bit port: Port 0: 26 mA

Ports 1, 2, 3: 15 mA

Maximum total  $I_{\rm OL}$  for all output pins: 71 mA

If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum  $V_{CC}$  for Power-down is 2V.

## AT89C51

## **AC Characteristics**

Under operating conditions, load capacitance for Port 0, ALE/ $\overline{PROG}$ , and  $\overline{PSEN} = 100 \text{ pF}$ ; load capacitance for all other outputs = 80 pF.

## **External Program and Data Memory Characteristics**

		12 MHz	Oscillator	16 to 24 MHz Oscillator		
Symbol	Parameter	Min	Max	Min	Max	Units
1/t <sub>CLCL</sub>	Oscillator Frequency			0	24	MHz
t <sub>LHLL</sub>	ALE Pulse Width	127		2t <sub>CLCL</sub> -40		ns
t <sub>AVLL</sub>	Address Valid to ALE Low	43		t <sub>CLCL</sub> -13		ns
t <sub>LLAX</sub>	Address Hold after ALE Low	48		t <sub>CLCL</sub> -20		ns
t <sub>LLIV</sub>	ALE Low to Valid Instruction In		233		4t <sub>CLCL</sub> -65	ns
t <sub>LLPL</sub>	ALE Low to PSEN Low	43		t <sub>CLCL</sub> -13		ns
t <sub>PLPH</sub>	PSEN Pulse Width	205		3t <sub>CLCL</sub> -20		ns
t <sub>PLIV</sub>	PSEN Low to Valid Instruction In		145		3t <sub>CLCL</sub> -45	ns
t <sub>PXIX</sub>	Input Instruction Hold after PSEN	0		0		ns
t <sub>PXIZ</sub>	Input Instruction Float after PSEN		59		t <sub>CLCL</sub> -10	ns
t <sub>PXAV</sub>	PSEN to Address Valid	75		t <sub>CLCL</sub> -8		ns
t <sub>AVIV</sub>	Address to Valid Instruction In		312		5t <sub>CLCL</sub> -55	ns
t <sub>PLAZ</sub>	PSEN Low to Address Float		10		10	ns
t <sub>RLRH</sub>	RD Pulse Width	400		6t <sub>CLCL</sub> -100		ns
t <sub>WLWH</sub>	WR Pulse Width	400		6t <sub>CLCL</sub> -100		ns
t <sub>RLDV</sub>	RD Low to Valid Data In		252		5t <sub>CLCL</sub> -90	ns
t <sub>RHDX</sub>	Data Hold after RD	0		0		ns
t <sub>RHDZ</sub>	Data Float after RD		97		2t <sub>CLCL</sub> -28	ns
t <sub>LLDV</sub>	ALE Low to Valid Data In		517		8t <sub>CLCL</sub> -150	ns
t <sub>AVDV</sub>	Address to Valid Data In		585		9t <sub>CLCL</sub> -165	ns
t <sub>LLWL</sub>	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3t <sub>CLCL</sub> -50	3t <sub>CLCL</sub> +50	ns
t <sub>AVWL</sub>	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4t <sub>CLCL</sub> -75		ns
t <sub>QVWX</sub>	Data Valid to WR Transition	23		t <sub>CLCL</sub> -20		ns
t <sub>QVWH</sub>	Data Valid to WR High	433		7t <sub>CLCL</sub> -120		ns
t <sub>WHQX</sub>	Data Hold after WR	33		t <sub>CLCL</sub> -20		ns
t <sub>RLAZ</sub>	RD Low to Address Float		0		0	ns
t <sub>WHLH</sub>	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t <sub>CLCL</sub> -20	t <sub>CLCL</sub> +25	ns





## **External Program Memory Read Cycle**



## **External Data Memory Read Cycle**





## **External Data Memory Write Cycle**

## **External Clock Drive Waveforms**



## **External Clock Drive**

Symbol	Parameter	Min	Мах	Units
1/t <sub>CLCL</sub>	Oscillator Frequency	0	24	MHz
t <sub>CLCL</sub>	Clock Period	41.6		ns
t <sub>CHCX</sub>	High Time	15		ns
t <sub>CLCX</sub>	Low Time	15		ns
t <sub>CLCH</sub>	Rise Time		20	ns
t <sub>CHCL</sub>	Fall Time		20	ns





## Serial Port Timing: Shift Register Mode Test Conditions

(V<sub>CC</sub> = 5.0 V  $\pm$ 20%; Load Capacitance = 80 pF)

		12 MH	Iz Osc	Variable Oscillator		Units
Symbol	Parameter	Min	Max	Min	Мах	
t <sub>XLXL</sub>	Serial Port Clock Cycle Time	1.0		12t <sub>CLCL</sub>		μs
t <sub>QVXH</sub>	Output Data Setup to Clock Rising Edge	700		10t <sub>CLCL</sub> -133		ns
t <sub>XHQX</sub>	Output Data Hold after Clock Rising Edge	50		2t <sub>CLCL</sub> -117		ns
t <sub>XHDX</sub>	Input Data Hold after Clock Rising Edge	0		0		ns
t <sub>XHDV</sub>	Clock Rising Edge to Input Data Valid		700		10t <sub>CLCL</sub> -133	ns

## Shift Register Mode Timing Waveforms



# AC Testing Input/Output Waveforms<sup>(1)</sup>

## Float Waveforms<sup>(1)</sup>



Note: 1. AC Inputs during testing are driven at  $V_{CC}$  - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at  $V_{IH}$  min. for a logic 1 and  $V_{IL}$  max. for a logic 0.



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V<sub>OH</sub>/V<sub>OL</sub> level occurs.



Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ±20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0° C to 70° C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40° C to 85° C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
16	5V ±20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0° C to 70° C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40° C to 85° C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
20	5V ±20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0° C to 70° C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40° C to 85° C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	
24	5V ±20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0° C to 70° C)
		AT89C51-24PC	40P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40° C to 85° C)
		AT89C51-24PI	40P6	
		AT89C51-24QI	44Q	

Package Type				
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)			
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)			
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)			
44Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)			





## **Packaging Information**





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## ULN2801A ULN2802A - ULN2803A ULN2804A - ULN2805A

## **EIGHT DARLINGTON ARRAYS**

- EIGHT DARLINGTONS WITH COMMON EMIT-TERS
- OUTPUT CURRENT TO 500 mA
- OUTPUT VOLTAGE TO 50 V
- INTEGRAL SUPPRESSION DIODES
- VERSIONS FOR ALL POPULAR LOGIC FAMI-LIES
- OUTPUT CAN BE PARALLELED
- INPUTS PINNED OPPOSITE OUTPUTS TO SIMPLIFY BOARD LAYOUT



#### **PIN CONNECTION** (top view)

#### DESCRIPTION

The ULN2801A-ULN2805A each contain eight darlington transistors with common emitters and integral suppression diodes for inductive loads. Each darlington features a peak load current rating of 600mA (500mA continuous) and can withstand at least 50V in the off state. Outputs may be paralleled for higher current capability.

Five versions are available to simplify interfacing to standard logic families : the ULN2801A is designed for general purpose applications with a current limit resistor; the ULN2802A has a 10.5k $\Omega$  input resistor and zener for 14-25V PMOS; the ULN2803A has a 2.7k $\Omega$  input resistor for 5V TTL and CMOS; the ULN2804A has a 10.5k $\Omega$  input resistor for 6-15V CMOS and the ULN2805A is designed to sink a minimum of 350mA for standard and Schottky TTL where higher output current is required.

All types are supplied in a 18-lead plastic DIP with a copperlead from and feature the convenient inputopposite-output pinout to simplify board layout.



September 1997

## SCHEMATIC DIAGRAM AND ORDER CODES

For ULN2801A (each driver for PMOS-CMOS)



For ULN2803A (each driver for 5 V, TTL/CMOS)



For ULN2805A (each driver for high out TTL)



For ULN2802A (each driver for 14-15 V PMOS)



For ULN2804A (each driver for 6-15 V CMOS/PMOS



#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
Vo	Output Voltage	50	V
Vi	Input Voltage for ULN2802A, UL2803A, ULN2804A for ULN2805A	30 15	V
lc	Continuous Collector Current	500	mA
Ι <sub>Β</sub>	Continuous Base Current	25	mA
P <sub>tot</sub>	Power Dissipation (one Darlington pair) (total package)	1.0 2.25	W
Tamb	Operating Ambient Temperature Range	– 20 to 85	°C
T <sub>stg</sub>	Storage Temperature Range	- 55 to 150	°C
Tj	Junction Temperature Range	– 20 to 150	°C

#### THERMAL DATA

Symbol	Parameter	Value	Unit
R <sub>th j–amb</sub>	Thermal Resistance Junction-ambient Max.	55	°C/W

## **ELECTRICAL CHARACTERISTICS** (T<sub>amb</sub> = 25<sup>o</sup>C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit	Fig.
ICEX	Output Leakage Current	$V_{CE} = 50V$ Tamb = 70°C, V <sub>CE</sub> = 50V Tamb = 70°C			50 100	μΑ μΑ	1a 1a
		for ULN2802A $V_{CE} = 50V, V_i = 6V$ for ULN2804A			500	μA	1b
		$V_{CE} = 50V, V_i = 1V$			500	μA	1b
V <sub>CE(sat)</sub>	Collector-emitter Saturation Voltage	$\begin{array}{l} I_{C} = 100 m A,  I_{B} = 250 \mu A \\ I_{C} = 200 m A,  I_{B} = 350 \mu A \\ I_{C} = 350 m A,  I_{B} = 500 \mu A \end{array}$		0.9 1.1 1.3	1.1 1.3 1.6	V V V	2
l <sub>i(on)</sub>	Input Current	$\begin{array}{llllllllllllllllllllllllllllllllllll$		0.82 0.93 0.35 1 1.5	1.25 1.35 0.5 1.45 2.4	mA mA mA mA	3
I <sub>i(off)</sub>	Input Current	$T_{amb} = 70^{\circ}C, I_{C} = 500 \mu A$	50	65		μA	4
Vi(on)	Input Voltage	$\begin{array}{l} \text{V}_{CE} = 2 \ \text{V} \\ \text{for ULN2802A} \\ \text{I}_{C} = 300\text{mA} \\ \text{for ULN2803A} \\ \text{I}_{C} = 250\text{mA} \\ \text{I}_{C} = 250\text{mA} \\ \text{I}_{C} = 300\text{mA} \\ \text{I}_{C} = 300\text{mA} \\ \text{I}_{C} = 125\text{mA} \\ \text{I}_{C} = 125\text{mA} \\ \text{I}_{C} = 275\text{mA} \\ \text{I}_{C} = 275\text{mA} \\ \text{I}_{C} = 350\text{mA} \\ \text{for ULN2805A} \\ \text{I}_{C} = 350\text{mA} \\ \end{array}$			13 2.4 2.7 3 5 6 7 8 2.4		5
h <sub>FE</sub>	DC Forward Current Gain	for ULN2801A $V_{CE} = 2V$ , $I_C = 350mA$	1000			_	2
Ci	Input Capacitance			15	25	pF	-
t <sub>PLH</sub>	Turn-on Delay Time	0.5 V <sub>i</sub> to 0.5 V <sub>o</sub>		0.25	1	μs	-
<b>t</b> PHL	Turn-off Delay Time	0.5 Vi to 0.5 Vo		0.25	1	μs	-
I <sub>R</sub>	Clamp Diode Leakage Current	$V_{R} = 50V$ $T_{amb} = 70^{\circ}C, V_{R} = 50V$			50 100	μΑ μΑ	6 6
V <sub>F</sub>	Clamp Diode Forward Voltage	I <sub>F</sub> = 350mA		1.7	2	V	7



### **TEST CIRCUITS**

## Figure 1a.



## Figure 2.



## Figure 4.



## Figure 6.



Figure 1b.



Figure 3.



Figure 5.



Figure 7.





Figure 8 : Collector Current as a Function of Saturation Voltage.



Figure 10 : Allowable Average Power Dissipation as a Function of Ambient Temperature.



Figure 12 : Peak Collector Current as a Function of Duty.



Figure 9 : Collector Current as a Function of Input Current.



Figure 11 : Peak Collector Current as a Function of Duty Cycle.



Figure 13 : Input Current as a Function of Input Voltage (for ULN2802A).





## ULN2801A - ULN2802A - ULN2803A - ULN2804A - ULN2805A

Figure 14 : Input Current as a Function of Input Voltage (for ULN2804A)

Figure 15 : Input Current as a Function of Input Voltage (for ULN2803A)







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	DIP18	PACKAGE	MECHANICAL	DATA
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DIM.	mm			inch			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
a1	0.254			0.010			
В	1.39		1.65	0.055		0.065	
b		0.46			0.018		
b1		0.25			0.010		
D			23.24			0.915	
E		8.5			0.335		
е		2.54			0.100		
e3		20.32			0.800		
F			7.1			0.280	
I			3.93			0.155	
L		3.3			0.130		
z		1.27	1.59		0.050	0.063	



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