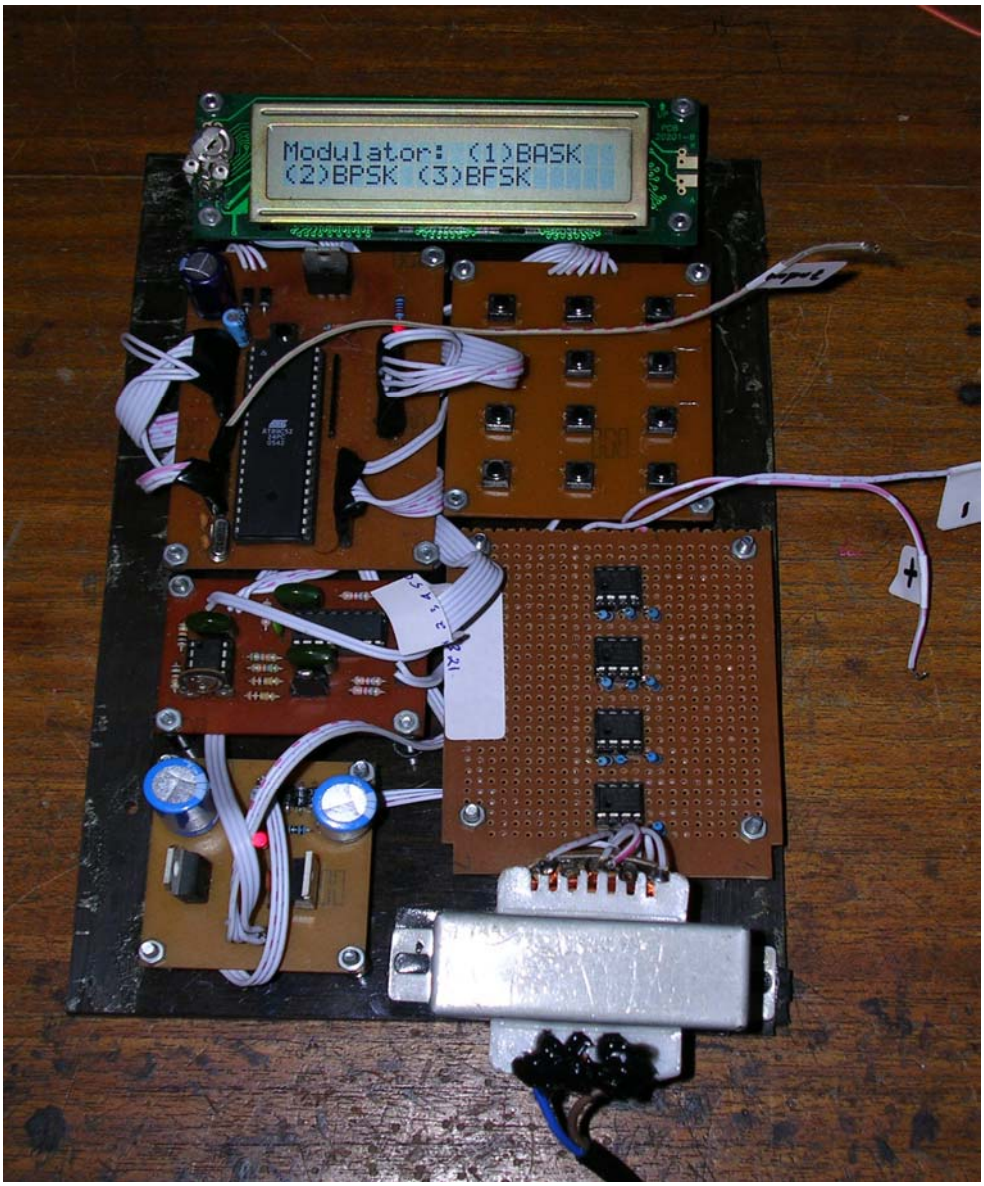
LAMPIRAN A
FOTO RANGKAIAN MODULATOR DIGITAL

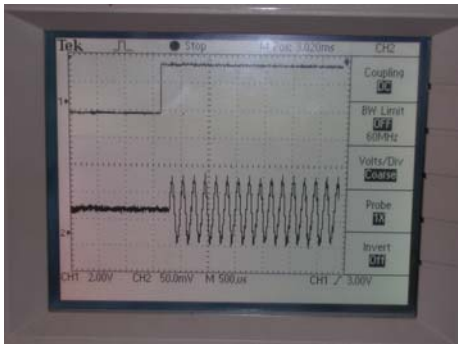

Modulator: (1)BASK
(2)BPSK (3)BFSK

LAMPIRAN B

FOTO SINYAL

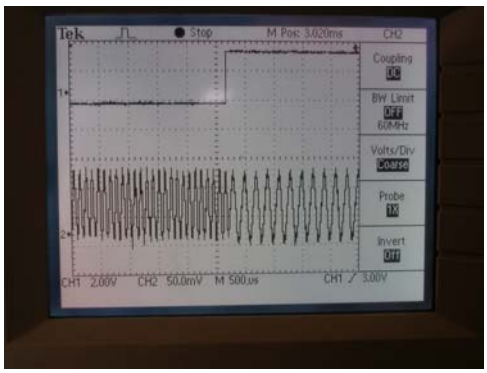
Sinyal dengan input 300bps

BASK



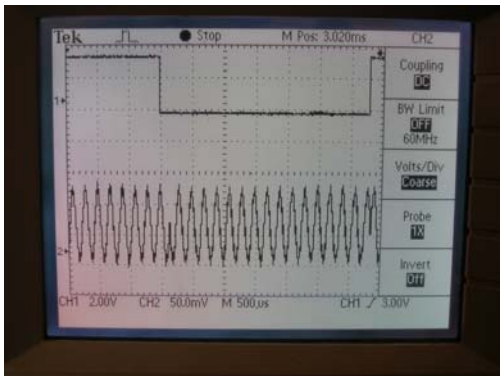
Time/div 0.5ms

BFSK



Time/div 0.5ms

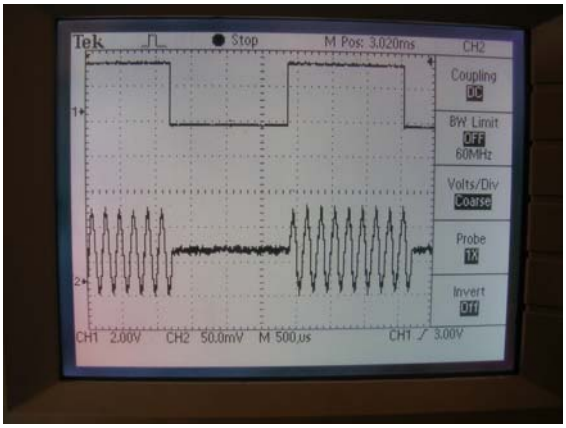
BPSK



Time/div 0.5ms

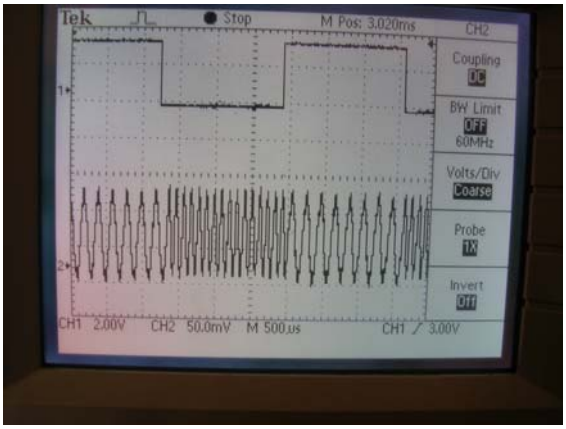
Sinyal dengan input 900bps

BASK



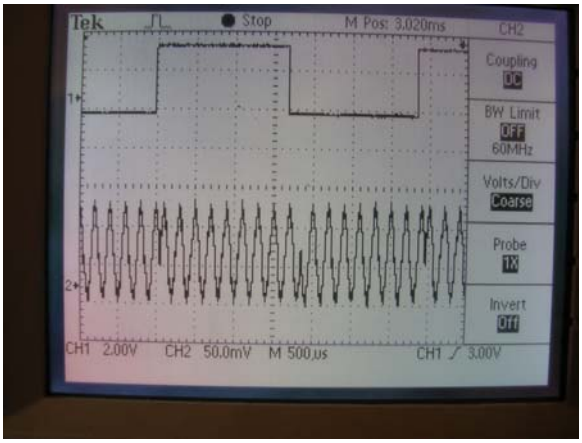
Time/div 0.5ms

BFSK



Time/div 0.5ms

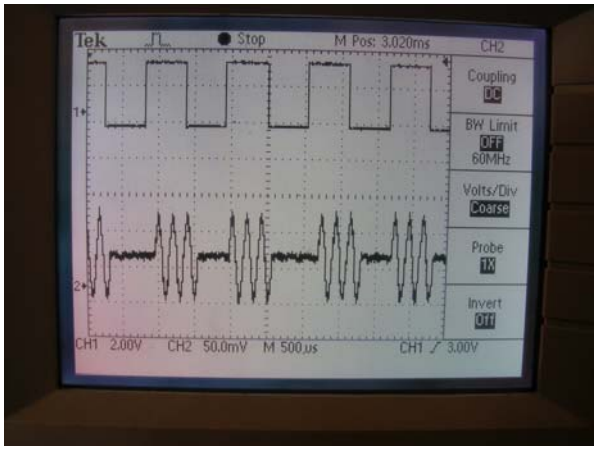
BPSK



Time/div 0.5ms

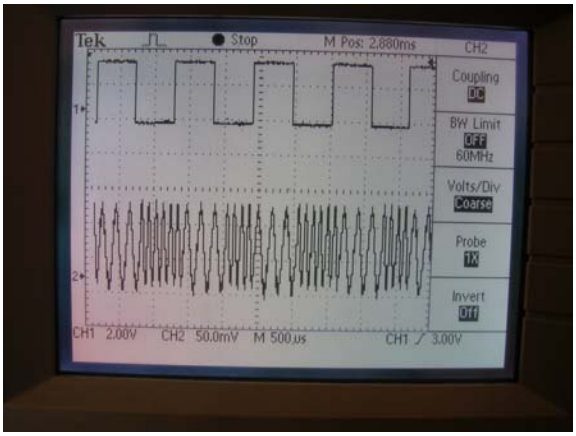
Sinyal dengan input 1800bps

BASK



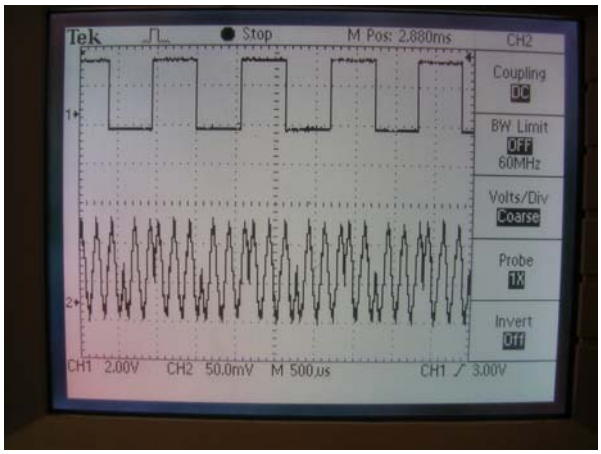
Time/div 0.5ms

BFSK



Time/div 0.5ms

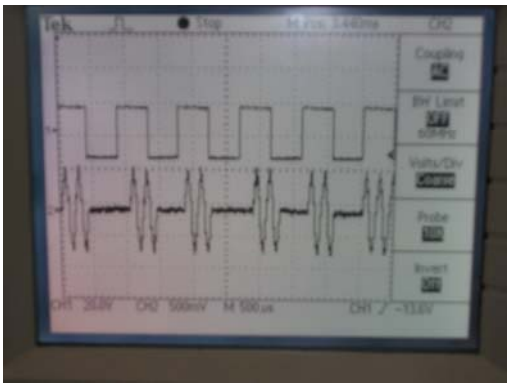
BPSK



Time/div 0.5ms

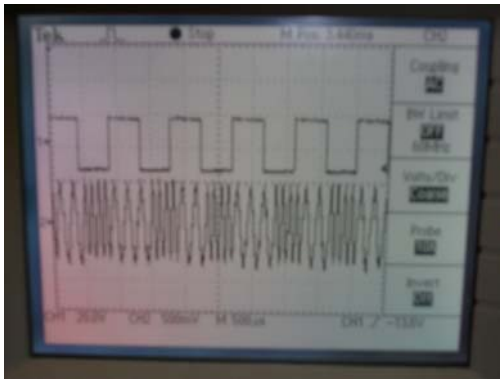
Sinyal Dengan Input 2200bps

BASK



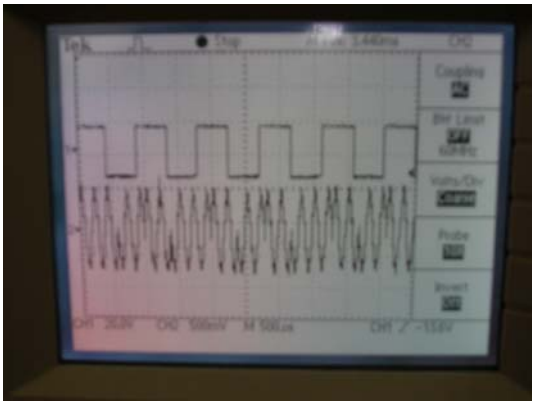
Time/Div 0.5ms

BFSK



Time/Div 0.5ms

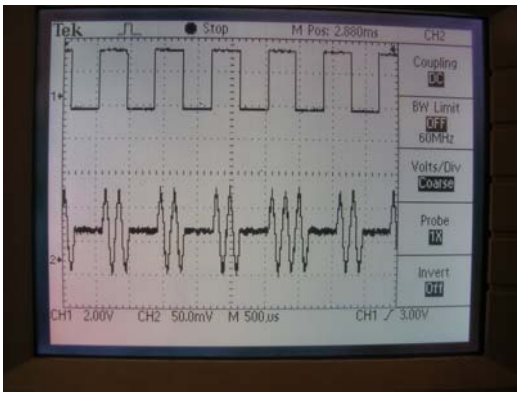
BPSK



Time/Div 0.5ms

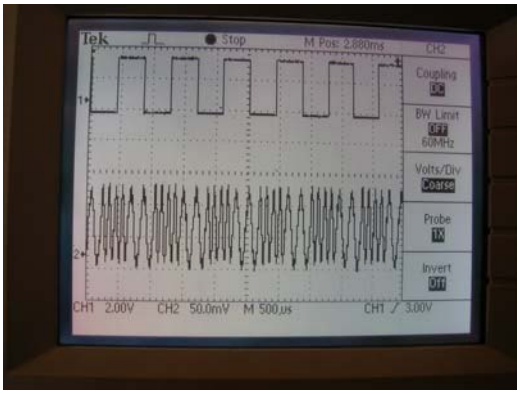
Sinyal Dengan input 2400bps

BASK



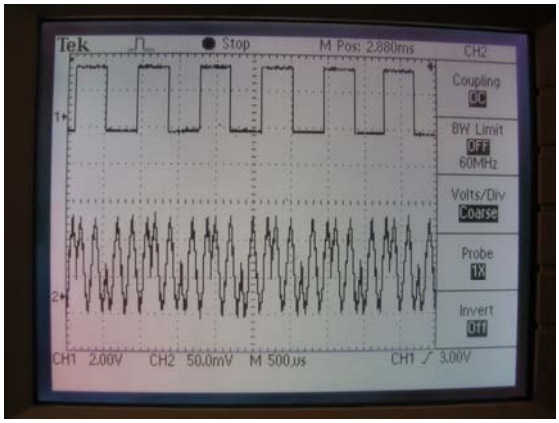
Time/div 0.5ms

BFSK



Time/div 0.5ms

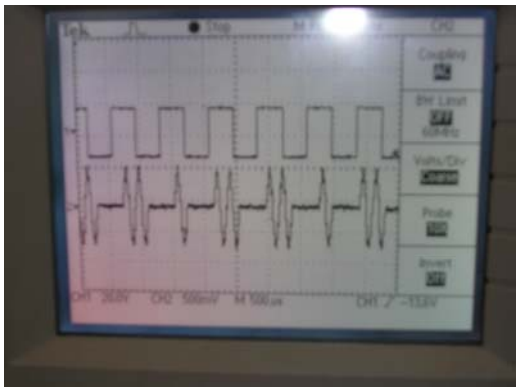
BPSK



Time/div 0.5ms

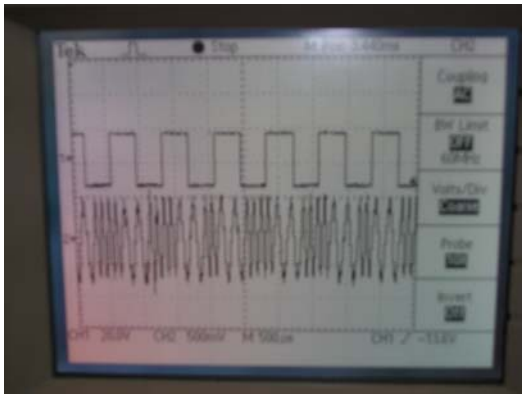
Sinyal Dengan Input 2600bps

BASK



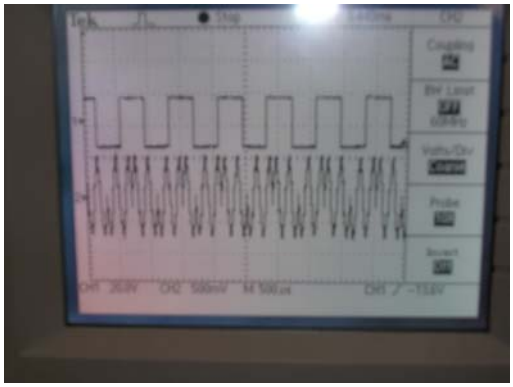
Time/Div 0.5ms

BFSK



Time/Div 0.5ms

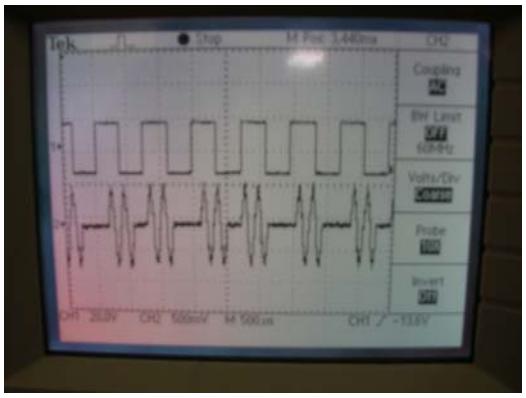
BPSK



Time/Div 0.5ms

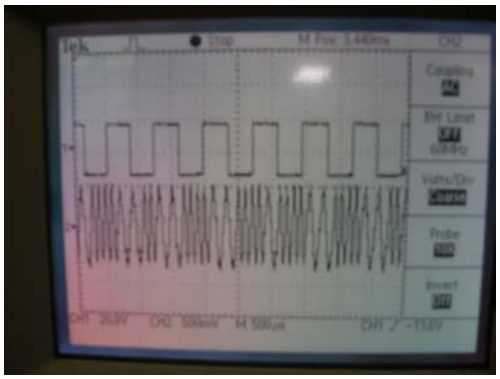
Sinyal Dengan Input 3000bps

BASK



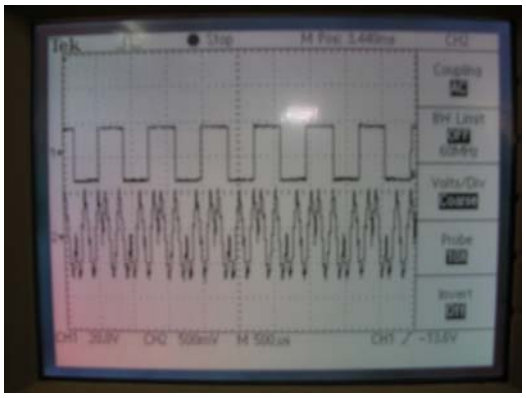
Time/Div 0.5ms

BFSK



Time/Div 0.5ms

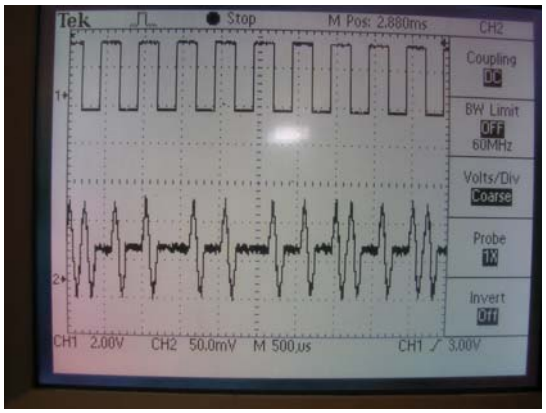
BPSK



Time/Div 0.5ms

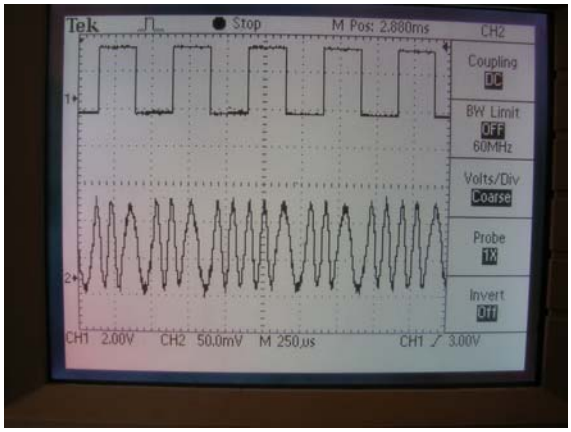
Sinyal Dengan Input 4000bps

BASK



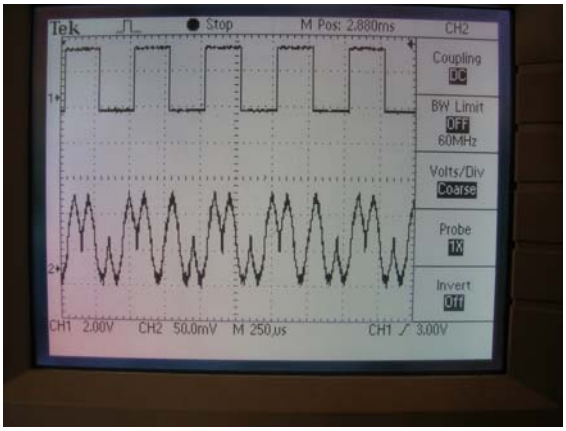
Time/div 0.5ms

BFSK



Time/div 0.25ms

BPSK



Time/div 0.25ms

LAMPIRAN C

DATA ROM SINUS

Data ROM Sinus

No	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
1	80	36	E0	71	FE	106	C4
2	83	37	E2	72	FE	107	C1
3	86	38	E4	73	FD	108	BF
4	89	39	E6	74	FC	109	BC
5	8C	40	E8	75	FC	110	B9
6	8F	41	EA	76	FB	111	B6
7	92	42	EC	77	FA	112	B3
8	95	43	ED	78	F9	113	B0
9	98	44	EF	79	F8	114	AE
10	9C	45	F0	80	F7	115	AB
11	9F	46	F2	81	F6	116	A8
12	A2	47	F3	82	F5	117	A5
13	A5	48	F5	83	F3	118	A2
14	A8	49	F6	84	F2	119	9F
15	AB	50	F7	85	F0	120	9C
16	AE	51	F8	86	EF	121	98
17	B0	52	F9	87	ED	122	95
18	B3	53	FA	88	EC	123	92
19	B6	54	FB	89	EA	124	8F
20	B9	55	FC	90	E8	125	8C
21	BC	56	FC	91	E6	126	89
22	BF	57	FD	92	E4	127	86
23	C1	58	FE	93	E2	128	83
24	C4	59	FE	94	E0	129	80
25	C7	60	FF	95	DE	130	80
26	C9	61	FF	96	DC	131	7C
27	CC	62	FF	97	DA	132	79
28	CE	63	FF	98	D8	133	73
29	D1	64	FF	99	D5	134	70
30	D3	65	FF	100	D3	135	6D
31	D5	66	FF	101	D1	136	6A
32	D8	67	FF	102	CE	137	67
33	DA	68	FF	103	CC	138	63
34	DC	69	FF	104	C9	139	60
35	DE	70	FF	105	C7	140	5D

No	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
141	5A	176	0A	211	0C	246	5D
142	57	177	09	212	0D	247	60
143	54	178	08	213	0F	248	63
144	51	179	07	214	10	249	67
145	4F	180	06	215	12	250	6A
146	4C	181	05	216	13	251	6D
147	49	182	04	217	15	252	70
148	46	183	03	218	17	253	73
149	43	184	03	219	19	254	76
150	40	185	02	220	1B	255	79
151	3E	186	01	221	1D	256	7C
152	3B	187	00	222	1F		
153	38	188	00	223	21		
154	36	189	00	224	23		
155	33	190	00	225	25		
156	31	191	00	226	27		
157	2E	192	00	227	2A		
158	2C	193	00	228	2C		
159	2A	194	00	229	2E		
160	27	195	00	230	31		
161	25	196	00	231	33		
162	23	197	00	232	36		
163	21	198	00	233	38		
164	1F	199	01	234	3B		
165	1F	200	01	235	3E		
166	1D	201	02	236	40		
167	19	202	03	237	43		
168	17	203	03	238	46		
169	15	204	04	239	49		
170	13	205	05	240	4C		
171	12	206	06	241	4F		
172	10	207	07	242	51		
173	0F	208	08	243	54		
174	0D	209	09	244	57		
175	0C	210	0A	245	5A		

LAMPIRAN D

DATA HASIL PENGAMATAN / PENGUKURAN

Tabel Keluaran 8 bit Alamat Bawah ROM Sinus input 1 modulasi BASK

Step	8 bit Alamat Bawah	Dec
1	0000 0100	4
2	0000 1000	8
3	0000 1100	12
4	0001 0000	16
5	0001 0100	20
6	0001 1000	24
7	0001 1100	28
8	0010 0000	32
9	0010 0100	36
10	0010 1000	40
11	0010 1100	44
12	0011 0000	48
13	0011 0100	52
14	0011 1000	56
15	0011 1100	60
16	0100 0000	64
17	0100 0100	68
18	0100 1000	72
19	0100 1100	76
20	0101 0000	80
21	0101 0100	84
22	0101 1000	88
23	0101 1100	92
24	0110 0000	96
25	0110 0100	100
26	0110 1000	104
27	0110 1100	108
28	0111 0000	112
29	0111 0100	116
30	0111 1000	120
31	0111 1100	124
32	1000 0000	128
33	1000 0100	132
34	1000 1000	136
35	1000 1100	140

Step	8 bit Alamat Bawah	Dec
36	1001 0000	144
37	1001 0100	148
38	1001 1000	152
39	1001 1100	156
40	1010 0000	160
41	1010 0100	164
42	1010 1000	168
43	1010 1100	172
44	1011 0000	176
45	1011 0100	180
46	1011 1000	184
47	1011 1100	188
48	1100 0000	192
49	1100 0100	196
50	1100 1000	200
51	1100 1100	204
52	1101 0000	208
53	1101 0100	212
54	1101 1000	216
55	1101 1100	220
56	1110 0000	224
57	1110 0100	228
58	1110 1000	232
59	1110 1100	236
60	1111 0000	240
61	1111 0100	244
62	1111 1000	248
63	1111 1100	252
64	0000 0000	0
65	0000 0100	4
66	0000 1000	8
67	0000 1100	12
68	0001 0000	16
69	0001 0100	20
70	0001 1000	24

Step	8 bit Alamat Bawah	Dec
71	0001 1100	28
72	0010 0000	32
73	0010 0100	36
74	0010 1000	40
75	0010 1100	44
76	0011 0000	48
77	0011 0100	52
78	0011 1000	56
79	0011 1100	60
80	0100 0000	64
81	0100 0100	68
82	0100 1000	72
83	0100 1100	76
84	0101 0000	80
85	0101 0100	84
86	0101 1000	88
87	0101 1100	92
88	0110 0000	96
89	0110 0100	100
90	0110 1000	104
91	0110 1100	108
92	0111 0000	112
93	0111 0100	116
94	0111 1000	120
95	0111 1100	124
96	1000 0000	128
97	1000 0100	132
98	1000 1000	136
99	1000 1100	140
100	1001 0000	144
101	1001 0100	148
102	1001 1000	152
103	1001 1100	156
104	1010 0000	160
105	1010 0100	164

Step	8 bit Alamat Bawah	Dec
106	1010 1000	168
107	1010 1100	172
108	1011 0000	176
109	1011 0100	180
110	1011 1000	184
111	1011 1100	188
112	1100 0000	192
113	1100 0100	196
114	1100 1000	200
115	1100 1100	204
116	1101 0000	208
117	1101 0100	212
118	1101 1000	216
119	1101 1100	220
120	1110 0000	224
121	1110 0100	228
122	1110 1000	232
123	1110 1100	236
124	1111 0000	240
125	1111 0100	244
126	1111 1000	248
127	1111 1100	252
128	0000 0000	0
129	0000 0100	4
130	0000 1000	8
131	0000 1100	12
132	0001 0000	16
133	0001 0100	20
134	0001 1000	24
135	0001 1100	28
136	0010 0000	32
137	0010 0100	36
138	0010 1000	40
139	0010 1100	44
140	0011 0000	48

Step	8 bit Alamat Bawah	Dec
141	0011 0100	52
142	0011 1000	56
143	0011 1100	60
144	0100 0000	64
145	0100 0100	68
146	0100 1000	72
147	0100 1100	76
148	0101 0000	80
149	0101 0100	84
150	0101 1000	88
151	0101 1100	92
152	0110 0000	96
153	0110 0100	100
154	0110 1000	104
155	0110 1100	108
156	0111 0000	112
157	0111 0100	116
158	0111 1000	120
159	0111 1100	124
160	1000 0000	128
161	1000 0100	132
162	1000 1000	136
163	1000 1100	140
164	1001 0000	144
165	1001 0100	148
166	1001 1000	152
167	1001 1100	156
168	1010 0000	160
169	1010 0100	164
170	1010 1000	168
171	1010 1100	172
172	1011 0000	176
173	1011 0100	180
174	1011 1000	184
175	1011 1100	188

Step	8 bit Alamat Bawah	Dec
176	1100 0000	192
177	1100 0100	196
178	1100 1000	200
179	1100 1100	204
180	1101 0000	208
181	1101 0100	212
182	1101 1000	216
183	1101 1100	220
184	1110 0000	224
185	1110 0100	228
186	1110 1000	232
187	1110 1100	236
188	1111 0000	240
189	1111 0100	244
190	1111 1000	248
191	1111 1100	252
192	0000 0000	0
193	0000 0100	4
194	0000 1000	8
195	0000 1100	12
196	0001 0000	16
197	0001 0100	20
198	0001 1000	24
199	0001 1100	28
200	0010 0000	32
201	0010 0100	36
202	0010 1000	40
203	0010 1100	44
204	0011 0000	48
205	0011 0100	52
206	0011 1000	56
207	0011 1100	60
208	0100 0000	64
209	0100 0100	68
210	0100 1000	72

Step	8 bit Alamat Bawah	Dec
211	0100 1100	76
212	0101 0000	80
213	0101 0100	84
214	0101 1000	88
215	0101 1100	92
216	0110 0000	96
217	0110 0100	100
218	0110 1000	104
219	0110 1100	108
220	0111 0000	112
221	0111 0100	116
222	0111 1000	120
223	0111 1100	124
224	1000 0000	128
225	1000 0100	132
226	1000 1000	136
227	1000 1100	140
228	1001 0000	144
229	1001 0100	148
230	1001 1000	152
231	1001 1100	156
232	1010 0000	160
233	1010 0100	164
234	1010 1000	168
235	1010 1100	172
236	1011 0000	176
237	1011 0100	180
238	1011 1000	184
239	1011 1100	188
240	1100 0000	192
241	1100 0100	196
242	1100 1000	200
243	1100 1100	204
244	1101 0000	208
245	1101 0100	212

Step	8 bit Alamat Bawah	Dec
246	1101 1000	216
247	1101 1100	220
248	1110 0000	224
249	1110 0100	228
250	1110 1000	232
251	1110 1100	236
252	1111 0000	240
253	1111 0100	244
254	1111 1000	248
255	1111 1100	252
256	0000 0000	0

Tabel Keluaran 8 bit Alamat Bawah ROM Sinus input 0 modulasi BASK

Step	8 bit Alamat Bawah	Dec
1	0000 0000	0
2	0000 0000	0
3	0000 0000	0
4	0000 0000	0
5	0000 0000	0
6	0000 0000	0
7	0000 0000	0
8	0000 0000	0
9	0000 0000	0
10	0000 0000	0
11	0000 0000	0
12	0000 0000	0
13	0000 0000	0
14	0000 0000	0
15	0000 0000	0
16	0000 0000	0
17	0000 0000	0
18	0000 0000	0
19	0000 0000	0
20	0000 0000	0
21	0000 0000	0
22	0000 0000	0
23	0000 0000	0
24	0000 0000	0
25	0000 0000	0
26	0000 0000	0
27	0000 0000	0
28	0000 0000	0
29	0000 0000	0
30	0000 0000	0
31	0000 0000	0
32	0000 0000	0
33	0000 0000	0
34	0000 0000	0
35	0000 0000	0

Step	8 bit Alamat Bawah	Dec
36	0000 0000	0
37	0000 0000	0
38	0000 0000	0
39	0000 0000	0
40	0000 0000	0
41	0000 0000	0
42	0000 0000	0
43	0000 0000	0
44	0000 0000	0
45	0000 0000	0
46	0000 0000	0
47	0000 0000	0
48	0000 0000	0
49	0000 0000	0
50	0000 0000	0
51	0000 0000	0
52	0000 0000	0
53	0000 0000	0
54	0000 0000	0
55	0000 0000	0
56	0000 0000	0
57	0000 0000	0
58	0000 0000	0
59	0000 0000	0
60	0000 0000	0
61	0000 0000	0
62	0000 0000	0
63	0000 0000	0
64	0000 0000	0
65	0000 0000	0
66	0000 0000	0
67	0000 0000	0
68	0000 0000	0
69	0000 0000	0
70	0000 0000	0

Step	8 bit Alamat Bawah	Dec
71	0000 0000	0
72	0000 0000	0
73	0000 0000	0
74	0000 0000	0
75	0000 0000	0
76	0000 0000	0
77	0000 0000	0
78	0000 0000	0
79	0000 0000	0
80	0000 0000	0
81	0000 0000	0
82	0000 0000	0
83	0000 0000	0
84	0000 0000	0
85	0000 0000	0
86	0000 0000	0
87	0000 0000	0
88	0000 0000	0
89	0000 0000	0
90	0000 0000	0
91	0000 0000	0
92	0000 0000	0
93	0000 0000	0
94	0000 0000	0
95	0000 0000	0
96	0000 0000	0
97	0000 0000	0
98	0000 0000	0
99	0000 0000	0
100	0000 0000	0
101	0000 0000	0
102	0000 0000	0
103	0000 0000	0
104	0000 0000	0
105	0000 0000	0

Step	8 bit Alamat Bawah	Dec
106	0000 0000	0
107	0000 0000	0
108	0000 0000	0
109	0000 0000	0
110	0000 0000	0
111	0000 0000	0
112	0000 0000	0
113	0000 0000	0
114	0000 0000	0
115	0000 0000	0
116	0000 0000	0
117	0000 0000	0
118	0000 0000	0
119	0000 0000	0
120	0000 0000	0
121	0000 0000	0
122	0000 0000	0
123	0000 0000	0
124	0000 0000	0
125	0000 0000	0
126	0000 0000	0
127	0000 0000	0
128	0000 0000	0
129	0000 0000	0
130	0000 0000	0
131	0000 0000	0
132	0000 0000	0
133	0000 0000	0
134	0000 0000	0
135	0000 0000	0
136	0000 0000	0
137	0000 0000	0
138	0000 0000	0
139	0000 0000	0
140	0000 0000	0

Step	8 bit Alamat Bawah	Dec
141	0000 0000	0
142	0000 0000	0
143	0000 0000	0
144	0000 0000	0
145	0000 0000	0
146	0000 0000	0
147	0000 0000	0
148	0000 0000	0
149	0000 0000	0
150	0000 0000	0
151	0000 0000	0
152	0000 0000	0
153	0000 0000	0
154	0000 0000	0
155	0000 0000	0
156	0000 0000	0
157	0000 0000	0
158	0000 0000	0
159	0000 0000	0
160	0000 0000	0
161	0000 0000	0
162	0000 0000	0
163	0000 0000	0
164	0000 0000	0
165	0000 0000	0
166	0000 0000	0
167	0000 0000	0
168	0000 0000	0
169	0000 0000	0
170	0000 0000	0
171	0000 0000	0
172	0000 0000	0
173	0000 0000	0
174	0000 0000	0
175	0000 0000	0

Step	8 bit Alamat Bawah	Dec
176	0000 0000	0
177	0000 0000	0
178	0000 0000	0
179	0000 0000	0
180	0000 0000	0
181	0000 0000	0
182	0000 0000	0
183	0000 0000	0
184	0000 0000	0
185	0000 0000	0
186	0000 0000	0
187	0000 0000	0
188	0000 0000	0
189	0000 0000	0
190	0000 0000	0
191	0000 0000	0
192	0000 0000	0
193	0000 0000	0
194	0000 0000	0
195	0000 0000	0
196	0000 0000	0
197	0000 0000	0
198	0000 0000	0
199	0000 0000	0
200	0000 0000	0
201	0000 0000	0
202	0000 0000	0
203	0000 0000	0
204	0000 0000	0
205	0000 0000	0
206	0000 0000	0
207	0000 0000	0
208	0000 0000	0
209	0000 0000	0
210	0000 0000	0

Step	8 bit Alamat Bawah	Dec
211	0000 0000	0
212	0000 0000	0
213	0000 0000	0
214	0000 0000	0
215	0000 0000	0
216	0000 0000	0
217	0000 0000	0
218	0000 0000	0
219	0000 0000	0
220	0000 0000	0
221	0000 0000	0
222	0000 0000	0
223	0000 0000	0
224	0000 0000	0
225	0000 0000	0
226	0000 0000	0
227	0000 0000	0
228	0000 0000	0
229	0000 0000	0
230	0000 0000	0
231	0000 0000	0
232	0000 0000	0
233	0000 0000	0
234	0000 0000	0
235	0000 0000	0
236	0000 0000	0
237	0000 0000	0
238	0000 0000	0
239	0000 0000	0
240	0000 0000	0
241	0000 0000	0
242	0000 0000	0
243	0000 0000	0
244	0000 0000	0
245	0000 0000	0

Step	8 bit Alamat Bawah	Dec
246	0000 0000	0
247	0000 0000	0
248	0000 0000	0
249	0000 0000	0
250	0000 0000	0
251	0000 0000	0
252	0000 0000	0
253	0000 0000	0
254	0000 0000	0
255	0000 0000	0
256	0000 0000	0

Tabel Keluaran 8 bit Alamat Bawah ROM Sinus input 1 modulasi BFSK

Step	8 bit Alamat Bawah	Dec
1	0000 0100	4
2	0000 1000	8
3	0000 1100	12
4	0001 0000	16
5	0001 0100	20
6	0001 1000	24
7	0001 1100	28
8	0010 0000	32
9	0010 0100	36
10	0010 1000	40
11	0010 1100	44
12	0011 0000	48
13	0011 0100	52
14	0011 1000	56
15	0011 1100	60
16	0100 0000	64
17	0100 0100	68
18	0100 1000	72
19	0100 1100	76
20	0101 0000	80
21	0101 0100	84
22	0101 1000	88
23	0101 1100	92
24	0110 0000	96
25	0110 0100	100
26	0110 1000	104
27	0110 1100	108
28	0111 0000	112
29	0111 0100	116
30	0111 1000	120
31	0111 1100	124
32	1000 0000	128
33	1000 0100	132
34	1000 1000	136
35	1000 1100	140

Step	8 bit Alamat Bawah	Dec
36	1001 0000	144
37	1001 0100	148
38	1001 1000	152
39	1001 1100	156
40	1010 0000	160
41	1010 0100	164
42	1010 1000	168
43	1010 1100	172
44	1011 0000	176
45	1011 0100	180
46	1011 1000	184
47	1011 1100	188
48	1100 0000	192
49	1100 0100	196
50	1100 1000	200
51	1100 1100	204
52	1101 0000	208
53	1101 0100	212
54	1101 1000	216
55	1101 1100	220
56	1110 0000	224
57	1110 0100	228
58	1110 1000	232
59	1110 1100	236
60	1111 0000	240
61	1111 0100	244
62	1111 1000	248
63	1111 1100	252
64	0000 0000	0
65	0000 0100	4
66	0000 1000	8
67	0000 1100	12
68	0001 0000	16
69	0001 0100	20
70	0001 1000	24

Step	8 bit Alamat Bawah	Dec
71	0001 1100	28
72	0010 0000	32
73	0010 0100	36
74	0010 1000	40
75	0010 1100	44
76	0011 0000	48
77	0011 0100	52
78	0011 1000	56
79	0011 1100	60
80	0100 0000	64
81	0100 0100	68
82	0100 1000	72
83	0100 1100	76
84	0101 0000	80
85	0101 0100	84
86	0101 1000	88
87	0101 1100	92
88	0110 0000	96
89	0110 0100	100
90	0110 1000	104
91	0110 1100	108
92	0111 0000	112
93	0111 0100	116
94	0111 1000	120
95	0111 1100	124
96	1000 0000	128
97	1000 0100	132
98	1000 1000	136
99	1000 1100	140
100	1001 0000	144
101	1001 0100	148
102	1001 1000	152
103	1001 1100	156
104	1010 0000	160
105	1010 0100	164

Step	8 bit Alamat Bawah	Dec
106	1010 1000	168
107	1010 1100	172
108	1011 0000	176
109	1011 0100	180
110	1011 1000	184
111	1011 1100	188
112	1100 0000	192
113	1100 0100	196
114	1100 1000	200
115	1100 1100	204
116	1101 0000	208
117	1101 0100	212
118	1101 1000	216
119	1101 1100	220
120	1110 0000	224
121	1110 0100	228
122	1110 1000	232
123	1110 1100	236
124	1111 0000	240
125	1111 0100	244
126	1111 1000	248
127	1111 1100	252
128	0000 0000	0
129	0000 0100	4
130	0000 1000	8
131	0000 1100	12
132	0001 0000	16
133	0001 0100	20
134	0001 1000	24
135	0001 1100	28
136	0010 0000	32
137	0010 0100	36
138	0010 1000	40
139	0010 1100	44
140	0011 0000	48

Step	8 bit Alamat Bawah	Dec
141	0011 0100	52
142	0011 1000	56
143	0011 1100	60
144	0100 0000	64
145	0100 0100	68
146	0100 1000	72
147	0100 1100	76
148	0101 0000	80
149	0101 0100	84
150	0101 1000	88
151	0101 1100	92
152	0110 0000	96
153	0110 0100	100
154	0110 1000	104
155	0110 1100	108
156	0111 0000	112
157	0111 0100	116
158	0111 1000	120
159	0111 1100	124
160	1000 0000	128
161	1000 0100	132
162	1000 1000	136
163	1000 1100	140
164	1001 0000	144
165	1001 0100	148
166	1001 1000	152
167	1001 1100	156
168	1010 0000	160
169	1010 0100	164
170	1010 1000	168
171	1010 1100	172
172	1011 0000	176
173	1011 0100	180
174	1011 1000	184
175	1011 1100	188

Step	8 bit Alamat Bawah	Dec
176	1100 0000	192
177	1100 0100	196
178	1100 1000	200
179	1100 1100	204
180	1101 0000	208
181	1101 0100	212
182	1101 1000	216
183	1101 1100	220
184	1110 0000	224
185	1110 0100	228
186	1110 1000	232
187	1110 1100	236
188	1111 0000	240
189	1111 0100	244
190	1111 1000	248
191	1111 1100	252
192	0000 0000	0
193	0000 0100	4
194	0000 1000	8
195	0000 1100	12
196	0001 0000	16
197	0001 0100	20
198	0001 1000	24
199	0001 1100	28
200	0010 0000	32
201	0010 0100	36
202	0010 1000	40
203	0010 1100	44
204	0011 0000	48
205	0011 0100	52
206	0011 1000	56
207	0011 1100	60
208	0100 0000	64
209	0100 0100	68
210	0100 1000	72

Step	8 bit Alamat Bawah	Dec
211	0100 1100	76
212	0101 0000	80
213	0101 0100	84
214	0101 1000	88
215	0101 1100	92
216	0110 0000	96
217	0110 0100	100
218	0110 1000	104
219	0110 1100	108
220	0111 0000	112
221	0111 0100	116
222	0111 1000	120
223	0111 1100	124
224	1000 0000	128
225	1000 0100	132
226	1000 1000	136
227	1000 1100	140
228	1001 0000	144
229	1001 0100	148
230	1001 1000	152
231	1001 1100	156
232	1010 0000	160
233	1010 0100	164
234	1010 1000	168
235	1010 1100	172
236	1011 0000	176
237	1011 0100	180
238	1011 1000	184
239	1011 1100	188
240	1100 0000	192
241	1100 0100	196
242	1100 1000	200
243	1100 1100	204
244	1101 0000	208
245	1101 0100	212

Step	8 bit Alamat Bawah	Dec
246	1101 1000	216
247	1101 1100	220
248	1110 0000	224
249	1110 0100	228
250	1110 1000	232
251	1110 1100	236
252	1111 0000	240
253	1111 0100	244
254	1111 1000	248
255	1111 1100	252
256	0000 0000	0

Tabel Keluaran 8 bit Alamat Bawah ROM Sinus input 0 modulasi BFSK

Step	8 bit Alamat Bawah	Dec
1	0000 1000	8
2	0001 0000	16
3	0001 1000	24
4	0010 0000	32
5	0010 1000	40
6	0011 0000	48
7	0011 1000	56
8	0100 0000	64
9	0100 1000	72
10	0101 0000	80
11	0101 1000	88
12	0110 0000	96
13	0110 1000	104
14	0111 0000	112
15	0111 1000	120
16	1000 0000	128
17	1000 1000	136
18	1001 0000	144
19	1001 1000	152
20	1010 0000	160
21	1010 1000	168
22	1011 0000	176
23	1011 1000	184
24	1100 0000	192
25	1100 1000	200
26	1101 0000	208
27	1101 1000	216
28	1110 0000	224
29	1110 1000	232
30	1111 0000	240
31	1111 1000	248
32	0000 0000	0
33	0000 1000	8
34	0001 0000	16
35	0001 1000	24

Step	8 bit Alamat Bawah	Dec
36	0010 0000	32
37	0010 1000	40
38	0011 0000	48
39	0011 1000	56
40	0100 0000	64
41	0100 1000	72
42	0101 0000	80
43	0101 1000	88
44	0110 0000	96
45	0110 1000	104
46	0111 0000	112
47	0111 1000	120
48	1000 0000	128
49	1000 1000	136
50	1001 0000	144
51	1001 1000	152
52	1010 0000	160
53	1010 1000	168
54	1011 0000	176
55	1011 1000	184
56	1100 0000	192
57	1100 1000	200
58	1101 0000	208
59	1101 1000	216
60	1110 0000	224
61	1110 1000	232
62	1111 0000	240
63	1111 1000	248
64	0000 0000	0
65	0000 1000	8
66	0001 0000	16
67	0001 1000	24
68	0010 0000	32
69	0010 1000	40
70	0011 0000	48

Step	8 bit Alamat Bawah	Dec
71	0011 1000	56
72	0100 0000	64
73	0100 1000	72
74	0101 0000	80
75	0101 1000	88
76	0110 0000	96
77	0110 1000	104
78	0111 0000	112
79	0111 1000	120
80	1000 0000	128
81	1000 1000	136
82	1001 0000	144
83	1001 1000	152
84	1010 0000	160
85	1010 1000	168
86	1011 0000	176
87	1011 1000	184
88	1100 0000	192
89	1100 1000	200
90	1101 0000	208
91	1101 1000	216
92	1110 0000	224
93	1110 1000	232
94	1111 0000	240
95	1111 1000	248
96	0000 0000	0
97	0000 1000	8
98	0001 0000	16
99	0001 1000	24
100	0010 0000	32
101	0010 1000	40
102	0011 0000	48
103	0011 1000	56
104	0100 0000	64
105	0100 1000	72

Step	8 bit Alamat Bawah	Dec
106	0101 0000	80
107	0101 1000	88
108	0110 0000	96
109	0110 1000	104
110	0111 0000	112
111	0111 1000	120
112	1000 0000	128
113	1000 1000	136
114	1001 0000	144
115	1001 1000	152
116	1010 0000	160
117	1010 1000	168
118	1011 0000	176
119	1011 1000	184
120	1100 0000	192
121	1100 1000	200
122	1101 0000	208
123	1101 1000	216
124	1110 0000	224
125	1110 1000	232
126	1111 0000	240
127	1111 1000	248
128	0000 0000	0
129	0000 1000	8
130	0001 0000	16
131	0001 1000	24
132	0010 0000	32
133	0010 1000	40
134	0011 0000	48
135	0011 1000	56
136	0100 0000	64
137	0100 1000	72
138	0101 0000	80
139	0101 1000	88
140	0110 0000	96

Step	8 bit Alamat Bawah	Dec
141	0110 1000	104
142	0111 0000	112
143	0111 1000	120
144	1000 0000	128
145	1000 1000	136
146	1001 0000	144
147	1001 1000	152
148	1010 0000	160
149	1010 1000	168
150	1011 0000	176
151	1011 1000	184
152	1100 0000	192
153	1100 1000	200
154	1101 0000	208
155	1101 1000	216
156	1110 0000	224
157	1110 1000	232
158	1111 0000	240
159	1111 1000	248
160	0000 0000	0
161	0000 1000	8
162	0001 0000	16
163	0001 1000	24
164	0010 0000	32
165	0010 1000	40
166	0011 0000	48
167	0011 1000	56
168	0100 0000	64
169	0100 1000	72
170	0101 0000	80
171	0101 1000	88
172	0110 0000	96
173	0110 1000	104
174	0111 0000	112
175	0111 1000	120

Step	8 bit Alamat Bawah	Dec
176	1000 0000	128
177	1000 1000	136
178	1001 0000	144
179	1001 1000	152
180	1010 0000	160
181	1010 1000	168
182	1011 0000	176
183	1011 1000	184
184	1100 0000	192
185	1100 1000	200
186	1101 0000	208
187	1101 1000	216
188	1110 0000	224
189	1110 1000	232
190	1111 0000	240
191	1111 1000	248
192	0000 0000	0
193	0000 1000	8
194	0001 0000	16
195	0001 1000	24
196	0010 0000	32
197	0010 1000	40
198	0011 0000	48
199	0011 1000	56
200	0100 0000	64
201	0100 1000	72
202	0101 0000	80
203	0101 1000	88
204	0110 0000	96
205	0110 1000	104
206	0111 0000	112
207	0111 1000	120
208	1000 0000	128
209	1000 1000	136
210	1001 0000	144

Step	8 bit Alamat Bawah	Dec
211	1001 1000	152
212	1010 0000	160
213	1010 1000	168
214	1011 0000	176
215	1011 1000	184
216	1100 0000	192
217	1100 1000	200
218	1101 0000	208
219	1101 1000	216
220	1110 0000	224
221	1110 1000	232
222	1111 0000	240
223	1111 1000	248
224	0000 0000	0
225	0000 1000	8
226	0001 0000	16
227	0001 1000	24
228	0010 0000	32
229	0010 1000	40
230	0011 0000	48
231	0011 1000	56
232	0100 0000	64
233	0100 1000	72
234	0101 0000	80
235	0101 1000	88
236	0110 0000	96
237	0110 1000	104
238	0111 0000	112
239	0111 1000	120
240	1000 0000	128
241	1000 1000	136
242	1001 0000	144
243	1001 1000	152
244	1010 0000	160
245	1010 1000	168

Step	8 bit Alamat Bawah	Dec
246	1011 0000	176
247	1011 1000	184
248	1100 0000	192
249	1100 1000	200
250	1101 0000	208
251	1101 1000	216
252	1110 0000	224
253	1110 1000	232
254	1111 0000	240
255	1111 1000	248
256	0000 0000	0

Tabel Keluaran 8 bit Alamat Bawah ROM Sinus input 1 modulasi BPSK

Step	8 bit Alamat Bawah	Dec
1	0000 0100	4
2	0000 1000	8
3	0000 1100	12
4	0001 0000	16
5	0001 0100	20
6	0001 1000	24
7	0001 1100	28
8	0010 0000	32
9	0010 0100	36
10	0010 1000	40
11	0010 1100	44
12	0011 0000	48
13	0011 0100	52
14	0011 1000	56
15	0011 1100	60
16	0100 0000	64
17	0100 0100	68
18	0100 1000	72
19	0100 1100	76
20	0101 0000	80
21	0101 0100	84
22	0101 1000	88
23	0101 1100	92
24	0110 0000	96
25	0110 0100	100
26	0110 1000	104
27	0110 1100	108
28	0111 0000	112
29	0111 0100	116
30	0111 1000	120
31	0111 1100	124
32	1000 0000	128
33	1000 0100	132
34	1000 1000	136
35	1000 1100	140

Step	8 bit Alamat Bawah	Dec
36	1001 0000	144
37	1001 0100	148
38	1001 1000	152
39	1001 1100	156
40	1010 0000	160
41	1010 0100	164
42	1010 1000	168
43	1010 1100	172
44	1011 0000	176
45	1011 0100	180
46	1011 1000	184
47	1011 1100	188
48	1100 0000	192
49	1100 0100	196
50	1100 1000	200
51	1100 1100	204
52	1101 0000	208
53	1101 0100	212
54	1101 1000	216
55	1101 1100	220
56	1110 0000	224
57	1110 0100	228
58	1110 1000	232
59	1110 1100	236
60	1111 0000	240
61	1111 0100	244
62	1111 1000	248
63	1111 1100	252
64	0000 0000	0
65	0000 0100	4
66	0000 1000	8
67	0000 1100	12
68	0001 0000	16
69	0001 0100	20
70	0001 1000	24

Step	8 bit Alamat Bawah	Dec
71	0001 1100	28
72	0010 0000	32
73	0010 0100	36
74	0010 1000	40
75	0010 1100	44
76	0011 0000	48
77	0011 0100	52
78	0011 1000	56
79	0011 1100	60
80	0100 0000	64
81	0100 0100	68
82	0100 1000	72
83	0100 1100	76
84	0101 0000	80
85	0101 0100	84
86	0101 1000	88
87	0101 1100	92
88	0110 0000	96
89	0110 0100	100
90	0110 1000	104
91	0110 1100	108
92	0111 0000	112
93	0111 0100	116
94	0111 1000	120
95	0111 1100	124
96	1000 0000	128
97	1000 0100	132
98	1000 1000	136
99	1000 1100	140
100	1001 0000	144
101	1001 0100	148
102	1001 1000	152
103	1001 1100	156
104	1010 0000	160
105	1010 0100	164

Step	8 bit Alamat Bawah	Dec
106	1010 1000	168
107	1010 1100	172
108	1011 0000	176
109	1011 0100	180
110	1011 1000	184
111	1011 1100	188
112	1100 0000	192
113	1100 0100	196
114	1100 1000	200
115	1100 1100	204
116	1101 0000	208
117	1101 0100	212
118	1101 1000	216
119	1101 1100	220
120	1110 0000	224
121	1110 0100	228
122	1110 1000	232
123	1110 1100	236
124	1111 0000	240
125	1111 0100	244
126	1111 1000	248
127	1111 1100	252
128	0000 0000	0
129	0000 0100	4
130	0000 1000	8
131	0000 1100	12
132	0001 0000	16
133	0001 0100	20
134	0001 1000	24
135	0001 1100	28
136	0010 0000	32
137	0010 0100	36
138	0010 1000	40
139	0010 1100	44
140	0011 0000	48

Step	8 bit Alamat Bawah	Dec
141	0011 0100	52
142	0011 1000	56
143	0011 1100	60
144	0100 0000	64
145	0100 0100	68
146	0100 1000	72
147	0100 1100	76
148	0101 0000	80
149	0101 0100	84
150	0101 1000	88
151	0101 1100	92
152	0110 0000	96
153	0110 0100	100
154	0110 1000	104
155	0110 1100	108
156	0111 0000	112
157	0111 0100	116
158	0111 1000	120
159	0111 1100	124
160	1000 0000	128
161	1000 0100	132
162	1000 1000	136
163	1000 1100	140
164	1001 0000	144
165	1001 0100	148
166	1001 1000	152
167	1001 1100	156
168	1010 0000	160
169	1010 0100	164
170	1010 1000	168
171	1010 1100	172
172	1011 0000	176
173	1011 0100	180
174	1011 1000	184
175	1011 1100	188

Step	8 bit Alamat Bawah	Dec
176	1100 0000	192
177	1100 0100	196
178	1100 1000	200
179	1100 1100	204
180	1101 0000	208
181	1101 0100	212
182	1101 1000	216
183	1101 1100	220
184	1110 0000	224
185	1110 0100	228
186	1110 1000	232
187	1110 1100	236
188	1111 0000	240
189	1111 0100	244
190	1111 1000	248
191	1111 1100	252
192	0000 0000	0
193	0000 0100	4
194	0000 1000	8
195	0000 1100	12
196	0001 0000	16
197	0001 0100	20
198	0001 1000	24
199	0001 1100	28
200	0010 0000	32
201	0010 0100	36
202	0010 1000	40
203	0010 1100	44
204	0011 0000	48
205	0011 0100	52
206	0011 1000	56
207	0011 1100	60
208	0100 0000	64
209	0100 0100	68
210	0100 1000	72

Step	8 bit Alamat Bawah	Dec
211	0100 1100	76
212	0101 0000	80
213	0101 0100	84
214	0101 1000	88
215	0101 1100	92
216	0110 0000	96
217	0110 0100	100
218	0110 1000	104
219	0110 1100	108
220	0111 0000	112
221	0111 0100	116
222	0111 1000	120
223	0111 1100	124
224	1000 0000	128
225	1000 0100	132
226	1000 1000	136
227	1000 1100	140
228	1001 0000	144
229	1001 0100	148
230	1001 1000	152
231	1001 1100	156
232	1010 0000	160
233	1010 0100	164
234	1010 1000	168
235	1010 1100	172
236	1011 0000	176
237	1011 0100	180
238	1011 1000	184
239	1011 1100	188
240	1100 0000	192
241	1100 0100	196
242	1100 1000	200
243	1100 1100	204
244	1101 0000	208
245	1101 0100	212

Step	8 bit Alamat Bawah	Dec
246	1101 1000	216
247	1101 1100	220
248	1110 0000	224
249	1110 0100	228
250	1110 1000	232
251	1110 1100	236
252	1111 0000	240
253	1111 0100	244
254	1111 1000	248
255	1111 1100	252
256	0000 0000	0

Tabel Keluaran 8 bit Alamat Bawah ROM Sinus input 0 modulasi BPSK

Step	8 bit Alamat Bawah	Dec
1	1111 1100	252
2	1111 1000	248
3	1111 0100	244
4	1111 0000	240
5	1110 1100	236
6	1110 1000	232
7	1110 0100	228
8	1110 0000	224
9	1101 1100	220
10	1101 1000	216
11	1101 0100	212
12	1101 0000	208
13	1100 1100	204
14	1100 1000	200
15	1100 0100	196
16	1100 0000	192
17	1011 1100	188
18	1011 1000	184
19	1011 0100	180
20	1011 0000	176
21	1010 1100	172
22	1010 1000	168
23	1010 0100	164
24	1010 0000	160
25	1001 1100	156
26	1001 1000	152
27	1001 0100	148
28	1001 0000	144
29	1000 1100	140
30	1000 1000	136
31	1000 0100	132
32	1000 0000	128
33	0111 1100	124
34	0111 1000	120
35	0111 0100	116

Step	8 bit Alamat Bawah	Dec
36	0111 0000	112
37	0110 1100	108
38	0110 1000	104
39	0110 0100	100
40	0110 0000	96
41	0101 1100	92
42	0101 1000	88
43	0101 0100	84
44	0101 0000	80
45	0100 1100	76
46	0100 1000	72
47	0100 0100	68
48	0100 0000	64
49	0011 1100	60
50	0011 1000	56
51	0011 0100	52
52	0011 0000	48
53	0010 1100	44
54	0010 1000	40
55	0010 0100	36
56	0010 0000	32
57	0001 1100	28
58	0001 1000	24
59	0001 0100	20
60	0001 0000	16
61	0000 1100	12
62	0000 1000	8
63	0000 0100	4
64	0000 0000	0
65	1111 1100	252
66	1111 1000	248
67	1111 0100	244
68	1111 0000	240
69	1110 1100	236
70	1110 1000	232

Step	8 bit Alamat Bawah	Dec
71	1110 0100	228
72	1110 0000	224
73	1101 1100	220
74	1101 1000	216
75	1101 0100	212
76	1101 0000	208
77	1100 1100	204
78	1100 1000	200
79	1100 0100	196
80	1100 0000	192
81	1011 1100	188
82	1011 1000	184
83	1011 0100	180
84	1011 0000	176
85	1010 1100	172
86	1010 1000	168
87	1010 0100	164
88	1010 0000	160
89	1001 1100	156
90	1001 1000	152
91	1001 0100	148
92	1001 0000	144
93	1000 1100	140
94	1000 1000	136
95	1000 0100	132
96	1000 0000	128
97	0111 1100	124
98	0111 1000	120
99	0111 0100	116
100	0111 0000	112
101	0110 1100	108
102	0110 1000	104
103	0110 0100	100
104	0110 0000	96
105	0101 1100	92

Step	8 bit Alamat Bawah	Dec
106	0101 1000	88
107	0101 0100	84
108	0101 0000	80
109	0100 1100	76
110	0100 1000	72
111	0100 0100	68
112	0100 0000	64
113	0011 1100	60
114	0011 1000	56
115	0011 0100	52
116	0011 0000	48
117	0010 1100	44
118	0010 1000	40
119	0010 0100	36
120	0010 0000	32
121	0001 1100	28
122	0001 1000	24
123	0001 0100	20
124	0001 0000	16
125	0000 1100	12
126	0000 1000	8
127	0000 0100	4
128	0000 0000	0
129	1111 1100	252
130	1111 1000	248
131	1111 0100	244
132	1111 0000	240
133	1110 1100	236
134	1110 1000	232
135	1110 0100	228
136	1110 0000	224
137	1101 1100	220
138	1101 1000	216
139	1101 0100	212
140	1101 0000	208

Step	8 bit Alamat Bawah	Dec
141	1100 1100	204
142	1100 1000	200
143	1100 0100	196
144	1100 0000	192
145	1011 1100	188
146	1011 1000	184
147	1011 0100	180
148	1011 0000	176
149	1010 1100	172
150	1010 1000	168
151	1010 0100	164
152	1010 0000	160
153	1001 1100	156
154	1001 1000	152
155	1001 0100	148
156	1001 0000	144
157	1000 1100	140
158	1000 1000	136
159	1000 0100	132
160	1000 0000	128
161	0111 1100	124
162	0111 1000	120
163	0111 0100	116
164	0111 0000	112
165	0110 1100	108
166	0110 1000	104
167	0110 0100	100
168	0110 0000	96
169	0101 1100	92
170	0101 1000	88
171	0101 0100	84
172	0101 0000	80
173	0100 1100	76
174	0100 1000	72
175	0100 0100	68

Step	8 bit Alamat Bawah	Dec
176	0100 0000	64
177	0011 1100	60
178	0011 1000	56
179	0011 0100	52
180	0011 0000	48
181	0010 1100	44
182	0010 1000	40
183	0010 0100	36
184	0010 0000	32
185	0001 1100	28
186	0001 1000	24
187	0001 0100	20
188	0001 0000	16
189	0000 1100	12
190	0000 1000	8
191	0000 0100	4
192	0000 0000	0
193	1111 1100	252
194	1111 1000	248
195	1111 0100	244
196	1111 0000	240
197	1110 1100	236
198	1110 1000	232
199	1110 0100	228
200	1110 0000	224
201	1101 1100	220
202	1101 1000	216
203	1101 0100	212
204	1101 0000	208
205	1100 1100	204
206	1100 1000	200
207	1100 0100	196
208	1100 0000	192
209	1011 1100	188
210	1011 1000	184

Step	8 bit Alamat Bawah	Dec
211	1011 0100	180
212	1011 0000	176
213	1010 1100	172
214	1010 1000	168
215	1010 0100	164
216	1010 0000	160
217	1001 1100	156
218	1001 1000	152
219	1001 0100	148
220	1001 0000	144
221	1000 1100	140
222	1000 1000	136
223	1000 0100	132
224	1000 0000	128
225	0111 1100	124
226	0111 1000	120
227	0111 0100	116
228	0111 0000	112
229	0110 1100	108
230	0110 1000	104
231	0110 0100	100
232	0110 0000	96
233	0101 1100	92
234	0101 1000	88
235	0101 0100	84
236	0101 0000	80
237	0100 1100	76
238	0100 1000	72
239	0100 0100	68
240	0100 0000	64
241	0011 1100	60
242	0011 1000	56
243	0011 0100	52
244	0011 0000	48
245	0010 1100	44

Step	8 bit Alamat Bawah	Dec
246	0010 1000	40
247	0010 0100	36
248	0010 0000	32
249	0001 1100	28
250	0001 1000	24
251	0001 0100	20
252	0001 0000	16
253	0000 1100	12
254	0000 1000	8
255	0000 0100	4
256	0000 0000	0

Tabel Keluaran ROM Sinus untuk input bit 1 modulasi BASK

Step	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
1	8C	36	4F	71	D1	106	15
2	98	37	43	72	DA	107	0F
3	A5	38	38	73	E2	108	9
4	B0	39	2E	74	EA	109	5
5	BC	40	25	75	F0	110	2
6	C7	41	1F	76	F6	111	0
7	D1	42	15	77	FA	112	0
8	DA	43	0F	78	FD	113	0
9	E2	44	9	79	FF	114	2
10	EA	45	5	80	FF	115	5
11	F0	46	2	81	FF	116	9
12	F6	47	0	82	FD	117	0F
13	FA	48	0	83	FA	118	15
14	FD	49	0	84	F6	119	1D
15	FF	50	2	85	F0	120	25
16	FF	51	5	86	EA	121	2E
17	FF	52	9	87	E2	122	38
18	FD	53	0F	88	DA	123	43
19	FA	54	15	89	D1	124	4F
20	F6	55	1D	90	C7	125	5A
21	F0	56	25	91	BC	126	67
22	EA	57	2E	92	B0	127	73
23	E2	58	38	93	A5	128	80
24	DA	59	43	94	98	129	8C
25	D1	60	4F	95	8C	130	98
26	C7	61	5A	96	80	131	A5
27	BC	62	67	97	73	132	B0
28	B0	63	73	98	67	133	BC
29	A5	64	80	99	5A	134	C7
30	98	65	8C	100	4F	135	D1
31	8C	66	98	101	43	136	DA
32	80	67	A5	102	38	137	E2
33	73	68	B0	103	2E	138	EA
34	67	69	BC	104	25	139	F0
35	5A	70	C7	105	1F	140	F6

No	Data (Hex)
141	FA
142	FD
143	FF
144	FF
145	FF
146	FD
147	FA
148	F6
149	F0
150	EA
151	E2
152	DA
153	D1
154	C7
155	BC
156	B0
157	A5
158	98
159	8C
160	80
161	73
162	67
163	5A
164	4F
165	43
166	38
167	2E
168	25
169	1F
170	15
171	0F
172	9
173	5
174	2
175	0

No	Data (Hex)
176	0
177	0
178	2
179	5
180	9
181	0F
182	15
183	1D
184	25
185	2E
186	38
187	43
188	4F
189	5A
190	67
191	73
192	80
193	8C
194	98
195	A5
196	B0
197	BC
198	C7
199	D1
200	DA
201	E2
202	EA
203	F0
204	F6
205	FA
206	FD
207	FF
208	FF
209	FF
210	FD

No	Data (Hex)
211	FA
212	F6
213	F0
214	EA
215	E2
216	DA
217	D1
218	C7
219	BC
220	B0
221	A5
222	98
223	8C
224	80
225	73
226	67
227	5A
228	4F
229	43
230	38
231	2E
232	25
233	1F
234	15
235	0F
236	9
237	5
238	2
239	0
240	0
241	0
242	2
243	5
244	9
245	0F

No	Data (Hex)
246	15
247	1D
248	25
249	2E
250	38
251	43
252	4F
253	5A
254	67
255	73
256	80

Tabel Keluaran ROM Sinus untuk input bit 0 modulasi BASK

Step	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
1	87	36	87	71	87	106	87
2	87	37	87	72	87	107	87
3	87	38	87	73	87	108	87
4	87	39	87	74	87	109	87
5	87	40	87	75	87	110	87
6	87	41	87	76	87	111	87
7	87	42	87	77	87	112	87
8	87	43	87	78	87	113	87
9	87	44	87	79	87	114	87
10	87	45	87	80	87	115	87
11	87	46	87	81	87	116	87
12	87	47	87	82	87	117	87
13	87	48	87	83	87	118	87
14	87	49	87	84	87	119	87
15	87	50	87	85	87	120	87
16	87	51	87	86	87	121	87
17	87	52	87	87	87	122	87
18	87	53	87	88	87	123	87
19	87	54	87	89	87	124	87
20	87	55	87	90	87	125	87
21	87	56	87	91	87	126	87
22	87	57	87	92	87	127	87
23	87	58	87	93	87	128	87
24	87	59	87	94	87	129	87
25	87	60	87	95	87	130	87
26	87	61	87	96	87	131	87
27	87	62	87	97	87	132	87
28	87	63	87	98	87	133	87
29	87	64	87	99	87	134	87
30	87	65	87	100	87	135	87
31	87	66	87	101	87	136	87
32	87	67	87	102	87	137	87
33	87	68	87	103	87	138	87
34	87	69	87	104	87	139	87
35	87	70	87	105	87	140	87

No	Data (Hex)
141	87
142	87
143	87
144	87
145	87
146	87
147	87
148	87
149	87
150	87
151	87
152	87
153	87
154	87
155	87
156	87
157	87
158	87
159	87
160	87
161	87
162	87
163	87
164	87
165	87
166	87
167	87
168	87
169	87
170	87
171	87
172	87
173	87
174	87
175	87

No	Data (Hex)
176	87
177	87
178	87
179	87
180	87
181	87
182	87
183	87
184	87
185	87
186	87
187	87
188	87
189	87
190	87
191	87
192	87
193	87
194	87
195	87
196	87
197	87
198	87
199	87
200	87
201	87
202	87
203	87
204	87
205	87
206	87
207	87
208	87
209	87
210	87

No	Data (Hex)
211	87
212	87
213	87
214	87
215	87
216	87
217	87
218	87
219	87
220	87
221	87
222	87
223	87
224	87
225	87
226	87
227	87
228	87
229	87
230	87
231	87
232	87
233	87
234	87
235	87
236	87
237	87
238	87
239	87
240	87
241	87
242	87
243	87
244	87
245	87

No	Data (Hex)
246	87
247	87
248	87
249	87
250	87
251	87
252	87
253	87
254	87
255	87
256	87

Tabel Keluaran ROM Sinus untuk input bit 1 modulasi BFSK

Step	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
1	8C	36	4F	71	D1	106	15
2	98	37	43	72	DA	107	0F
3	A5	38	38	73	E2	108	9
4	B0	39	2E	74	EA	109	5
5	BC	40	25	75	F0	110	2
6	C7	41	1F	76	F6	111	0
7	D1	42	15	77	FA	112	0
8	DA	43	0F	78	FD	113	0
9	E2	44	9	79	FF	114	2
10	EA	45	5	80	FF	115	5
11	F0	46	2	81	FF	116	9
12	F6	47	0	82	FD	117	0F
13	FA	48	0	83	FA	118	15
14	FD	49	0	84	F6	119	1D
15	FF	50	2	85	F0	120	25
16	FF	51	5	86	EA	121	2E
17	FF	52	9	87	E2	122	38
18	FD	53	0F	88	DA	123	43
19	FA	54	15	89	D1	124	4F
20	F6	55	1D	90	C7	125	5A
21	F0	56	25	91	BC	126	67
22	EA	57	2E	92	B0	127	73
23	E2	58	38	93	A5	128	80
24	DA	59	43	94	98	129	8C
25	D1	60	4F	95	8C	130	98
26	C7	61	5A	96	80	131	A5
27	BC	62	67	97	73	132	B0
28	B0	63	73	98	67	133	BC
29	A5	64	80	99	5A	134	C7
30	98	65	8C	100	4F	135	D1
31	8C	66	98	101	43	136	DA
32	80	67	A5	102	38	137	E2
33	73	68	B0	103	2E	138	EA
34	67	69	BC	104	25	139	F0
35	5A	70	C7	105	1F	140	F6

No	Data (Hex)
141	FA
142	FD
143	FF
144	FF
145	FF
146	FD
147	FA
148	F6
149	F0
150	EA
151	E2
152	DA
153	D1
154	C7
155	BC
156	B0
157	A5
158	98
159	8C
160	80
161	73
162	67
163	5A
164	4F
165	43
166	38
167	2E
168	25
169	1F
170	15
171	0F
172	9
173	5
174	2
175	0

No	Data (Hex)
176	0
177	0
178	2
179	5
180	9
181	0F
182	15
183	1D
184	25
185	2E
186	38
187	43
188	4F
189	5A
190	67
191	73
192	80
193	8C
194	98
195	A5
196	B0
197	BC
198	C7
199	D1
200	DA
201	E2
202	EA
203	F0
204	F6
205	FA
206	FD
207	FF
208	FF
209	FF
210	FD

No	Data (Hex)
211	FA
212	F6
213	F0
214	EA
215	E2
216	DA
217	D1
218	C7
219	BC
220	B0
221	A5
222	98
223	8C
224	80
225	73
226	67
227	5A
228	4F
229	43
230	38
231	2E
232	25
233	1F
234	15
235	0F
236	9
237	5
238	2
239	0
240	0
241	0
242	2
243	5
244	9
245	0F

No	Data (Hex)
246	15
247	1D
248	25
249	2E
250	38
251	43
252	4F
253	5A
254	67
255	73
256	80

Tabel Keluaran ROM Sinus untuk input bit 0 modulasi BFSK

Step	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
1	98	36	DA	71	FD	106	F6
2	B0	37	EA	72	FF	107	EA
3	C7	38	F6	73	FD	108	DA
4	DA	39	FD	74	F6	109	C7
5	EA	40	FF	75	EA	110	B0
6	F6	41	FD	76	DA	111	98
7	FD	42	F6	77	C7	112	80
8	FF	43	EA	78	B0	113	67
9	FD	44	DA	79	98	114	4F
10	F6	45	C7	80	80	115	38
11	EA	46	B0	81	67	116	25
12	DA	47	98	82	4F	117	15
13	C7	48	80	83	38	118	9
14	B0	49	67	84	25	119	2
15	98	50	4F	85	15	120	0
16	80	51	38	86	9	121	2
17	67	52	25	87	2	122	9
18	4F	53	15	88	0	123	15
19	38	54	9	89	2	124	25
20	25	55	2	90	9	125	38
21	15	56	0	91	15	126	4F
22	9	57	2	92	25	127	67
23	2	58	9	93	38	128	80
24	0	59	15	94	4F	129	98
25	2	60	25	95	67	130	B0
26	9	61	38	96	80	131	C7
27	15	62	4F	97	98	132	DA
28	25	63	67	98	B0	133	EA
29	38	64	80	99	C7	134	F6
30	4F	65	98	100	DA	135	FD
31	67	66	B0	101	EA	136	FF
32	80	67	C7	102	F6	137	FD
33	98	68	DA	103	FD	138	F6
34	B0	69	EA	104	FF	139	EA
35	C7	70	F6	105	FD	140	DA

No	Data (Hex)
141	C7
142	B0
143	98
144	80
145	67
146	4F
147	38
148	25
149	15
150	9
151	2
152	0
153	2
154	9
155	15
156	25
157	38
158	4F
159	67
160	80
161	98
162	B0
163	C7
164	DA
165	EA
166	F6
167	FD
168	FF
169	FD
170	F6
171	EA
172	DA
173	C7
174	B0
175	98

No	Data (Hex)
176	80
177	67
178	4F
179	38
180	25
181	15
182	9
183	2
184	0
185	2
186	9
187	15
188	25
189	38
190	4F
191	67
192	80
193	98
194	B0
195	C7
196	DA
197	EA
198	F6
199	FD
200	FF
201	FD
202	F6
203	EA
204	DA
205	C7
206	B0
207	98
208	80
209	67
210	4F

No	Data (Hex)
211	38
212	25
213	15
214	9
215	2
216	0
217	2
218	9
219	15
220	25
221	38
222	4F
223	67
224	80
225	98
226	B0
227	C7
228	DA
229	EA
230	F6
231	FD
232	FF
233	FD
234	F6
235	EA
236	DA
237	C7
238	B0
239	98
240	80
241	67
242	4F
243	38
244	25
245	15

No	Data (Hex)
246	9
247	2
248	0
249	2
250	9
251	15
252	25
253	38
254	4F
255	67
256	80

Tabel Keluaran ROM Sinus untuk input bit 1 modulasi BPSK

Step	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
1	8C	36	4F	71	D1	106	15
2	98	37	43	72	DA	107	0F
3	A5	38	38	73	E2	108	9
4	B0	39	2E	74	EA	109	5
5	BC	40	25	75	F0	110	2
6	C7	41	1F	76	F6	111	0
7	D1	42	15	77	FA	112	0
8	DA	43	0F	78	FD	113	0
9	E2	44	9	79	FF	114	2
10	EA	45	5	80	FF	115	5
11	F0	46	2	81	FF	116	9
12	F6	47	0	82	FD	117	0F
13	FA	48	0	83	FA	118	15
14	FD	49	0	84	F6	119	1D
15	FF	50	2	85	F0	120	25
16	FF	51	5	86	EA	121	2E
17	FF	52	9	87	E2	122	38
18	FD	53	0F	88	DA	123	43
19	FA	54	15	89	D1	124	4F
20	F6	55	1D	90	C7	125	5A
21	F0	56	25	91	BC	126	67
22	EA	57	2E	92	B0	127	73
23	E2	58	38	93	A5	128	80
24	DA	59	43	94	98	129	8C
25	D1	60	4F	95	8C	130	98
26	C7	61	5A	96	80	131	A5
27	BC	62	67	97	73	132	B0
28	B0	63	73	98	67	133	BC
29	A5	64	80	99	5A	134	C7
30	98	65	8C	100	4F	135	D1
31	8C	66	98	101	43	136	DA
32	80	67	A5	102	38	137	E2
33	73	68	B0	103	2E	138	EA
34	67	69	BC	104	25	139	F0
35	5A	70	C7	105	1F	140	F6

No	Data (Hex)
141	FA
142	FD
143	FF
144	FF
145	FF
146	FD
147	FA
148	F6
149	F0
150	EA
151	E2
152	DA
153	D1
154	C7
155	BC
156	B0
157	A5
158	98
159	8C
160	80
161	73
162	67
163	5A
164	4F
165	43
166	38
167	2E
168	25
169	1F
170	15
171	0F
172	9
173	5
174	2
175	0

No	Data (Hex)
176	0
177	0
178	2
179	5
180	9
181	0F
182	15
183	1D
184	25
185	2E
186	38
187	43
188	4F
189	5A
190	67
191	73
192	80
193	8C
194	98
195	A5
196	B0
197	BC
198	C7
199	D1
200	DA
201	E2
202	EA
203	F0
204	F6
205	FA
206	FD
207	FF
208	FF
209	FF
210	FD

No	Data (Hex)
211	FA
212	F6
213	F0
214	EA
215	E2
216	DA
217	D1
218	C7
219	BC
220	B0
221	A5
222	98
223	8C
224	80
225	73
226	67
227	5A
228	4F
229	43
230	38
231	2E
232	25
233	1F
234	15
235	0F
236	9
237	5
238	2
239	0
240	0
241	0
242	2
243	5
244	9
245	0F

No	Data (Hex)
246	15
247	1D
248	25
249	2E
250	38
251	43
252	4F
253	5A
254	67
255	73
256	80

Tabel Keluaran ROM Sinus untuk input bit 0 modulasi BPSK

Step	Data (Hex)	No	Data (Hex)	No	Data (Hex)	No	Data (Hex)
1	73	36	B0	71	2E	106	EA
2	67	37	BC	72	25	107	F0
3	5A	38	C7	73	1D	108	F6
4	4F	39	D1	74	15	109	FA
5	43	40	DA	75	0F	110	FD
6	38	41	E2	76	9	111	FF
7	2E	42	EA	77	5	112	FF
8	25	43	F0	78	2	113	FF
9	1D	44	F6	79	0	114	FD
10	15	45	FA	80	0	115	FA
11	0F	46	FD	81	0	116	F6
12	9	47	FF	82	2	117	F0
13	5	48	FF	83	5	118	EA
14	2	49	FF	84	9	119	E2
15	0	50	FD	85	0F	120	DA
16	0	51	FA	86	15	121	D1
17	0	52	F6	87	1F	122	C7
18	2	53	F0	88	25	123	BC
19	5	54	EA	89	2E	124	B0
20	9	55	E2	90	38	125	A5
21	0F	56	DA	91	43	126	98
22	15	57	D1	92	4F	127	8C
23	1F	58	C7	93	5A	128	80
24	25	59	BC	94	67	129	73
25	2E	60	B0	95	73	130	67
26	38	61	A5	96	80	131	5A
27	43	62	98	97	8C	132	4F
28	4F	63	8C	98	98	133	43
29	5A	64	80	99	A5	134	38
30	67	65	73	100	B0	135	2E
31	73	66	67	101	BC	136	25
32	80	67	5A	102	C7	137	1D
33	8C	68	4F	103	D1	138	15
34	98	69	43	104	DA	139	0F
35	A5	70	38	105	E2	140	9

No	Data (Hex)
141	5
142	2
143	0
144	0
145	0
146	2
147	5
148	9
149	0F
150	15
151	1F
152	25
153	2E
154	38
155	43
156	4F
157	5A
158	67
159	73
160	80
161	8C
162	98
163	A5
164	B0
165	BC
166	C7
167	D1
168	DA
169	E2
170	EA
171	F0
172	F6
173	FA
174	FD
175	FF

No	Data (Hex)
176	FF
177	FF
178	FD
179	FA
180	F6
181	F0
182	EA
183	E2
184	DA
185	D1
186	C7
187	BC
188	B0
189	A5
190	98
191	8C
192	80
193	73
194	67
195	5A
196	4F
197	43
198	38
199	2E
200	25
201	1D
202	15
203	0F
204	9
205	5
206	2
207	0
208	0
209	0
210	2

No	Data (Hex)
211	5
212	9
213	0F
214	15
215	1F
216	25
217	2E
218	38
219	43
220	4F
221	5A
222	67
223	73
224	80
225	8C
226	98
227	A5
228	B0
229	BC
230	C7
231	D1
232	DA
233	E2
234	EA
235	F0
236	F6
237	FA
238	FD
239	FF
240	FF
241	FF
242	FD
243	FA
244	F6
245	F0

No	Data (Hex)
246	EA
247	E2
248	DA
249	D1
250	C7
251	BC
252	B0
253	A5
254	98
255	8C
256	80

TABEL PENGUKURAN LINEARITAS DIGITAL TO ANALOG CONVERTER (DAC)

DEC	B0	B1	B2	B3	B4	B5	B6	B7	V0 DAC (volt)
0	0	0	0	0	0	0	0	0	-5.02
1	0	0	0	0	0	0	0	1	-4.99
2	0	0	0	0	0	0	1	0	-4.95
3	0	0	0	0	0	0	1	1	-4.91
4	0	0	0	0	0	1	0	0	-4.87
5	0	0	0	0	0	1	0	1	-4.83
6	0	0	0	0	0	1	1	0	-4.79
7	0	0	0	0	0	1	1	1	-4.76
8	0	0	0	0	1	0	0	0	-4.71
9	0	0	0	0	1	0	0	1	-4.68
10	0	0	0	0	1	0	1	0	-4.64
11	0	0	0	0	1	0	1	1	-4.60
12	0	0	0	0	1	1	0	0	-4.56
13	0	0	0	0	1	1	0	1	-4.52
14	0	0	0	0	1	1	1	0	-4.48
15	0	0	0	0	1	1	1	1	-4.45
16	0	0	0	1	0	0	0	0	-4.41
17	0	0	0	1	0	0	0	1	-4.37
18	0	0	0	1	0	0	1	0	-4.33
19	0	0	0	1	0	0	1	1	-4.29
20	0	0	0	1	0	1	0	0	-4.26
21	0	0	0	1	0	1	0	1	-4.22
22	0	0	0	1	0	1	1	0	-4.18
23	0	0	0	1	0	1	1	1	-4.14
24	0	0	0	1	1	0	0	0	-4.10
25	0	0	0	1	1	0	0	1	-4.06
26	0	0	0	1	1	0	1	0	-4.02
27	0	0	0	1	1	0	1	1	-3.98
28	0	0	0	1	1	1	0	0	-3.94
29	0	0	0	1	1	1	0	1	-3.91
30	0	0	0	1	1	1	1	0	-3.87
31	0	0	0	1	1	1	1	1	-3.83
32	0	0	1	0	0	0	0	0	-3.79
33	0	0	1	0	0	0	0	1	-3.76
34	0	0	1	0	0	0	1	0	-3.72
35	0	0	1	0	0	0	1	1	-3.68
36	0	0	1	0	0	1	0	0	-3.64

37	0	0	1	0	0	1	0	1	-3.61
38	0	0	1	0	0	1	1	0	-3.57
39	0	0	1	0	0	1	1	1	-3.53
40	0	0	1	0	1	0	0	0	-3.49
41	0	0	1	0	1	0	0	1	-3.45
42	0	0	1	0	1	0	1	0	-3.41
43	0	0	1	0	1	0	1	1	-3.37
44	0	0	1	0	1	1	0	0	-3.34
45	0	0	1	0	1	1	0	1	-3.30
46	0	0	1	0	1	1	1	0	-3.26
47	0	0	1	0	1	1	1	1	-3.22
48	0	0	1	1	0	0	0	0	-3.18
49	0	0	1	1	0	0	0	1	-3.14
50	0	0	1	1	0	0	1	0	-3.10
51	0	0	1	1	0	0	1	1	-3.06
52	0	0	1	1	0	1	0	0	-3.03
53	0	0	1	1	0	1	0	1	-2.99
54	0	0	1	1	0	1	1	0	-2.95
55	0	0	1	1	0	1	1	1	-2.91
56	0	0	1	1	1	0	0	0	-2.87
57	0	0	1	1	1	0	0	1	-2.83
58	0	0	1	1	1	0	1	0	-2.79
59	0	0	1	1	1	0	1	1	-2.76
60	0	0	1	1	1	1	0	0	-2.72
61	0	0	1	1	1	1	0	1	-2.68
62	0	0	1	1	1	1	1	0	-2.64
63	0	0	1	1	1	1	1	1	-2.60
64	0	1	0	0	0	0	0	0	-2.57
65	0	1	0	0	0	0	0	1	-2.53
66	0	1	0	0	0	0	1	0	-2.49
67	0	1	0	0	0	0	1	1	-2.45
68	0	1	0	0	0	1	0	0	-2.42
69	0	1	0	0	0	1	0	1	-2.38
70	0	1	0	0	0	1	1	0	-2.34
71	0	1	0	0	0	1	1	1	-2.30
72	0	1	0	0	1	0	0	0	-2.26
73	0	1	0	0	1	0	0	1	-2.22
74	0	1	0	0	1	0	1	0	-2.19
75	0	1	0	0	1	0	1	1	-2.15
76	0	1	0	0	1	1	0	0	-2.11
77	0	1	0	0	1	1	0	1	-2.08

78	0	1	0	0	1	1	1	0	-2.04
79	0	1	0	0	1	1	1	1	-1.99
80	0	1	0	1	0	0	0	0	-1.96
81	0	1	0	1	0	0	0	1	-1.92
82	0	1	0	1	0	0	1	0	-1.88
83	0	1	0	1	0	0	1	1	-1.84
84	0	1	0	1	0	1	0	0	-1.80
85	0	1	0	1	0	1	0	1	-1.77
86	0	1	0	1	0	1	1	0	-1.73
87	0	1	0	1	0	1	1	1	-1.69
88	0	1	0	1	1	0	0	0	-1.65
89	0	1	0	1	1	0	0	1	-1.61
90	0	1	0	1	1	0	1	0	-1.57
91	0	1	0	1	1	0	1	1	-1.54
92	0	1	0	1	1	1	0	0	-1.50
93	0	1	0	1	1	1	0	1	-1.46
94	0	1	0	1	1	1	1	0	-1.42
95	0	1	0	1	1	1	1	1	-1.38
96	0	1	1	0	0	0	0	0	-1.34
97	0	1	1	0	0	0	0	1	-1.31
98	0	1	1	0	0	0	1	0	-1.27
99	0	1	1	0	0	0	1	1	-1.23
100	0	1	1	0	0	1	0	0	-1.19
101	0	1	1	0	0	1	0	1	-1.15
102	0	1	1	0	0	1	1	0	-1.11
103	0	1	1	0	0	1	1	1	-1.07
104	0	1	1	0	1	0	0	0	-1.03
105	0	1	1	0	1	0	0	1	-0.99
106	0	1	1	0	1	0	1	0	-0.96
107	0	1	1	0	1	0	1	1	-0.92
108	0	1	1	0	1	1	0	0	-0.88
109	0	1	1	0	1	1	0	1	-0.84
110	0	1	1	0	1	1	1	0	-0.80
111	0	1	1	0	1	1	1	1	-0.76
112	0	1	1	1	0	0	0	0	-0.73
113	0	1	1	1	0	0	0	1	-0.70
114	0	1	1	1	0	0	1	0	-0.66
115	0	1	1	1	0	0	1	1	-0.62
116	0	1	1	1	0	1	0	0	-0.58
117	0	1	1	1	0	1	0	1	-0.54
118	0	1	1	1	0	1	1	0	-0.51

119	0	1	1	1	0	1	1	1	-0.47
120	0	1	1	1	1	0	0	0	-0.43
121	0	1	1	1	1	0	0	1	-0.39
122	0	1	1	1	1	0	1	0	-0.35
123	0	1	1	1	1	0	1	1	-0.31
124	0	1	1	1	1	1	0	0	-0.27
125	0	1	1	1	1	1	0	1	-0.23
126	0	1	1	1	1	1	1	0	-0.19
127	0	1	1	1	1	1	1	1	-0.15
128	1	0	0	0	0	0	0	0	-0.12
129	1	0	0	0	0	0	0	1	-0.08
130	1	0	0	0	0	0	1	0	-0.05
131	1	0	0	0	0	0	1	1	-0.01
132	1	0	0	0	0	1	0	0	0.03
133	1	0	0	0	0	1	0	1	0.07
134	1	0	0	0	0	1	1	0	0.11
135	1	0	0	0	0	1	1	1	0.15
136	1	0	0	0	1	0	0	0	0.19
137	1	0	0	0	1	0	0	1	0.23
138	1	0	0	0	1	0	1	0	0.27
139	1	0	0	0	1	0	1	1	0.30
140	1	0	0	0	1	1	0	0	0.34
141	1	0	0	0	1	1	0	1	0.37
142	1	0	0	0	1	1	1	0	0.41
143	1	0	0	0	1	1	1	1	0.45
144	1	0	0	1	0	0	0	0	0.49
145	1	0	0	1	0	0	0	1	0.53
146	1	0	0	1	0	0	1	0	0.57
147	1	0	0	1	0	0	1	1	0.61
148	1	0	0	1	0	1	0	0	0.65
149	1	0	0	1	0	1	0	1	0.69
150	1	0	0	1	0	1	1	0	0.73
151	1	0	0	1	0	1	1	1	0.77
152	1	0	0	1	1	0	0	0	0.80
153	1	0	0	1	1	0	0	1	0.84
154	1	0	0	1	1	0	1	0	0.88
155	1	0	0	1	1	0	1	1	0.92
156	1	0	0	1	1	1	0	0	0.96
157	1	0	0	1	1	1	0	1	0.98
158	1	0	0	1	1	1	1	0	1.02
159	1	0	0	1	1	1	1	1	1.06

160	1	0	1	0	0	0	0	0	1.10
161	1	0	1	0	0	0	0	1	1.14
162	1	0	1	0	0	0	1	0	1.18
163	1	0	1	0	0	0	1	1	1.22
164	1	0	1	0	0	1	0	0	1.26
165	1	0	1	0	0	1	0	1	1.30
166	1	0	1	0	0	1	1	0	1.33
167	1	0	1	0	0	1	1	1	1.37
168	1	0	1	0	1	`	0	0	1.41
169	1	0	1	0	1	0	0	1	1.45
170	1	0	1	0	1	0	1	0	1.49
171	1	0	1	0	1	0	1	1	1.53
172	1	0	1	0	1	1	0	0	1.57
173	1	0	1	0	1	1	0	1	1.60
174	1	0	1	0	1	1	1	0	1.64
175	1	0	1	0	1	1	1	1	1.68
176	1	0	1	1	0	0	0	0	1.72
177	1	0	1	1	0	0	0	1	1.76
178	1	0	1	1	0	0	1	0	1.80
179	1	0	1	1	0	0	1	1	1.84
180	1	0	1	1	0	1	0	0	1.88
181	1	0	1	1	0	1	0	1	1.90
182	1	0	1	1	0	1	1	0	1.94
183	1	0	1	1	0	1	1	1	1.98
184	1	0	1	1	1	0	0	0	2.02
185	1	0	1	1	1	0	0	1	2.06
186	1	0	1	1	1	0	1	0	2.10
187	1	0	1	1	1	0	1	1	2.14
188	1	0	1	1	1	1	0	0	2.17
189	1	0	1	1	1	1	0	1	2.21
190	1	0	1	1	1	1	1	0	2.25
191	1	0	1	1	1	1	1	1	2.28
192	1	1	0	0	0	0	0	0	2.32
193	1	1	0	0	0	0	0	1	2.36
194	1	1	0	0	0	0	1	0	2.40
195	1	1	0	0	0	0	1	1	2.44
196	1	1	0	0	0	1	0	0	2.48
197	1	1	0	0	0	1	0	1	2.52
198	1	1	0	0	0	1	1	0	2.56
199	1	1	0	0	0	1	1	1	2.60
200	1	1	0	0	1	0	0	0	2.64

201	1	1	0	0	1	0	0	1	2.68
202	1	1	0	0	1	0	1	0	2.71
203	1	1	0	0	1	0	1	1	2.75
204	1	1	0	0	1	1	0	0	2.79
205	1	1	0	0	1	1	0	1	2.83
206	1	1	0	0	1	1	1	0	2.87
207	1	1	0	0	1	1	1	1	2.91
208	1	1	0	1	0	0	0	0	2.94
209	1	1	0	1	0	0	0	1	2.98
210	1	1	0	1	0	0	1	0	3.02
211	1	1	0	1	0	0	1	1	3.06
212	1	1	0	1	0	1	0	0	3.09
213	1	1	0	1	0	1	0	1	3.13
214	1	1	0	1	0	1	1	0	3.17
215	1	1	0	1	0	1	1	1	3.21
216	1	1	0	1	1	0	0	0	3.25
217	1	1	0	1	1	0	0	1	3.29
218	1	1	0	1	1	0	1	0	3.33
219	1	1	0	1	1	0	1	1	3.37
220	1	1	0	1	1	1	0	0	3.40
221	1	1	0	1	1	1	0	1	3.44
222	1	1	0	1	1	1	1	0	3.48
223	1	1	0	1	1	1	1	1	3.52
224	1	1	1	0	0	0	0	0	3.56
225	1	1	1	0	0	0	0	1	3.60
226	1	1	1	0	0	0	1	0	3.64
227	1	1	1	0	0	0	1	1	3.68
228	1	1	1	0	0	1	0	0	3.72
229	1	1	1	0	0	1	0	1	3.76
230	1	1	1	0	0	1	1	0	3.80
231	1	1	1	0	0	1	1	1	3.84
232	1	1	1	0	1	0	0	0	3.88
233	1	1	1	0	1	0	0	1	3.91
234	1	1	1	0	1	0	1	0	3.95
235	1	1	1	0	1	0	1	1	3.98
236	1	1	1	0	1	1	0	0	4.01
237	1	1	1	0	1	1	0	1	4.05
238	1	1	1	0	1	1	1	0	4.09
239	1	1	1	0	1	1	1	1	4.13
240	1	1	1	1	0	0	0	0	4.17
241	1	1	1	1	0	0	0	1	4.20

242	1	1	1	1	0	0	1	0	4.24
243	1	1	1	1	0	0	1	1	4.28
244	1	1	1	1	0	1	0	0	4.32
245	1	1	1	1	0	1	0	1	4.36
246	1	1	1	1	0	1	1	0	4.40
247	1	1	1	1	0	1	1	1	4.44
248	1	1	1	1	1	0	0	0	4.48
249	1	1	1	1	1	0	0	1	4.51
250	1	1	1	1	1	0	1	0	4.55
251	1	1	1	1	1	0	1	1	4.59
252	1	1	1	1	1	1	0	0	4.63
253	1	1	1	1	1	1	0	1	4.67
254	1	1	1	1	1	1	1	0	4.70
255	1	1	1	1	1	1	1	1	4.74

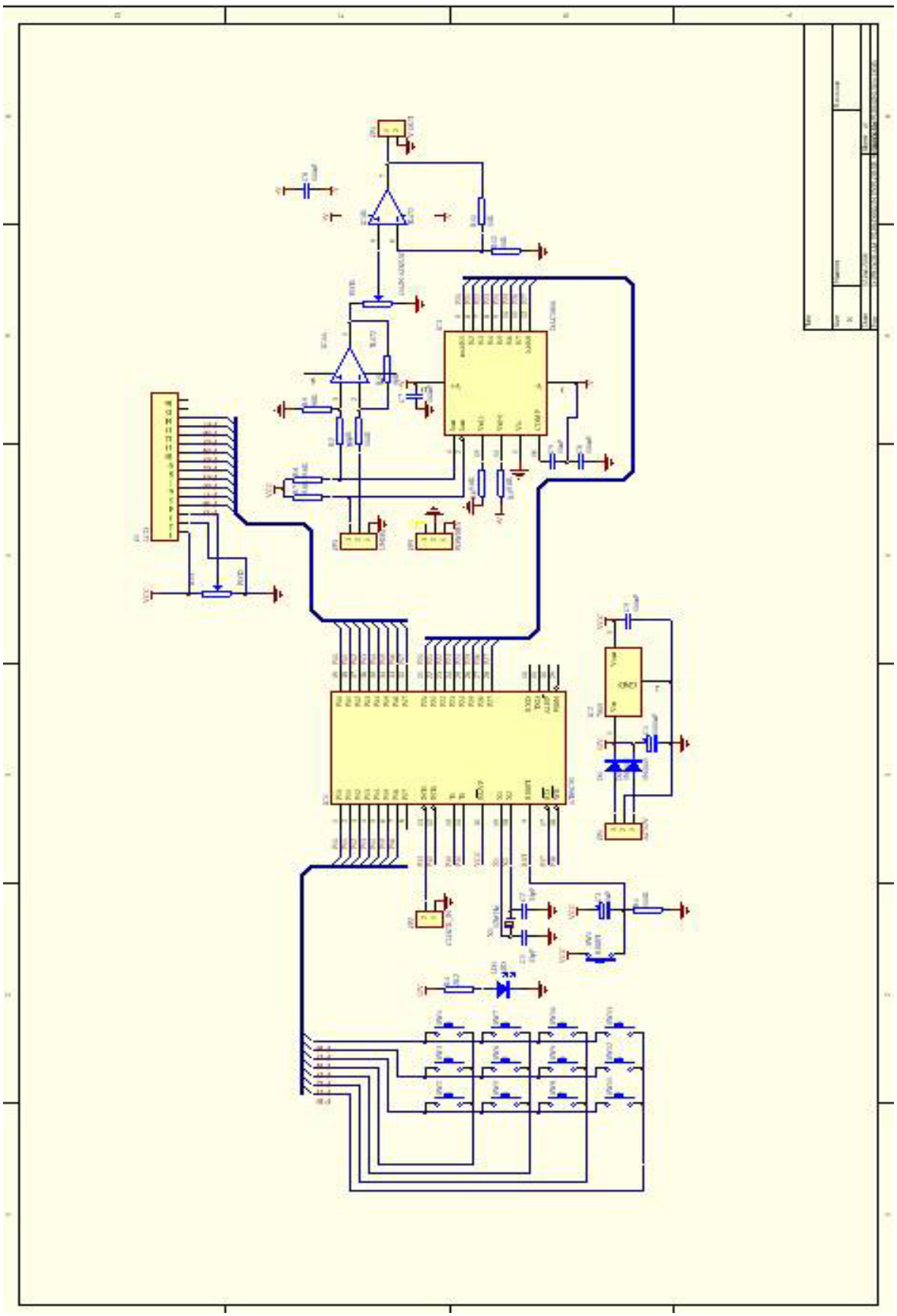
Tabel Pengukuran Karakteristik Frekuensi Lowpass

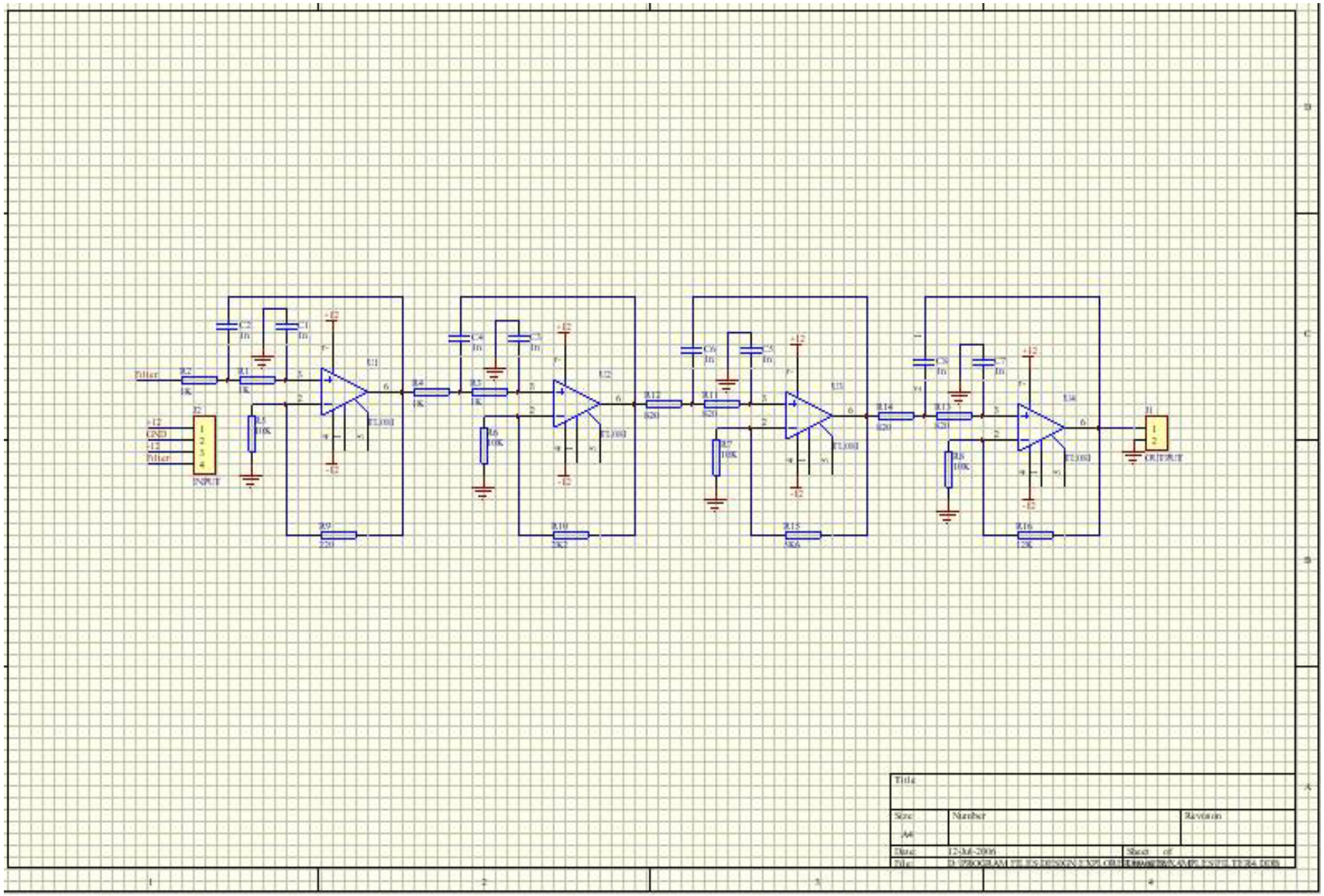
No	Frekuensi (Hz)	Vout (Volt)
1	150	4.20
2	300	4.20
3	400	4.20
4	500	4.20
5	600	4.20
6	700	4.20
7	800	4.20
8	900	4.20
9	1000	4.20
10	1100	4.20
11	1200	4.20
12	1300	4.20
13	1400	4.20
14	1500	4.20
15	1600	4.15
16	1700	4.15
17	1800	4.15
18	1900	4.15
19	2000	4.15
20	2200	4.15
21	2400	4.15
22	2600	4.15
23	2800	4.15
24	3000	4.15
25	3200	4.15
26	3400	4.15
27	3600	4.00
28	3800	4.00
29	4000	4.00
30	4400	4.00
31	4800	4.00
32	5200	4.00
33	5600	4.00
34	6000	4.00
35	6500	4.00
36	7000	4.00
37	7500	4.00
38	8000	4.00

No	Frekuensi (Hz)	Vout (Volt)
39	8500	4.00
40	9000	4.00
41	9500	4.00
42	10000	4.00
43	15000	4.00
44	20000	4.00
45	25000	3.90
46	30000	3.87
47	35000	3.80
48	40000	3.70
49	45000	3.63
50	50000	3.60
51	55000	3.52
52	60000	3.40
53	65000	3.30
54	70000	3.22
55	75000	3.10
56	80000	3.00
57	85000	2.90
58	90000	2.90
59	95000	2.80
60	100000	2.60
61	110000	2.40
62	120000	2.20
63	130000	2.00
64	140000	1.80
65	150000	1.40
66	160000	1.10
67	170000	0.80
68	180000	0.50
69	190000	0.30
70	200000	0.20
71	210000	0.15
72	220000	0.10
73	230000	0.10

LAMPIRAN E

SKEMA RANGKAIAN MODULATOR DIGITAL

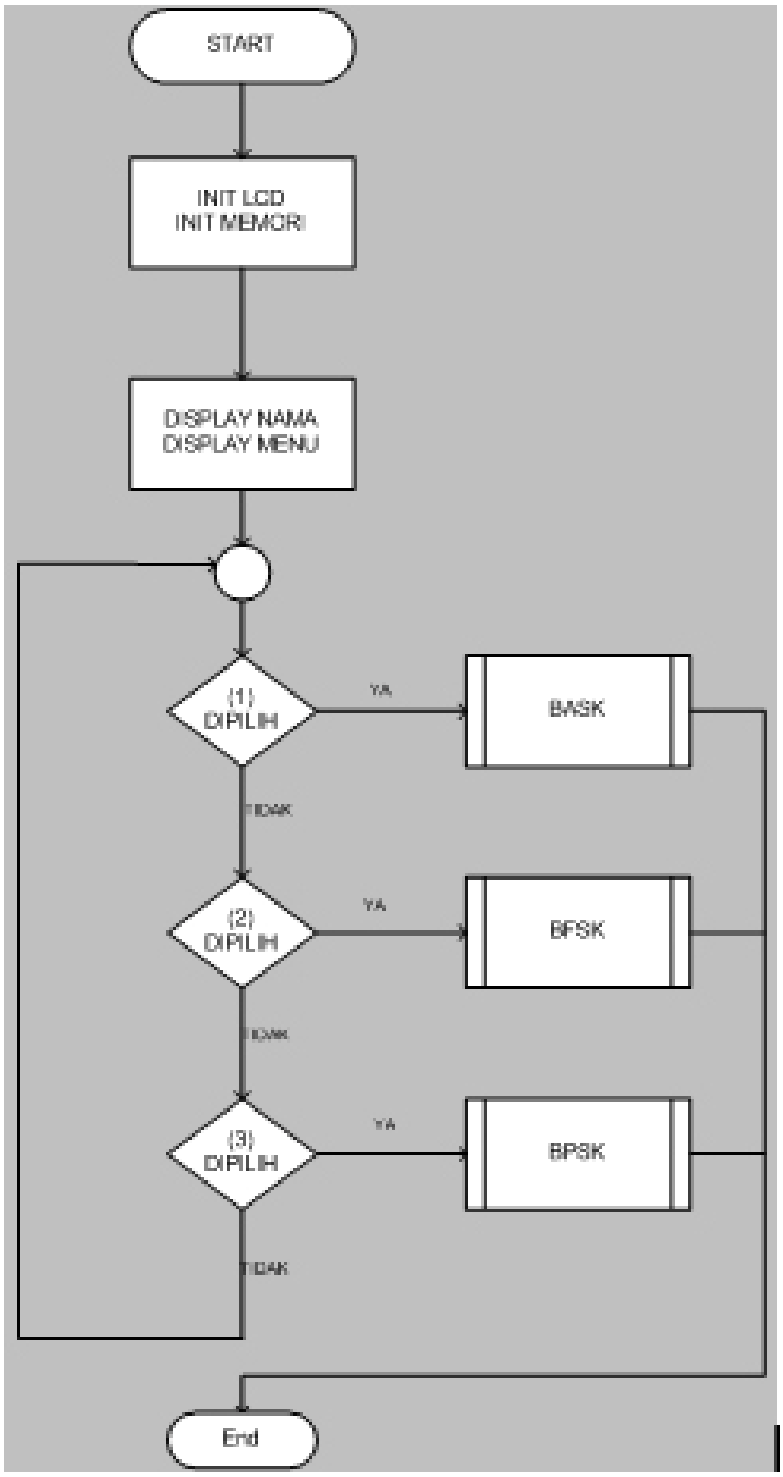



Filter
+12
GND
+12
Filter
J2
1
2
3
4
INPUT
C2
1n
C1
1n
+12
R2
1K
R1
1K
U1
TL081
R3
10K
-12
R9
220
C4
1n
C3
1n
R4
1K
R7
1K
U2
TL081
R6
10K
R10
5K6
C6
1n
C5
1n
R12
820
R11
820
U3
TL081
R7
10K
R13
5K6
C8
1n
C7
1n
R14
820
R17
820
U4
TL081
R8
10K
R15
5K6
R16
15K
J1
1
2
OUTPUT
Title
Size
A4
Number
Revision
Date:
12-Jul-2006
Sheet of
File:

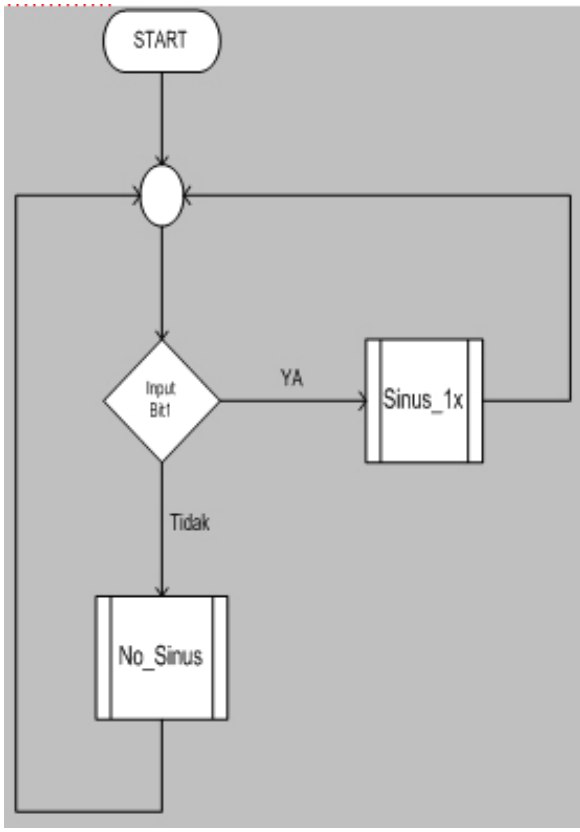
LAMPIRAN F

FLOWCHART

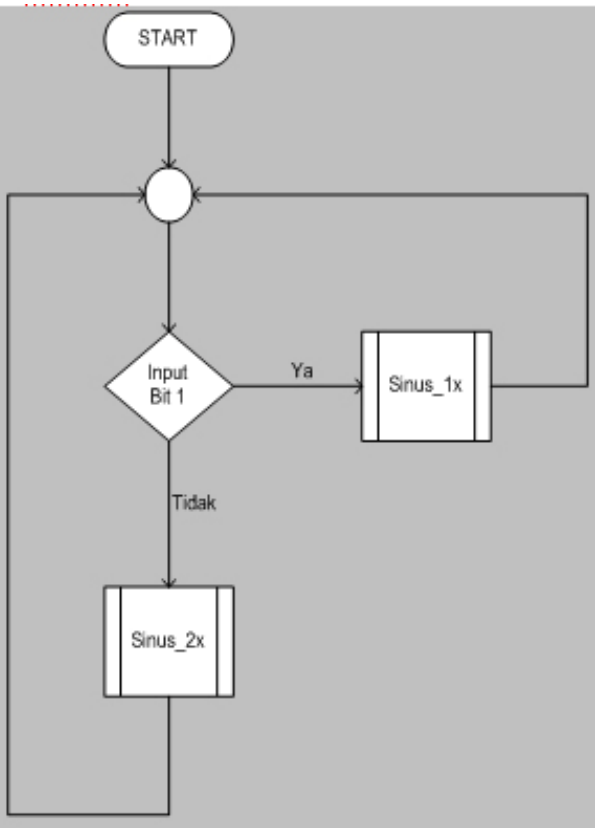
Flowchart Utama



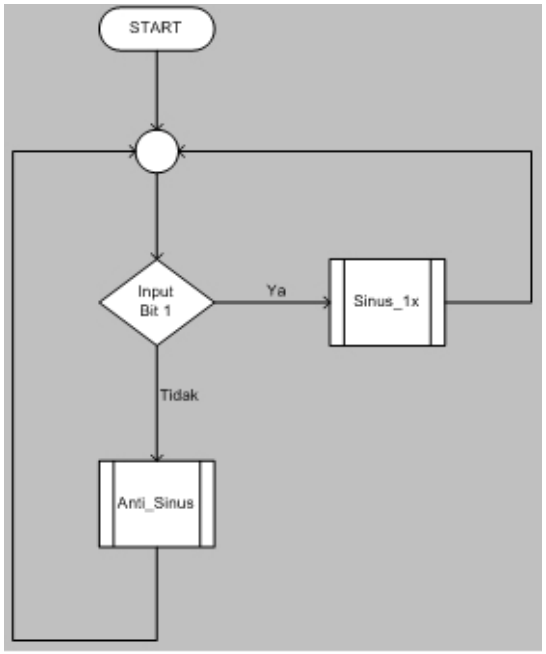
Subrutin BASK



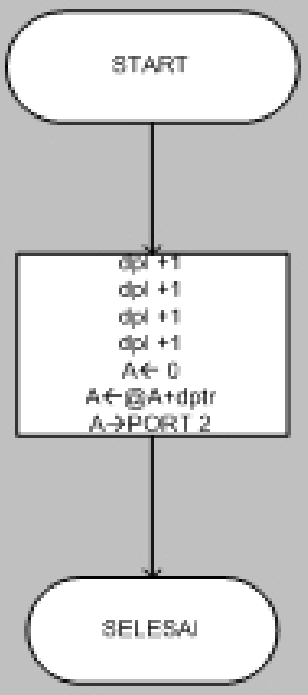
Subrutin BFSK



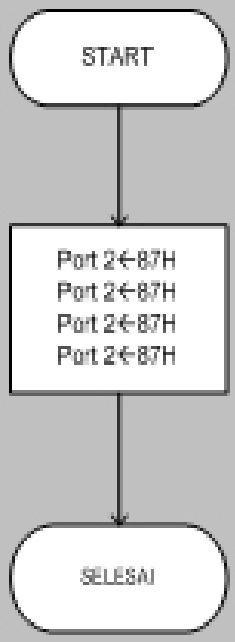
Subrutin BPSK



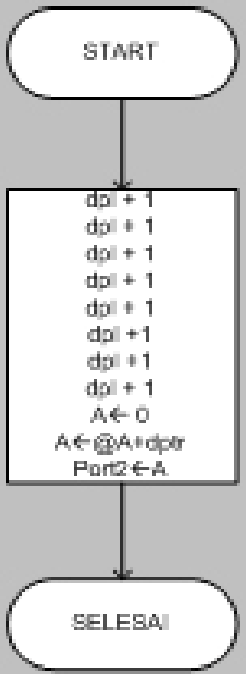
Subrutin Sinus_1x



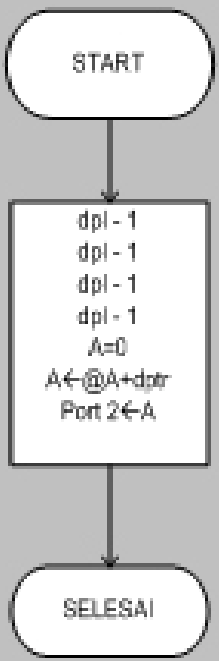
Subrutin No_Sinus



Subrutin Sinus_2x



Subrutin Anti_Sinus



LAMPIRAN G

LISTING PROGRAM

```
;-------------------------------------------------------------------------------
; Modulator Digital BASK, BPSK, BFSK dgn Metoda DDS(Direct Digital Synthesis)
; Nama : Wi.Arbi.Kamto
; NRP  : 0122006
; Dosen: Ir Daniel Setiadikurnia.,MT
; Modulator Digital BASK, BPSK, BFSK dgn Metoda DDS(Direct Digital Synthesis)
;-------------------------------------------------------------------------------

;------------------ Pin Assignment -----------------------------------------
; LCD :
;       D1 - D8         ->      p0
        rs              equ     p3.5
        rw              equ     p3.6
        en              equ     p3.7
        ;
; KEYPAD :
        col1            equ     p1.4
        col2            equ     p1.5
        col3            equ     p1.6
        row1            equ     p1.3
        row2            equ     p1.2
        row3            equ     p1.1
        row4            equ     p1.0
        ;
; DAC 0800 :
        dac_data        equ     p2
        ;
; Clock Out :
        clock_out       equ     p3.4
        clock_in        equ     p3.3
        ;

;------------------ Buffer -------------------------------------------------
; bit :
        pressf          bit     00h
        timer0_flag     bit     01h

; byte :
        ascii_buff      equ     30h
        timer0_buff     equ     31h
        temp_1          equ     32h
        temp_2          equ     33h
        ;
;------------------ Page Zero ----------------------------------------------
                org 0000h
                sjmp init
```

```
                ;

        org 000bh
        ljmp timer0
                ;
;------------------ Inisialisasi ----------------------------------------------
        org 0030h
init:
        mov sp,#4fh

                mov th0,#0ffh           ;60mS
                mov tl0,#0c3h
                clr clock_out
                mov timer0_buff,#20
                setb timer0_flag

        mov tmod,#01h
        mov ie,#10000010b
        mov tcon,#00001100b

        call init_lcd           ;inisialisasi LCD
                ;

;------------------ Mian Program ----------------------------------------------
        call clr_scr
        mov dptr,#msg1              ;
        call line1
        mov dptr,#msg2              ;
        call line2

                call delay_500ms
                call delay_500ms
                call delay_500ms
                call delay_500ms
select_mod:
                call clr_scr
                mov dptr,#msg3                  ;
                call line1
                mov dptr,#msg4                  ;
                call line2
chk_select:     call qchk
                jnb pressf,chk_select
                mov a,ascii_buff
                cjne a,#'1',chk_2
                call clr_scr
                 mov dptr,#msg5                 ;
```

```
                call line1
                jb clock_in,$
                mov dptr,#rom_sinus
                jmp bask
chk_2:          cjne a,#'2',chk_3
                call clr_scr
                mov dptr,#msg5          ;
                call line1
                jb clock_in,$
                mov dptr,#rom_sinus
                jmp bfsk
chk_3:          cjne a,#'3',chk_select
                call clr_scr
                mov dptr,#msg5          ;
                call line1
                jb clock_in,$
                mov dptr,#rom_sinus
                jmp bpsk
                ;
;-------------------------------------------------------------------------------
bask:
                jnb clock_in,_no_sinus
                call sinus_1x
                jmp bask
_no_sinus:      call no_sinus
                jmp bask
                ;
;-------------------------------------------------------------------------------
bfsk:
                jnb clock_in,_sinus_2x
                call sinus_1x
                jmp bfsk
_sinus_2x:
                call sinus_2x
                call sinus_2x
                jmp bfsk
                ;
;-------------------------------------------------------------------------------
bpsk:
                jnb clock_in,_anti_sinus
                mov dptr,#rom_sinus
                call sinus_1x
                jmp bpsk
_anti_sinus:    call anti_sinus
                jmp bpsk
                ;
```

```
;-------------------------------------------------------------------------
sinus_1x:
                inc dpl
                inc dpl
                inc dpl
                inc dpl
                clr a
                movc a,@a+dptr
                mov dac_data,a
                ret
                ;
;-------------------------------------------------------------------------
sinus_2x:
                inc dpl
                inc dpl
                inc dpl
                inc dpl
                inc dpl
                inc dpl
                inc dpl
                inc dpl
                clr a
                movc a,@a+dptr
                mov dac_data,a
                ret
                ;
;-------------------------------------------------------------------------
anti_sinus:
                dec dpl
                dec dpl
                dec dpl
                dec dpl
                clr a
                movc a,@a+dptr
                mov dac_data,a
                ret
                ;
;-------------------------------------------------------------------------
no_sinus:
                mov dac_data,#(0ffh-078h)
                mov dac_data,#(0ffh-078h)
                mov dac_data,#(0ffh-078h)
                mov dac_data,#(0ffh-078h)
                ret
                ;
```

```
;------------------ Timer 0 ----------------------------------------------------
timer0:
                mov th0,#0ffh           ;60mS
                mov tl0,#0c3h
                cpl clock_out
                reti
                ;
;------------------ Keypad -----------------------------------------------------
qchk:
        clr pressf
        clr row1
        jb col1,pad_1
        call delay_30ms
        jnb col1,$
        mov ascii_buff,#'1'
        setb row1
        ljmp pad_12
                ;
pad_1:
        jb col2,pad_2
        call delay_30ms
        jnb col2,$
        mov ascii_buff,#'2'
        setb row1
        ljmp pad_12
                ;
pad_2:
        jb col3,pad_3
        call delay_30ms
        jnb col3,$
        mov ascii_buff,#'3'
        setb row1
        ljmp pad_12
                ;
pad_3:
        setb row1
        clr row2
        jb col1,pad_4
        call delay_30ms
        jnb col1,$
        mov ascii_buff,#'4'
        setb row2
        ljmp pad_12
                ;
```

```
pad_4:
        jb col2,pad_5
        call delay_30ms
        jnb col2,$
        mov ascii_buff,#'5'
        setb row2
        ljmp pad_12
                ;
pad_5:
        jb col3,pad_6
        call delay_30ms
        jnb col3,$
        mov ascii_buff,#'6'
        setb row2
        ljmp pad_12
                ;
pad_6:
        setb row2
        clr row3
        jb col1,pad_7
        call delay_30ms
        jnb col1,$
        mov ascii_buff,#'7'
        setb row3
        jmp pad_12
                ;
pad_7:
        jb col2,pad_8
        call delay_30ms
        jnb col2,$
        mov ascii_buff,#'8'
        setb row3
        sjmp pad_12
                ;
pad_8:
        jb col3,pad_9
        call delay_30ms
        jnb col3,$
        mov ascii_buff,#'9'
        setb row3
        sjmp pad_12
                ;
pad_9:
        setb row3
        clr row4
        jb col1,pad_10
```

```
        call delay_30ms
        jnb col1,$
        mov ascii_buff,#'*'
        setb row4
        sjmp pad_12
pad_10:
        jb col2,pad_11
        call delay_30ms
        jnb col2,$
                mov ascii_buff,#'0'
        setb row4
        sjmp pad_12
pad_11:
        jb col3,exitkeypad
        call delay_30ms
        jnb col3,$
        mov ascii_buff,#'#'
        setb row4
pad_12:
        setb pressf
exitkeypad:
        setb row4
        ret
        ;
;------------------ LCD 2X20 ---------------------------------------------------
line1:      push acc
            mov acc,#80h
            call iwr
            call line
            pop acc
            ret
            ;
line2:       push acc
            mov acc,#0c0h
            call iwr
            call line
            pop acc
            ret
            ;
line:        clr a
            movc a,@a+dptr
            cjne a,#0ffh,go_on
            ret
            ;
go_on:      call dwr
            inc dptr
```

```
            jmp line
            ;

dwr:        mov p0,a            ;kirim data di a ke p0
            setb rs             ;rs = 1
            clr rw              ;rw = 0
            setb en             ;en = 1
            clr en              ;en = 0
            call delay_1ms      ;tunggu 1ms
            ret
            ;
iwr_1:      mov p0,a            ;kirim data di a ke p0
            clr rs              ;rs = 0
            clr rw              ;rw = 0
            setb en             ;en = 1
            clr en              ;en = 0
            call delay_10ms     ;tunggu 10ms
            ret
            ;
iwr:        mov p0,a            ;kirim data di a ke p0
            clr rs              ;rs = 0
            clr rw              ;rw = 0
            setb en             ;en = 1
            clr en              ;en = 0
            call delay_1ms      ;tunggu 1ms
            ret
            ;
clr_scr:    push acc
            mov a,#01h          ; clear display
            call iwr_1
            pop acc
            ret
            ;
blink:      push acc
            mov a,#0dh          ;blink char
            call iwr
            pop acc
            ret
            ;
stopblink: push acc
            mov a,#0ch      ;
            call iwr
            pop acc
            ret
            ;
```

```
init_lcd:   push acc
            call delay_30ms
            clr a
            mov a,#30h          ;interface is 8*bit long
            call iwr_1
            call iwr_1
            call iwr_1
            mov a,#38h          ;display off
            call iwr_1
            mov a,#08h          ;display off
            call iwr_1
            mov a,#01h
            call iwr_1
            mov a,#06h          ;inc
            call iwr_1
            mov a,#0ch          ;on
            call iwr_1
            pop acc
            ret
            ;

;------------------ Charakter Area -----------------------------------------
msg0:   db'                             ', 0ffh;
msg1:   db'Nama: Wi Arbi Kamto      ',0ffh;
msg2:   db'NRP : 0122006             ',0ffh;
msg3:   db'Modulator: (1)BASK       ',0ffh;
msg4:   db'(2)BFSK (3)BPSK          ',0ffh;
msg5:   db'Press Reset -> Stop      ',0ffh;
        ;

;------------------ Delay --------------------------------------------------

delay_1ms:      mov r6,#80          ;
loop1:          djnz r6,loop1
                ret
                ;

delay_10ms:     mov r5,#20          ;
loop3:          mov r6,#250
loop4:          djnz r6,loop4
                djnz r5,loop3
                ret
                ;

delay_30ms:     mov r5,#60          ;
loop10:         mov r6,#250
```

```
loop11:             djnz r6,loop11
                    djnz r5,loop10
                    ret
                   ;
delay_100ms:    mov r5,#200  ;
loop5:              mov r6,#250
loop6:              djnz r6,loop6
                    djnz r5,loop5
                    ret
                    ;
delay_500ms:    mov r5,#4
loop15:         mov r6,#250
loop16:         mov r7,#250
loop17:         djnz r7,loop17
                djnz r6,loop16
                djnz r5,loop15
                 ret
                  ;
;------------------ Look Up Table (ROM Sinus)---------------------------------
rom_sinus:
        db 080h, 083h, 086h, 089h, 08ch, 08fh, 092h, 095h, 098h, 09ch, 09fh
        db 0a2h, 0a5h, 0a8h, 0abh, 0aeh, 0b0h, 0b3h, 0b6h, 0b9h, 0bch, 0bfh
        db 0c1h, 0c4h, 0c7h, 0c9h, 0cch, 0ceh, 0d1h, 0d3h, 0d5h, 0d8h, 0dah
        db 0dch, 0deh, 0e0h, 0e2h, 0e4h, 0e6h, 0e8h, 0eah, 0ech, 0edh, 0efh
        db 0f0h, 0f2h, 0f3h, 0f5h, 0f6h, 0f7h, 0f8h, 0f9h, 0fah, 0fbh, 0fch
        db 0fch, 0fdh, 0feh, 0feh, 0ffh, 0ffh, 0ffh, 0ffh, 0ffh, 0ffh, 0ffh
        db 0ffh, 0ffh, 0ffh, 0ffh, 0feh, 0feh, 0fdh, 0fch, 0fch, 0fbh, 0fah
        db 0f9h, 0f8h, 0f7h, 0f6h, 0f5h, 0f3h, 0f2h, 0f0h, 0efh, 0edh, 0ech
        db 0eah, 0e8h, 0e6h, 0e4h, 0e2h, 0e0h, 0deh, 0dch, 0dah, 0d8h, 0d5h
        db 0d3h, 0d1h, 0ceh, 0cch, 0c9h, 0c7h, 0c4h, 0c1h, 0bfh, 0bch, 0b9h
        db 0b6h, 0b3h, 0b0h, 0aeh, 0abh, 0a8h, 0a5h, 0a2h, 09fh, 09ch, 098h
        db 095h, 092h, 08fh, 08ch, 089h, 086h, 083h, 080h, 080h, 07ch, 079h
        db 073h, 070h, 06dh, 06ah, 067h, 063h, 060h, 05dh, 05ah, 057h, 054h
        db 051h, 04fh, 04ch, 049h, 046h, 043h, 040h, 03eh, 03bh, 038h, 036h
        db 033h, 031h, 02eh, 02ch, 02ah, 027h, 025h, 023h, 021h, 01fh, 01fh
        db 01bh, 019h, 017h, 015h, 013h, 012h, 010h, 00fh, 00dh, 00ch, 00ah
        db 009h, 008h, 007h, 006h, 005h, 004h, 003h, 003h, 002h, 001h, 000h
        db 000h, 000h, 000h, 000h, 000h, 000h, 000h, 000h, 000h, 000h, 000h
        db 001h, 001h, 002h, 003h, 003h, 004h, 005h, 006h, 007h, 008h, 009h
        db 00ah, 00ch, 00dh, 00fh, 010h, 012h, 013h, 015h, 017h, 019h, 01bh
        db 01dh, 01fh, 021h, 023h, 025h, 027h, 02ah, 02ch, 02eh, 031h, 033h
        db 036h, 038h, 03bh, 03eh, 040h, 043h, 046h, 049h, 04ch, 04fh, 051h
        db 054h, 057h, 05ah, 05dh, 060h, 063h, 067h, 06ah, 06dh, 070h, 073h
        db 076h, 079h, 07ch
        ;
        End
```

LAMPIRAN H

DATASHEET KOMPONEN

Features

- Compatible with MCS-51™ Products
- 8K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 256 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Three 16-Bit Timer/Counters
- Eight Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

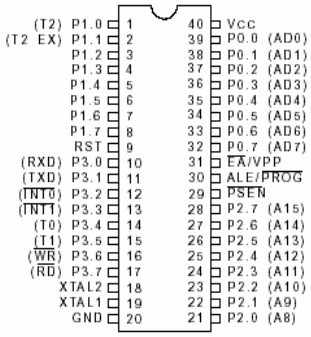
Description

The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard 80C51 and 80C52 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C52 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

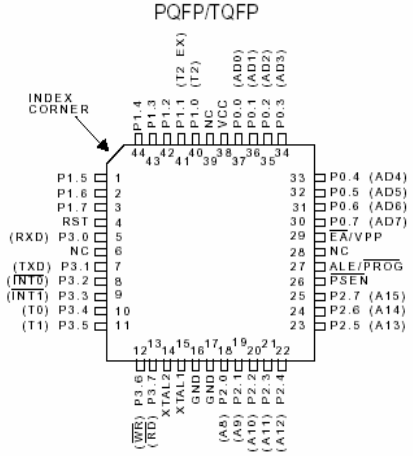
(continued)

Pin Configurations

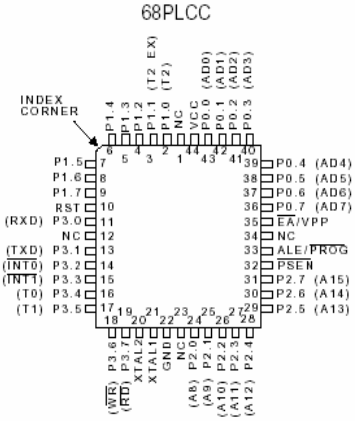
PDIP



PQFP/TQFP



68PLCC

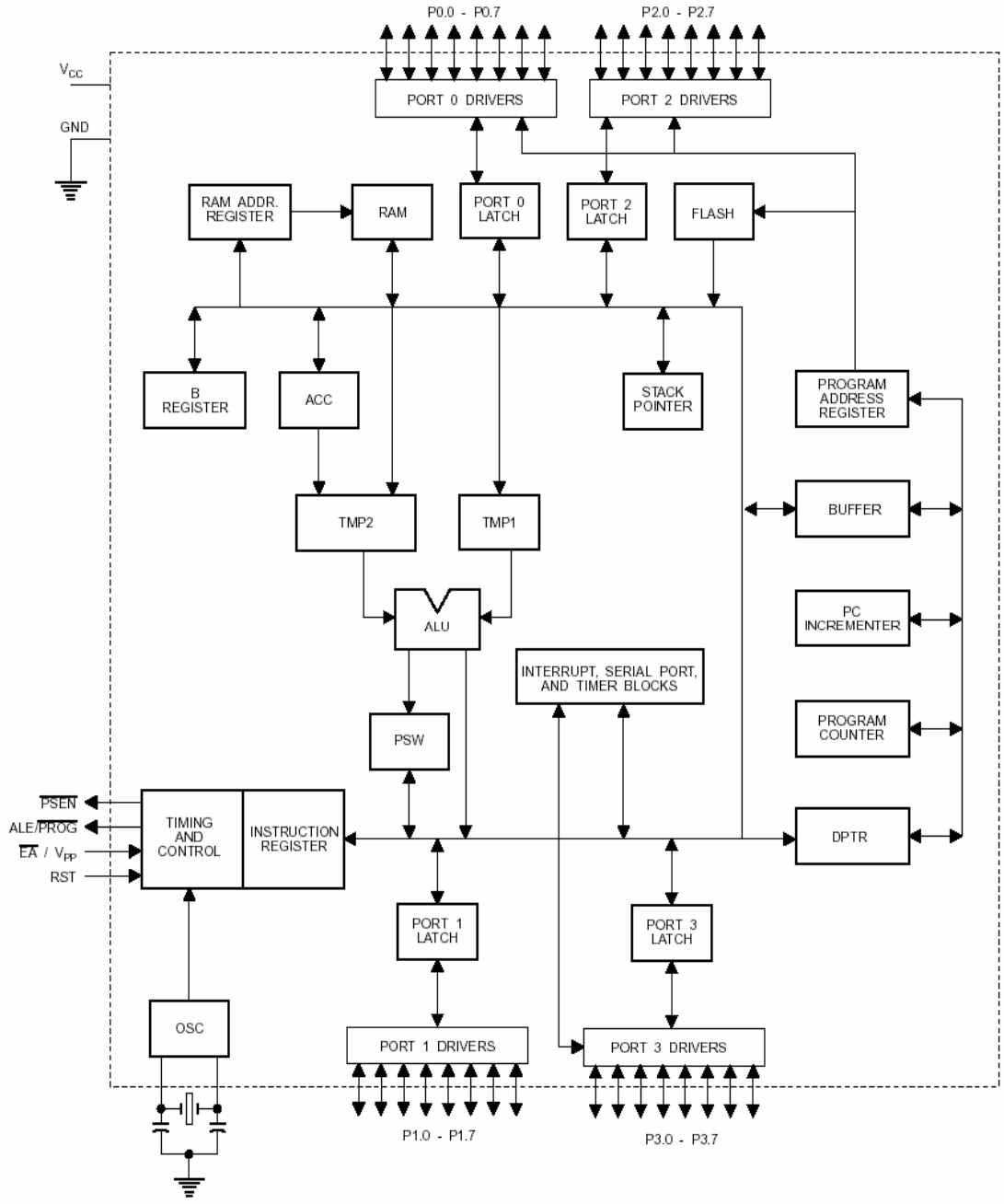


8-Bit Microcontroller with 8K Bytes Flash

AT89C52

0313F-A–12/97

Block Diagram



The AT89C52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89C52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port Pin	Alternate Functions
P1.0	T2 (external count input to Timer/Counter 2), clock-out
P1.1	T2EX (Timer/Counter 2 capture/reload trigger and direction control)

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51, as shown in the following table.

Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE

pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

When the AT89C52 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming when 12-volt programming is selected.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Table 1. AT89C52 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			0CFH
0C0H									0C7H
0B8H	IP XX000000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0X000000								0AFH
0A0H	P2 11111111								0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 0XXX0000	87H

Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Timer 2 Registers: Control and status bits are contained in registers T2CON (shown in Table 2) and T2MOD (shown in Table 4) for Timer 2. The register pair (RCAP2H, RCAP2L) are the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

Interrupt Registers: The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

Table 2. T2CON—Timer/Counter 2 Control Register

T2CON Address = 0C8H — Reset Value = 0000 0000B

Bit Addressable

Bit	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
	7	6	5	4	3	2	1	0

Symbol	Function
TF2	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1.
EXF2	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
RCLK	Receive clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	Transmit clock enable. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	Timer 2 external enable. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	Start/Stop control for Timer 2. TR2 = 1 starts the timer.
C/$\overline{T2}$	Timer or counter select for Timer 2. C/$\overline{T2}$ = 0 for timer function. C/$\overline{T2}$ = 1 for external event counter (falling edge triggered).
CP/$\overline{RL2}$	Capture/Reload select. CP/$\overline{RL2}$ = 1 causes captures to occur on negative transitions at T2EX if EXEN2 = 1. CP/$\overline{RL2}$ = 0 causes automatic reloads to occur when Timer 2 overflows or negative transitions occur at T2EX when EXEN2 = 1. When either RCLK or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Data Memory

The AT89C52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means the upper 128 bytes have the same addresses as the SFR space but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

```
MOV 0A0H, #data
```

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

```
MOV @R0, #data
```

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89C52 operate the same way as Timer 0 and Timer 1 in the AT89C51.

Timer 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/$\overline{T2}$ in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3.

Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

Table 3. Timer 2 Operating Modes

RCLK +TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-Bit Auto-Reload
0	1	1	16-Bit Capture
1	X	1	Baud Rate Generator
X	X	0	(Off)

In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

Capture Mode

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt. The capture mode is illustrated in Figure 1.

Auto-Reload (Up or Down Counter)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

Figure 1. Timer in Capture Mode

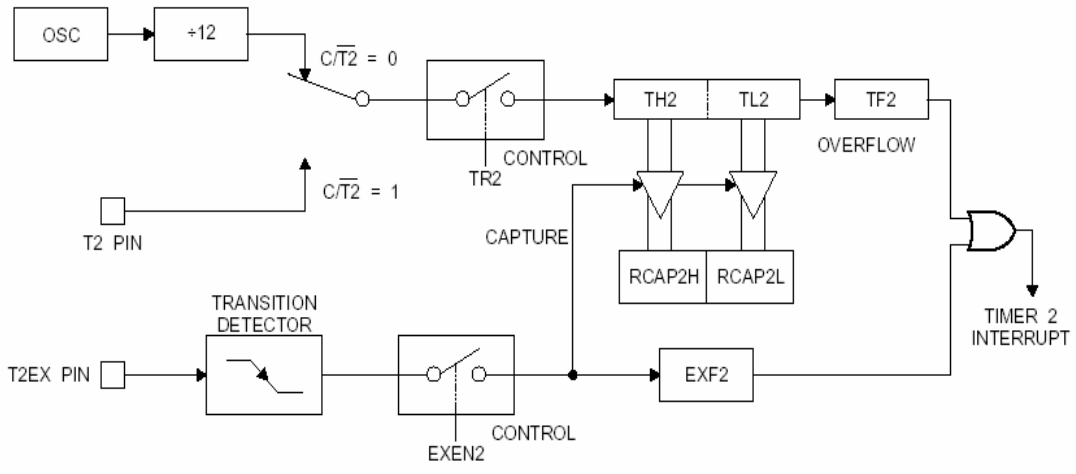


Figure 2 shows Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled.

Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. A logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

Figure 2. Timer 2 Auto Reload Mode (DCEN = 0)

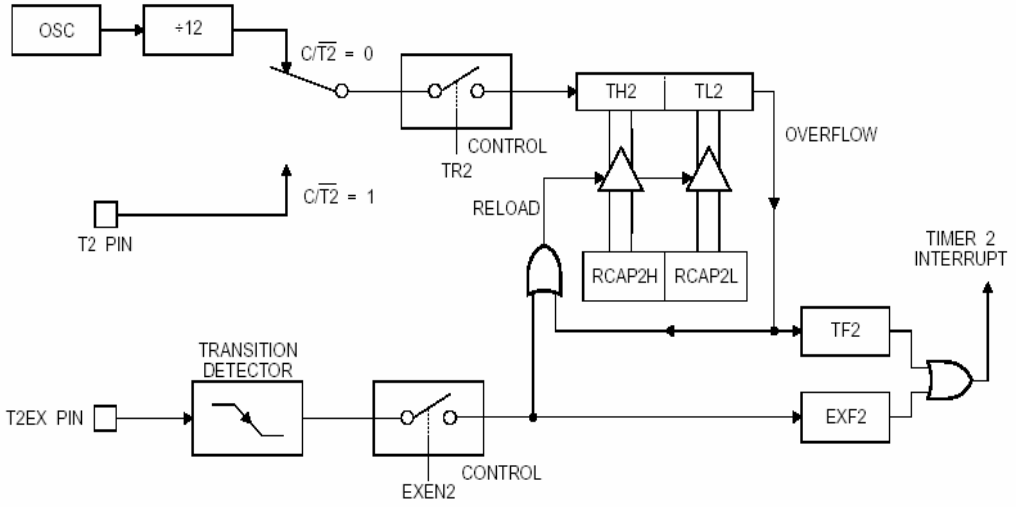


Table 4. T2MOD—Timer 2 Mode Control Register

T2MOD Address = 0C9H — Reset Value = XXXX XX00B

Not Bit Addressable

	—	—	—	—	—	—	T2OE	DCEN
Bit	7	6	5	4	3	2	1	0

Symbol	Function
—	Not implemented, reserved for future
T2OE	Timer 2 Output Enable bit.
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Figure 3. Timer 2 Auto Reload Mode (DCEN = 1)

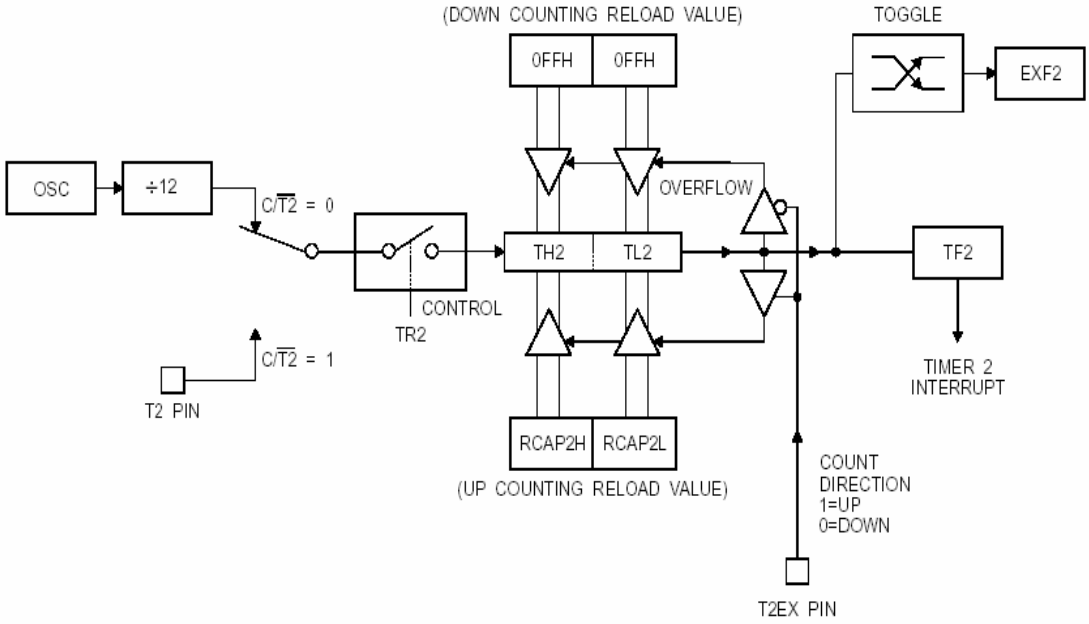
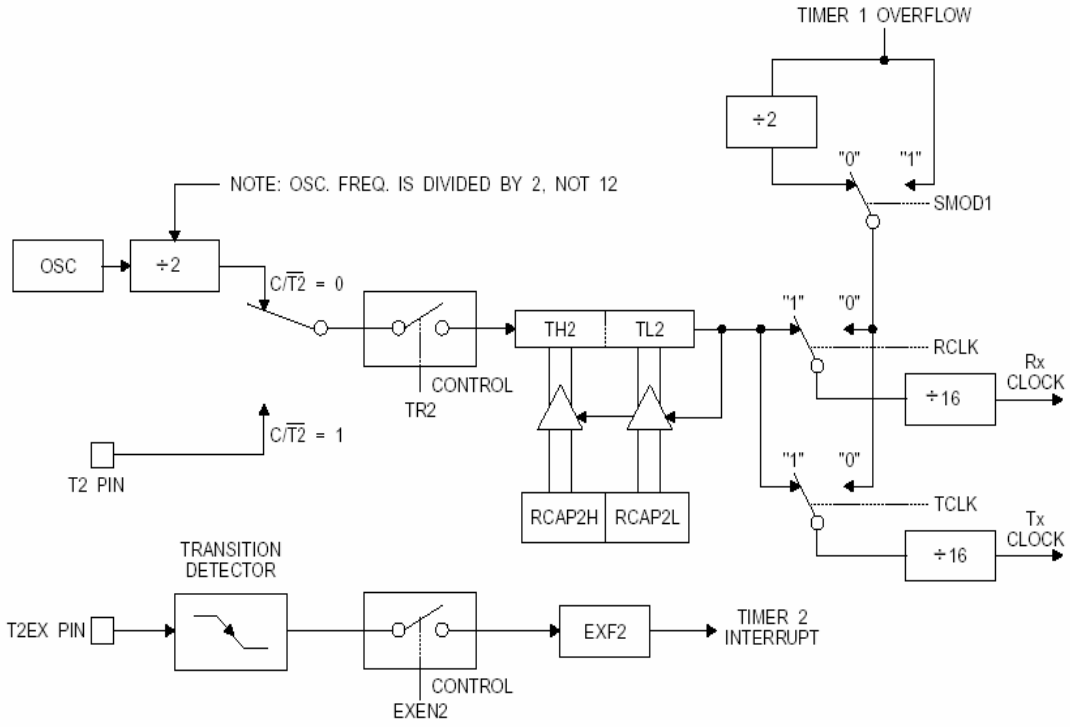


Figure 4. Timer 2 in Baud Rate Generator Mode



Baud Rate Generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Table 2). Note that the baud rates for transmit and receive can be different if Timer 2 is used for the receiver or transmitter and Timer 1 is used for the other function. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 4.

The baud rate generator mode is similar to the auto-reload mode, in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate according to the following equation.

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer can be configured for either timer or counter operation. In most applications, it is configured for timer operation (CP/$\overline{T2}$ = 0). The timer operation is different for Timer 2 when it is used as a baud rate generator. Normally, as a timer, it increments every machine cycle (at 1/12 the oscillator frequency). As a baud rate generator, however, it increments every state time (at 1/2 the oscillator frequency). The baud rate formula is given below.

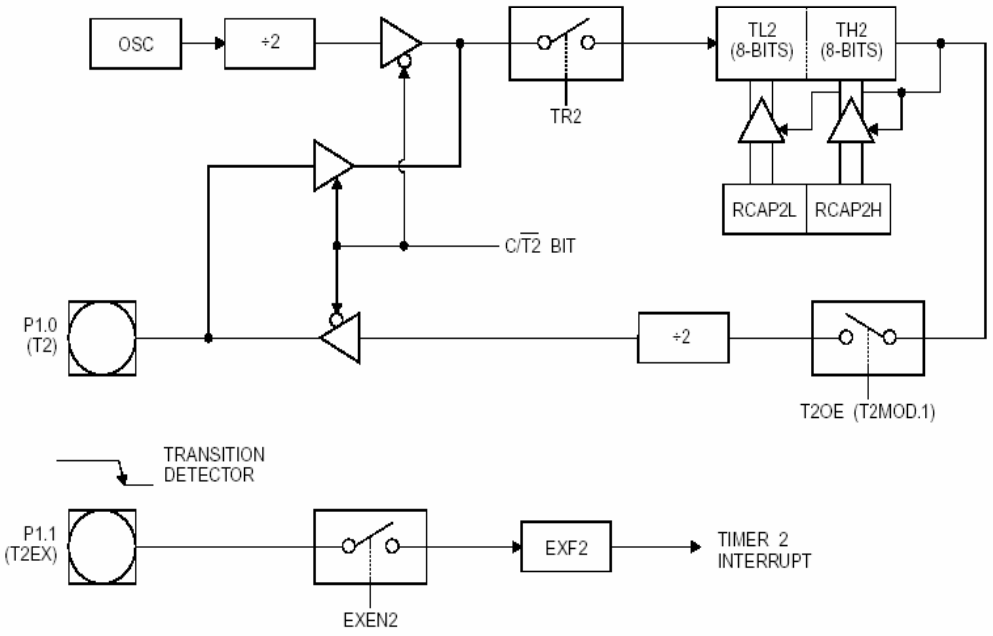
$$\frac{\text{Modes 1 and 3}}{\text{Baud Rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 4. This figure is valid only if RCLK or TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt.

Note that when Timer 2 is running (TR2 = 1) as a timer in the baud rate generator mode, TH2 or TL2 should not be read from or written to. Under these conditions, the Timer is incremented every state time, and the results of a read or write may not be accurate. The RCAP2 registers may be read but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Figure 5. Timer 2 in Clock-Out Mode



Programmable Clock Out

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ (T2CON.1) must be cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation.

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Fequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

The UART in the AT89C52 operates the same way as the UART in the AT89C51.

Interrupts

The AT89C52 has a total of six interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 5 shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

Table 5. Interrupt Enable (IE) Register

(MSB) (LSB)

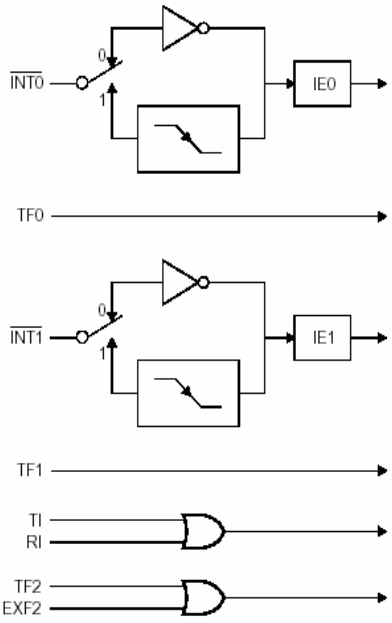
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Reserved.
ET2	IE.5	Timer 2 interrupt enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.
User software should never write 1s to unimplemented bits, because they may be used in future AT89 products.		

Figure 6. Interrupt Sources



Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 7. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 8. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

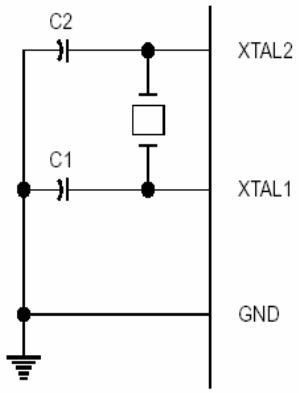
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

Power Down Mode

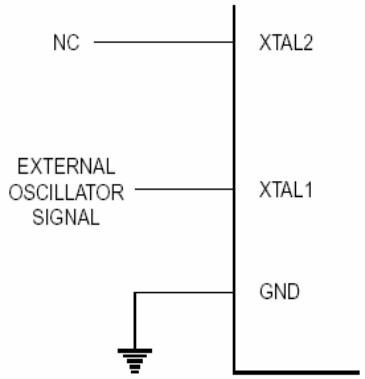
In the power down mode, the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Figure 7. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 8. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Program Memory Lock Bits

The AT89C52 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the following table.

Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled.
3	P	P	U	Same as mode 2, but verify is also disabled.
4	P	P	P	Same as mode 3, but external execution is also disabled.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

Programming the Flash

The AT89C52 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C52 inside the user's system, while the high-voltage programming mode is compatible with conventional third-party Flash or EPROM programmers.

The AT89C52 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C52 xxxx yyww	AT89C52 xxxx-5 yyww
Signature	(030H)=1EH (031H)=52H (032H)=FFH	(030H)=1EH (031H)=52H (032H)=05H

The AT89C52 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C52, the address, data and control signals should be set up according to the Flash programming mode table and Figures 9 and 10. To program the AT89C52, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C52 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on PO.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all 1s. The chip erase operation must be executed before the code memory can be reprogrammed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

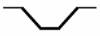
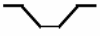
(030H) = 1EH indicates manufactured by Atmel
(031H) = 52H indicates 89C52
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written, and the entire array can be erased, by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms $\overline{PROG}$ pulse.

Figure 9. Programming the Flash Memory

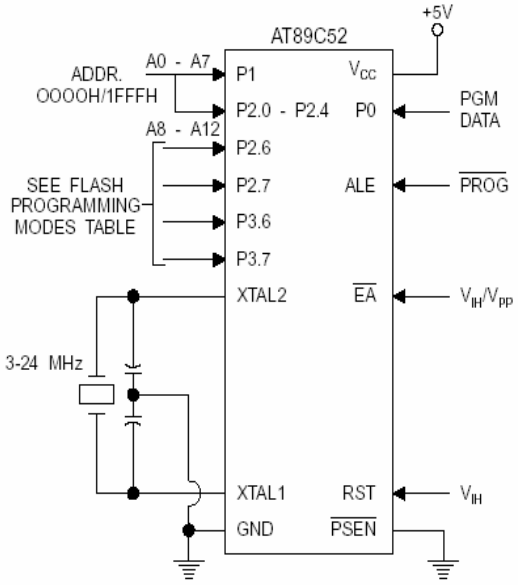
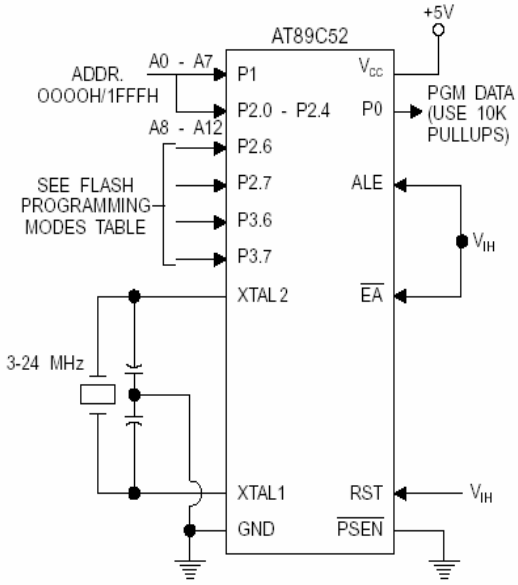


Figure 10. Verifying the Flash Memory



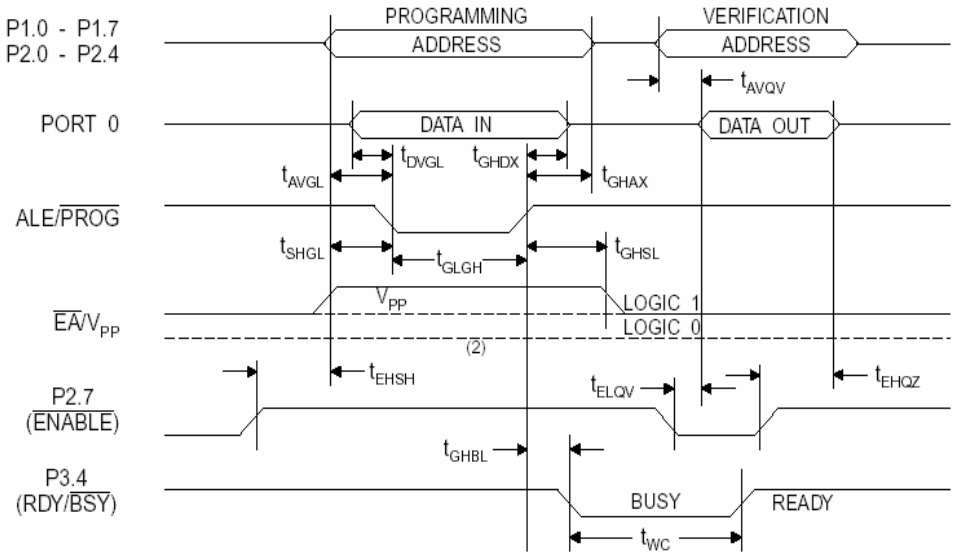
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

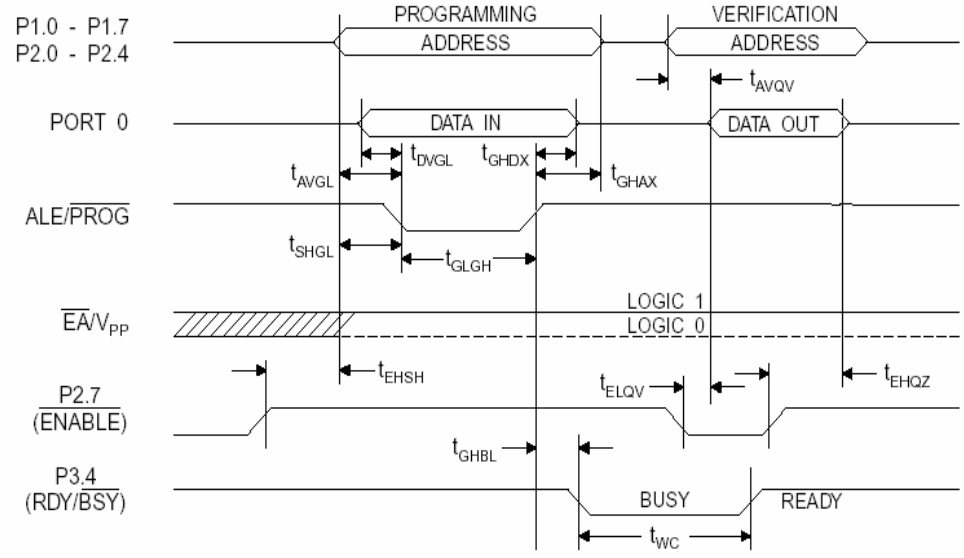
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP}=12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP}=5V)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = -40°C to 85°C and V_{CC} = 5.0V ± 20%, unless otherwise noted.

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC}-0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC}-0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC}+0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		25	mA
		Idle Mode, 12 MHz		6.5	mA
	Power Down Mode[1]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

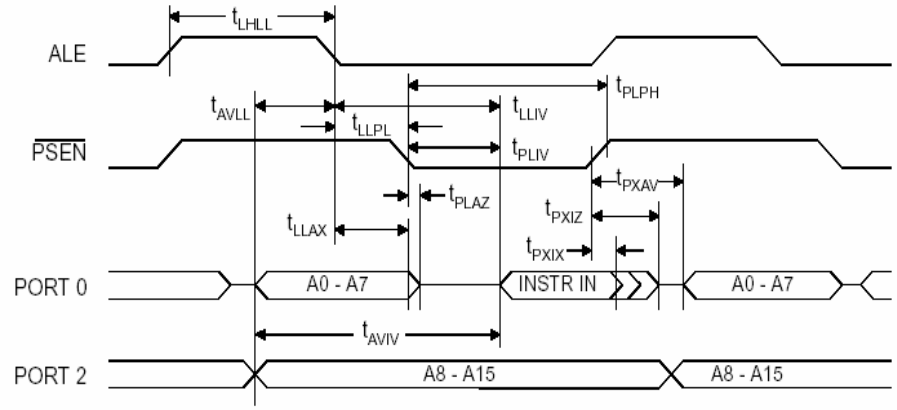
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

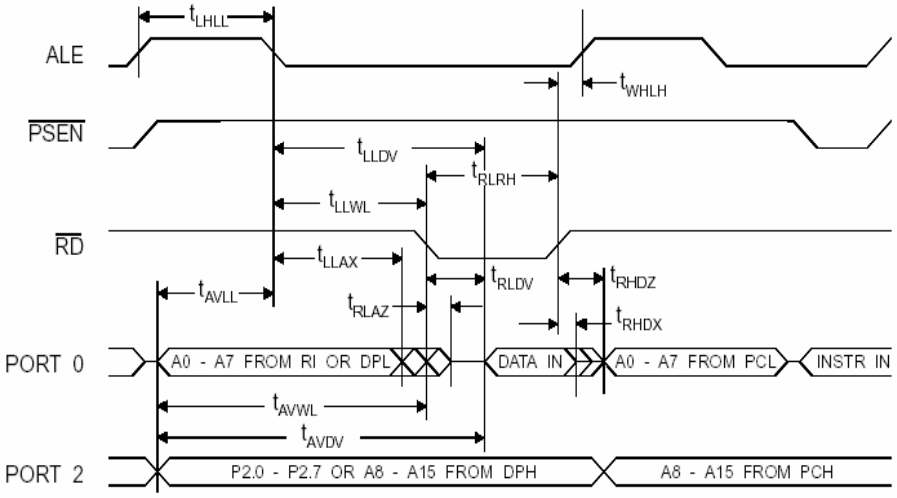
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

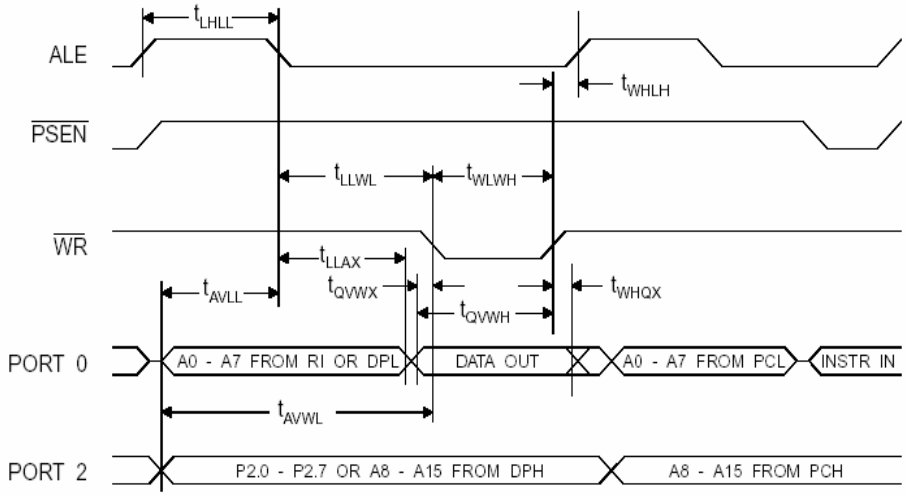
External Program Memory Read Cycle



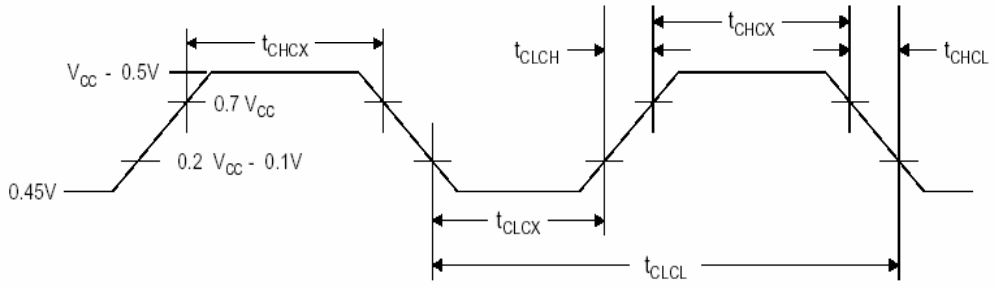
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

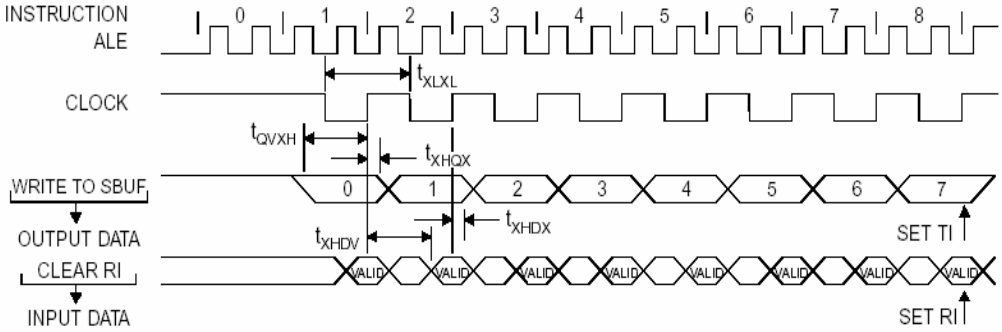
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

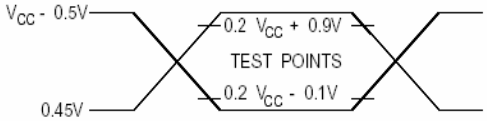
The values in this table are valid for V_{CC} = 5.0V ± 20% and Load Capacitance = 80 pF.

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

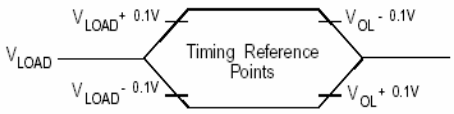


AC Testing Input/Output Waveforms(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C52-12AC AT89C52-12JC AT89C52-12PC AT89C52-12QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C52-12AI AT89C52-12JI AT89C52-12PI AT89C52-12QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
		AT89C52-12AA AT89C52-12JA AT89C52-12PA AT89C52-12QA	44A 44J 40P6 44Q	Automotive (-40°C to 105°C)
16	5V ± 20%	AT89C52-16AC AT89C52-16JC AT89C52-16PC AT89C52-16QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C52-16AI AT89C52-16JI AT89C52-16PI AT89C52-16QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)
		AT89C52-16AA AT89C52-16JA AT89C52-16PA AT89C52-16QA	44A 44J 40P6 44Q	Automotive (-40°C to 105°C)
20	5V ± 20%	AT89C52-20AC AT89C52-20JC AT89C52-20PC AT89C52-20QC	44A 44J 40P6 44Q	Commercial (0°C to 70°C)
		AT89C52-20AI AT89C52-20JI AT89C52-20PI AT89C52-20QI	44A 44J 40P6 44Q	Industrial (-40°C to 85°C)

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C52-24AC	44A	Commercial (0°C to 70°C)
		AT89C52-24JC	44J	
		AT89C52-24PC	40P6	
		AT89C52-24QC	44Q	
		AT89C52-24AI	44A	Industrial (-40°C to 85°C)
		AT89C52-24JI	44J	
		AT89C52-24PI	40P6	
		AT89C52-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

National Semiconductor

June 1999

DAC0800/DAC0802
8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

Typical Applications

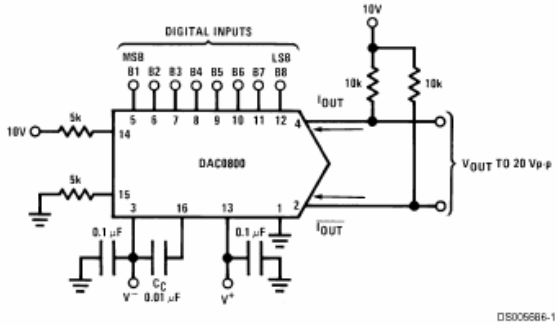


FIGURE 1. ±20 V_{P-P} Output Digital-to-Analog Converter (Note 5)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A) (Note 1)		N Package (N16E) (Note 1)		SO Package (M16A)
±0.1% FS	0°C ≤ T_A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C ≤ T_A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	±18V or 36V
Power Dissipation (Note 3)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus 36V
Analog Current Outputs (V_S- = −15V)	4.25 mA
ESD Susceptibility (Note 4)	TBD V
Storage Temperature	−65˚C to +150˚C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260˚C
Dual-In-Line Package (ceramic)	300˚C
Surface Mount Package	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C

Operating Conditions (Note 2)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	−55	+125	˚C
DAC0800LC	0	+70	˚C
DAC0802LC	0	+70	˚C

Electrical Characteristics

The following specifications apply for V_S = ±15V, I_{REF} = 2 mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				±0.1			±0.19	%FS
t_s	Settling Time	To ±½ LSB, All Bits Switched "ON" or "OFF", T_A=25˚C		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
tPLH, tPHL	Propagation Delay	T_A=25˚C							
	Each Bit			35	60		35	60	ns
	All Bits Switched			35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			±10	±50		±10	±50	ppm/˚C
V_{OC}	Output Voltage Compliance	Full Scale Current Change <½ LSB, R_{OUT}>20 MΩ Typ	−10		18	−10		18	V
I_{FS4}	Full Scale Current	V_{REF}=10.000V, R14=5.000 kΩ R15=5.000 kΩ, T_A=25˚C	1.984	1.992	2.000	1.94	1.99	2.04	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4}-I_{FS2}$		±0.5	±4.0		±1	±8.0	µA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0	µA
I_{FSR}	Output Current Range	V^-=−5V	0	2.0	2.1	0	2.0	2.1	mA
		V^-=−8V to −18V	0	2.0	4.2	0	2.0	4.2	mA
	Logic Input Levels								
V_{IL}	Logic "0"	V_{LC}=0V			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			V
	Logic Input Current	V_{LC}=0V							
I_{IL}	Logic "0"	−10V≤V_{IN}≤+0.8V		−2.0	−10		−2.0	−10	µA
I_{IH}	Logic "1"	2V≤V_{IN}≤+18V		0.002	10		0.002	10	µA
V_{IS}	Logic Input Swing	V^-=−15V	−10		18	−10		18	V
V_{THR}	Logic Threshold Range	V_S=±15V	−10		13.5	−10		13.5	V
I_{15}	Reference Bias Current			−1.0	−3.0		−1.0	−3.0	µA
dI/dt	Reference Input Slew Rate	(*Figure 11*)	4.0	8.0		4.0	8.0		mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity	4.5V≤V^+≤18V		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$		−4.5V≤V^-≤18V I_{REF}=1mA		0.0001	0.01		0.0001	0.01	%/%

Electrical Characteristics (Continued)

The following specifications apply for V_S = ±15V, I_{REF} = 2 mA and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Power Supply Current	V_S=±5V, I_{REF}=1 mA							
I+				2.3	3.8		2.3	3.8	mA
I−				−4.3	−5.8		−4.3	−5.8	mA
		V_S=5V, −15V, I_{REF}=2 mA							
I+				2.4	3.8		2.4	3.8	mA
I−				−6.4	−7.8		−6.4	−7.8	mA
		V_S=±15V, I_{REF}=2 mA							
I+				2.5	3.8		2.5	3.8	mA
I−				−6.5	−7.8		−6.5	−7.8	mA
P_D	Power Dissipation	±5V, I_{REF}=1 mA		33	48		33	48	mW
		5V,−15V, I_{REF}=2 mA		108	136		108	136	mW
		±15V, I_{REF}=2 mA		135	174		135	174	mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

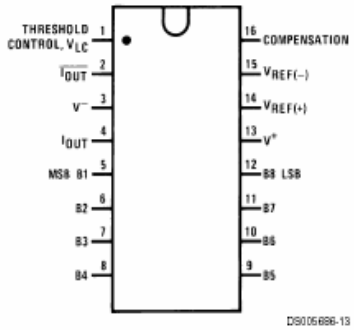
Note 3: The maximum junction temperature of the DAC0800 and DAC0802 is 125˚C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100˚C/W, junction-to-ambient, 175˚C/W for the molded Dual-In-Line N package and 100˚C/W for the Small Outline M package.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

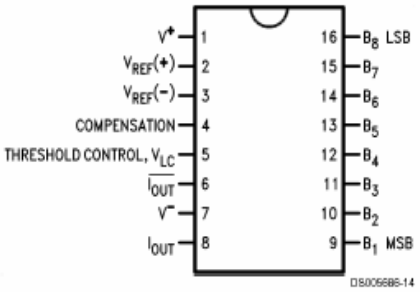
Connection Diagrams

Dual-In-Line Package



Top View

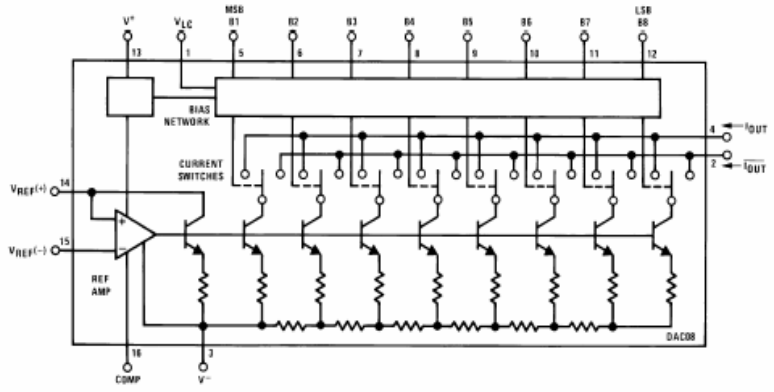
Small Outline Package



Top View

See Ordering Information

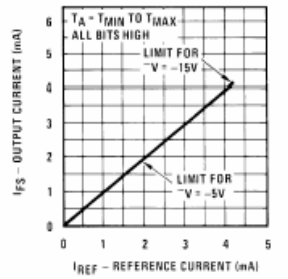
Block Diagram (Note 5)



DS005686-2

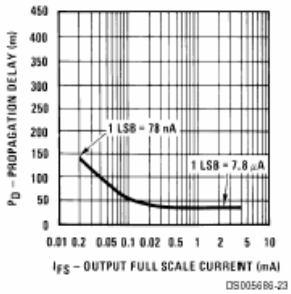
Typical Performance Characteristics

Full Scale Current vs Reference Current



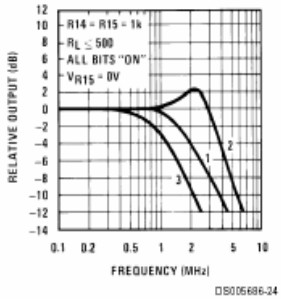
DS005686-22

LSB Propagation Delay vs I_{FS}



DS005686-23

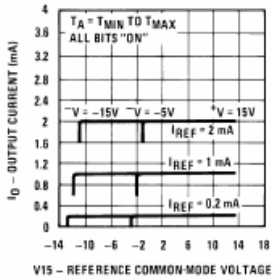
Reference Input Frequency Response



DS005686-24

Curve 1: C_C = 15 pF, V_{IN} = 2 Vp-p centered at 1V.
Curve 2: C_C = 15 pF, V_{IN} = 50 mVp-p centered at 200 mV.
Curve 3: C_C = 0 pF, V_{IN} = 100 mVp-p centered at 0V and applied through 50Ω connected to pin 14.2V applied to R14.

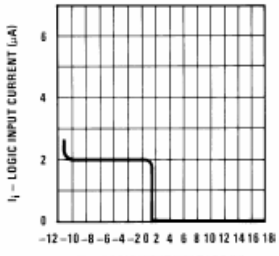
Reference Amp Common-Mode Range



DS005686-25

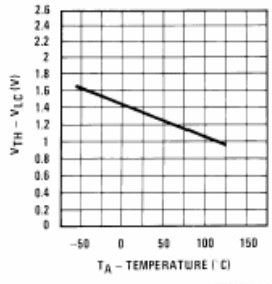
Note. Positive common-mode range is always (V+) − 1.5V.

Logic Input Current vs Input Voltage



DS005686-26

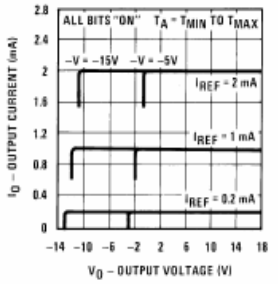
V_{TH} — V_{LC} vs Temperature



DS005686-27

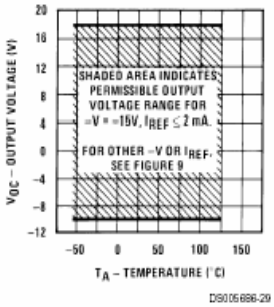
Typical Performance Characteristics (Continued)

Output Current vs Output Voltage (Output Voltage Compliance)



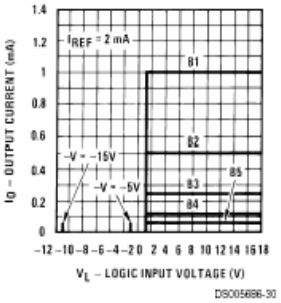
DS005686-28

Output Voltage Compliance vs Temperature



DS005686-29

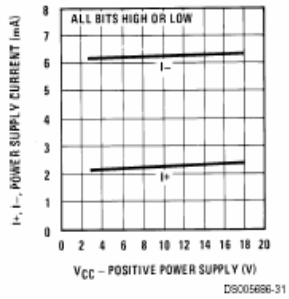
Bit Transfer Characteristics



DS005686-30

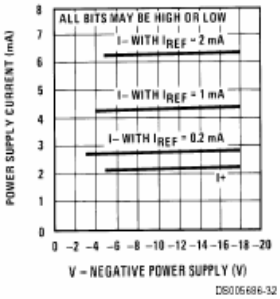
Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range (V_{LC} = 0V).

Power Supply Current vs +V



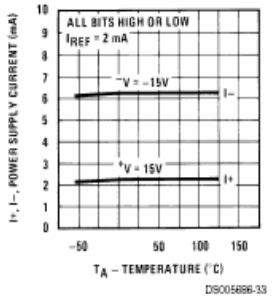
DS005686-31

Power Supply Current vs −V



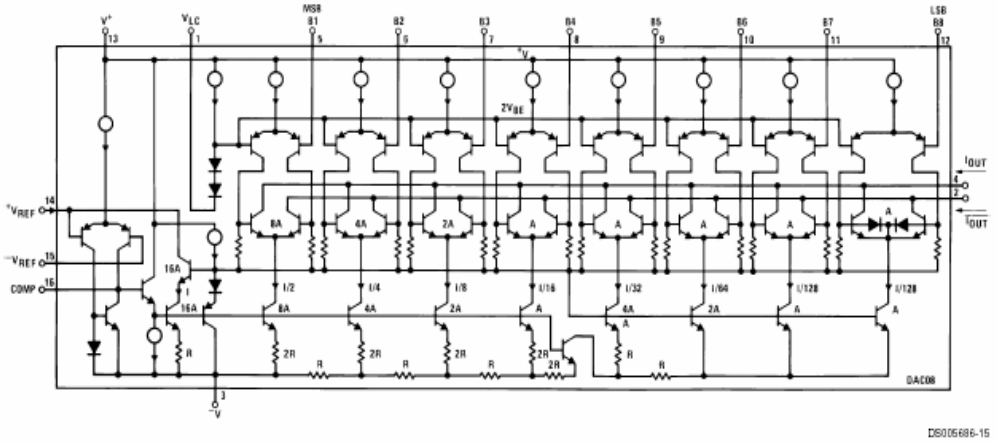
DS005686-32

Power Supply Current vs Temperature



DS005686-33

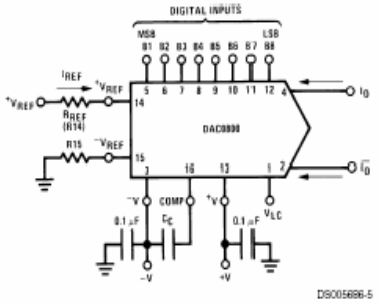
Equivalent Circuit



DS005686-15

FIGURE 2.

Typical Applications



$$I_{FS} \simeq \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I}_O = I_{FS}$ for all logic states
For fixed reference, TTL operation, typical values are:
V_{REF} = 10.000V
R_{REF} = 5.000k
R15 ≃ R_{REF}
C_C = 0.01 μF
V_{LC} = 0V (Ground)

FIGURE 3. Basic Positive Reference Operation (Note 5)

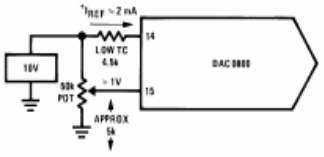
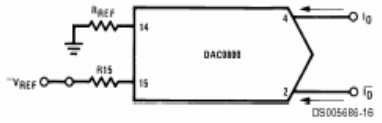


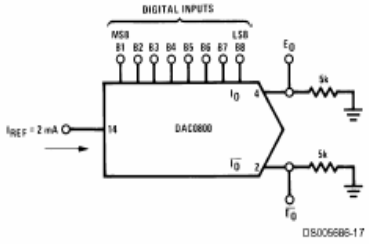
FIGURE 4. Recommended Full Scale Adjustment Circuit (Note 5)



$$I_{FS} \simeq \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note. R_{REF} sets I_{FS}; R15 is for bias current cancellation

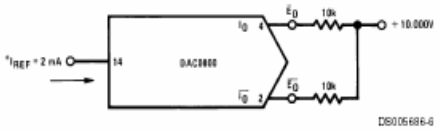
FIGURE 5. Basic Negative Reference Operation (Note 5)



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I}_O$mA	E_O	$\overline{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale−LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

FIGURE 6. Basic Unipolar Negative Operation (Note 5)

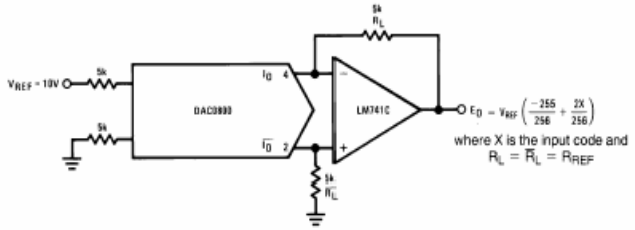
Typical Applications (Continued)



DS005686-6

	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E}_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale−LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

FIGURE 7. Basic Bipolar Output Operation (Note 5)

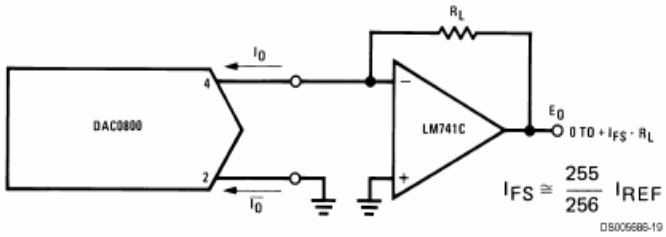


DS005686-18

If $R_L = \overline{R}_L$ within ±0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale−LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−)Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	−9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.960

FIGURE 8. Symmetrical Offset Binary Operation (Note 5)

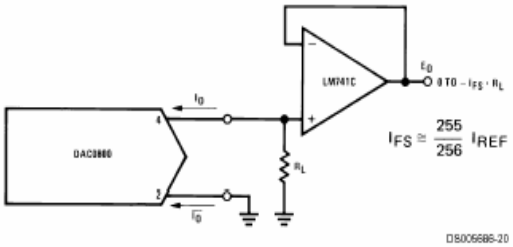


DS005686-19

For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I}_O$ (pin 2), connect I_O (pin 4) to ground.

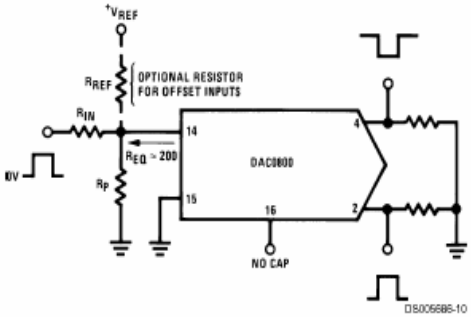
FIGURE 9. Positive Low Impedance Output Operation (Note 5)

Typical Applications (Continued)



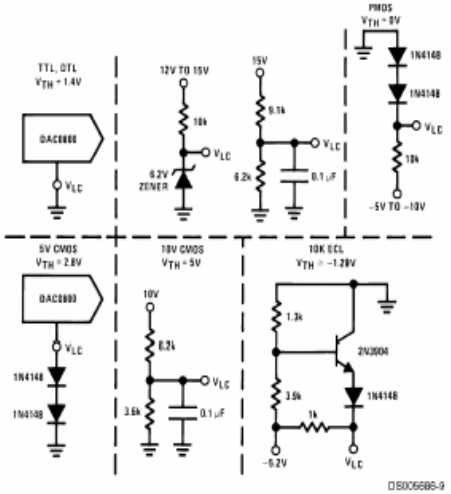
For complementary output (operation as a negative logic DAC) connect non-inverting input of op amp to $\overline{I_O}$ (pin 2); connect I_O (pin 4) to ground.

FIGURE 10. Negative Low Impedance Output Operation (Note 5)



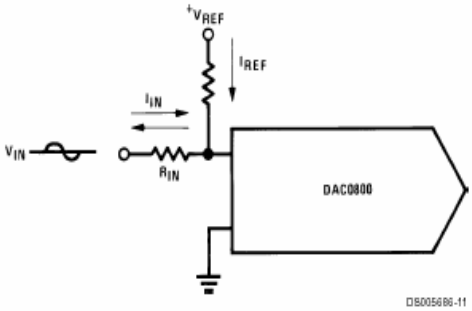
Typical values: $R_{IN}=5k, +V_{IN}=10V$

FIGURE 11. Pulsed Reference Operation (Note 5)

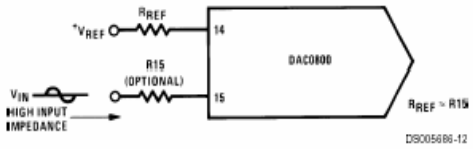


$V_{TH} = V_{LC} + 1.4V$
15V CMOS, HTL, HNIL
$V_{TH} = 7.6V$
Note. Do not exceed negative logic input range of DAC.

FIGURE 12. Interfacing with Various Logic Families



(a) $I_{REF} \geq$ peak negative swing of I_{IN}



(b) $+V_{REF}$ must be above peak positive swing of V_{IN}

FIGURE 13. Accommodating Bipolar References (Note 5)

Typical Applications (Continued)

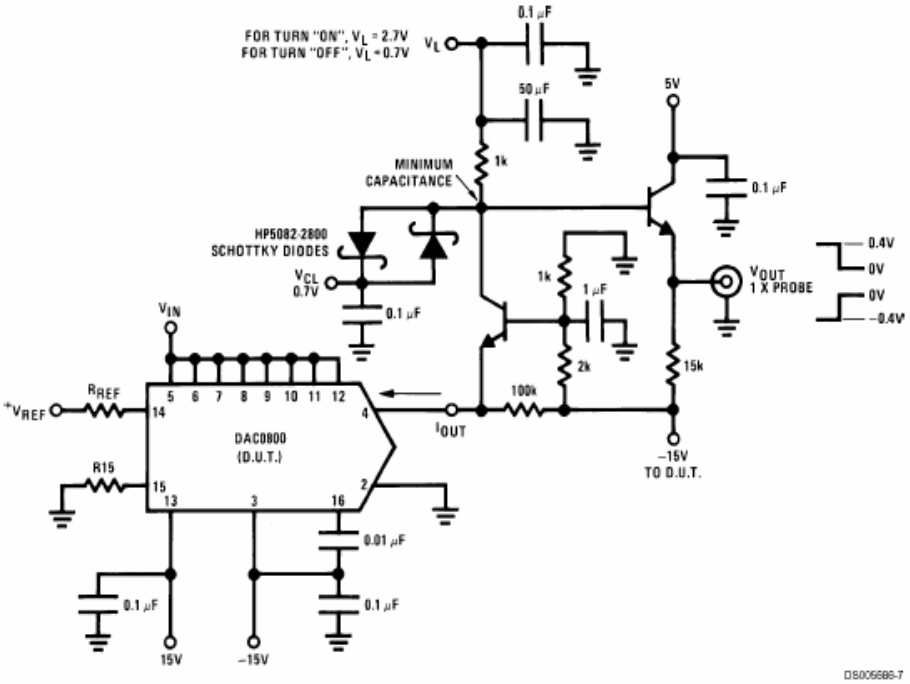
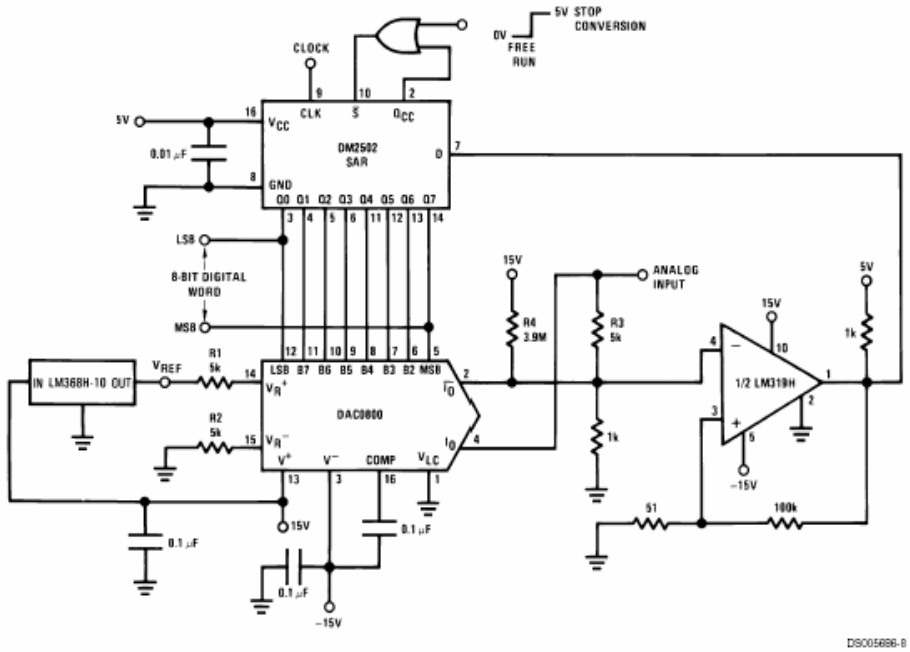


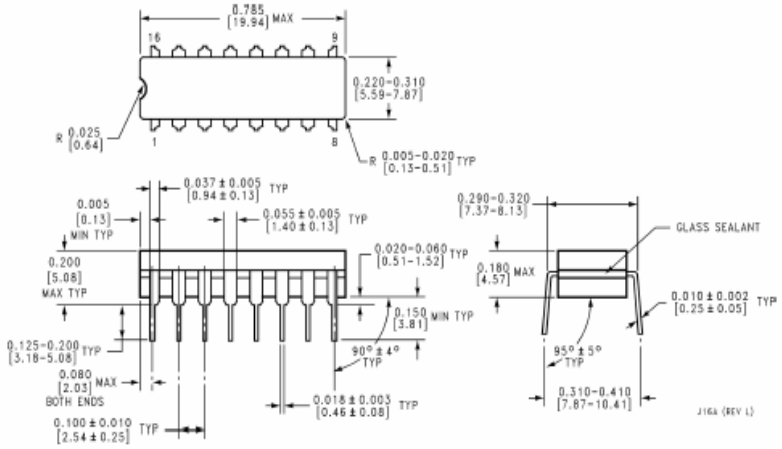
FIGURE 14. Settling Time Measurement (Note 5)



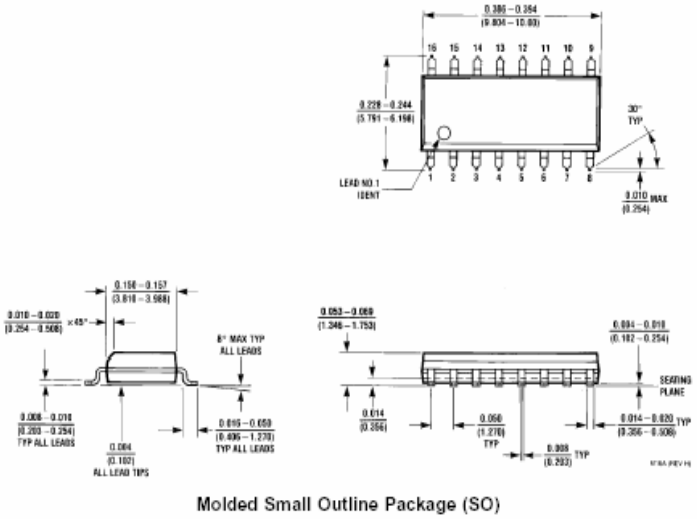
Note. For 1 µs conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 kΩ and R4 to 2 MΩ.

FIGURE 15. A Complete 2 µs Conversion Time, 8-Bit A/D Converter (Note 5)

Physical Dimensions inches (millimeters) unless otherwise noted

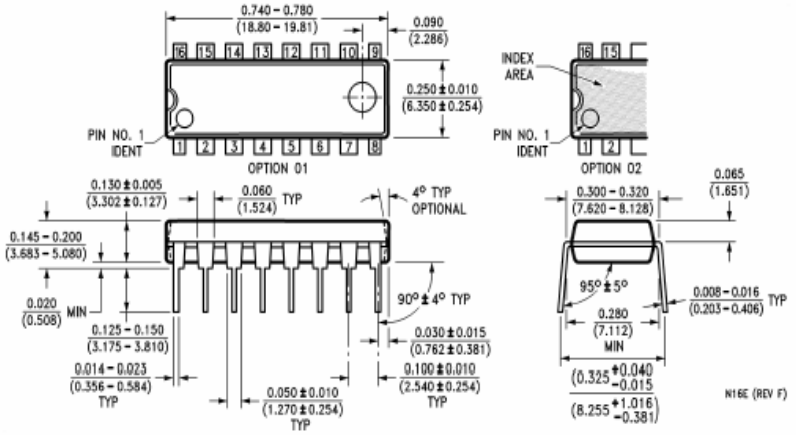


Molded Small Outline Package (SO)
Order Numbers DAC0800LCM,
or DAC0802LCM
NS Package Number M16A



Molded Small Outline Package (SO)
Order Numbers DAC0800LCM,
or DAC0802LCM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package
Order Numbers DAC0800, DAC0802
NS Package Number N16E

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Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor
Asia Pacific Customer
Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor
Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

15 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion 0.003% Typ
- Low Noise V_n = 18 nV/$\sqrt{Hz}$ Typ at f = 1 kHz
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description

The JFET-input operational amplifiers in the TL07_ series are designed as low-noise versions of the TL08_ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07_ series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

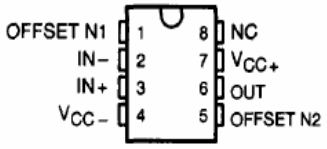
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C.

AVAILABLE OPTIONS

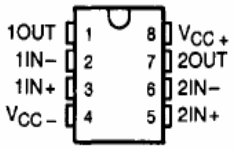
T_A	V_{IO}max AT 25°C	PACKAGE							
		SMALL OUTLINE (D)†	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP PACKAGE (PW)	FLAT PACKAGE (W)
0°C to 70°C	10 mV	TL071CD	—	—	—	—	TL071CP	TL071CPWLE	—
	6 mV	TL071ACD					TL071ACP	—	
	3 mV	TL071BCD					TL071BCP	—	
	10 mV	TL072CD	—	—	—	—	TL072CP	TL072CPWLE	—
	6 mV	TL072ACD					TL072ACP	—	
	3 mV	TL072BCD					TL072BCP	—	
	10 mV	TL074CD	—	—	—	TL074CN	—	TL074CPWLE	—
	6 mV	TL074ACD				TL074ACN		—	
	3 mV	TL074BCD				TL074BCN		—	
−40°C to 85°C	6 mV	TL071ID	—	—	—	—	TL071IP	—	—
		TL072ID				—	TL072P		
		TL074ID				TL074IN	—		
−55°C to 125°C	6 mV	—	TL071MFK	—	TL071MJG	—	—	—	—
	6 mV		TL072MFK	—	TL072MJG				—
	9 mV		TL074MFK	TL074MJ	—				TL074MW

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR). The PW package is only available left-ended taped and reeled (e.g., TL072CPWLE).

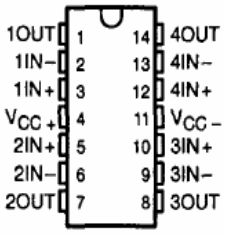
TL071, TL071A, TL071B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



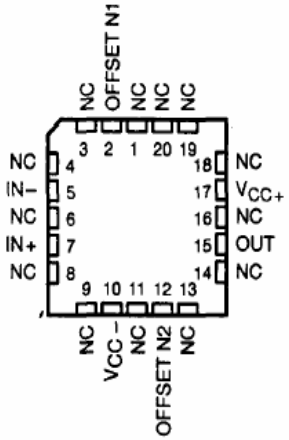
TL072, TL072A, TL072B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



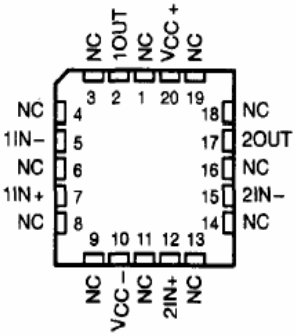
TL074, TL074A, TL074B
D, J, N, OR PW PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



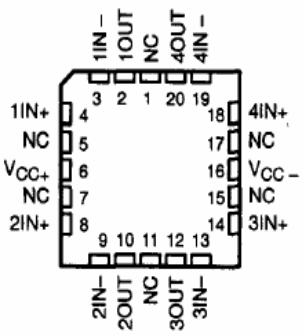
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



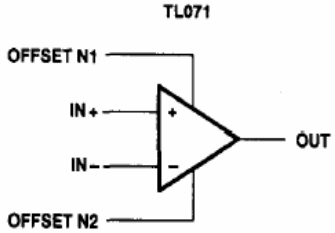
TL074
FK PACKAGE
(TOP VIEW)



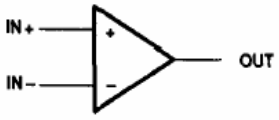
NC – No internal connection

symbols

TL071



TL072 (each amplifier)
TL074 (each amplifier)



TEXAS INSTRUMENTS
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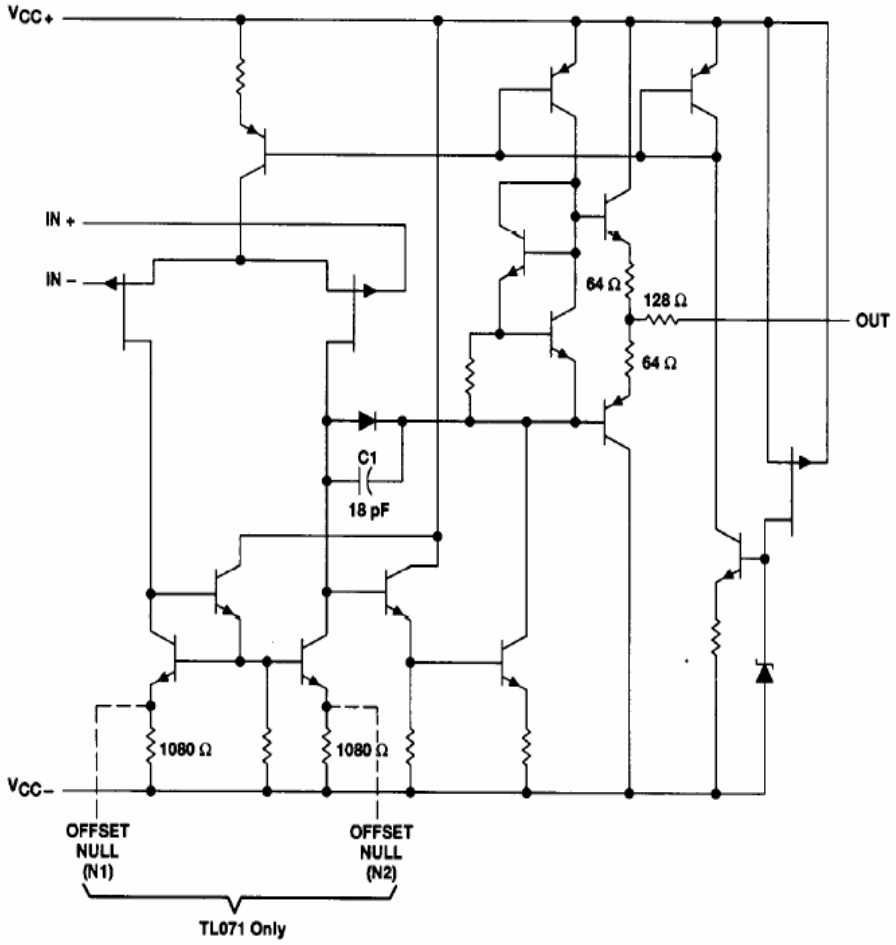
schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	18 V
Supply voltage, V_{CC-} (see Note 1)	−18 V
Differential input voltage, V_{ID} (see Note 2)	±30 V
Input voltage, V_I (see Notes 1 and 3)	±15 V
Duration of output short-circuit (see Note 4)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 85°C
M suffix	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, P, or PW package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	70°C	525 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	70°C	700 mW	N/A	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	10		3	6		2	3		3	6	mV
			Full range			13			7.5			5			8	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100		5	100		5	100	pA
			Full range			10			2			2			2	nA
I_{IB}	Input bias current§	V_O = 0	25°C		65	200		65	200		65	200		65	200	pA
			Full range			7			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
			Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	100		75	100		75	100		75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	70	100		80	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Full range is T_A = 0°C to 70°C for TL07_C, TL07_AC, TL07_BC and is T_A = −40°C to 85°C for TL07_I.
§ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A‡	TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			Full range			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		65	200		65	200	pA
						50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
				15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is T_A = −55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07xM			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	5	13		8	13		V/μs
t_r	Rise time overshoot factor	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
					20%			20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(RMS)}$ = 10 V, $R_L \geq 2$ kΩ,	$R_S \leq 1$ kΩ, f = 1 kHz		0.003%			0.003%		

PARAMETER MEASUREMENT INFORMATION

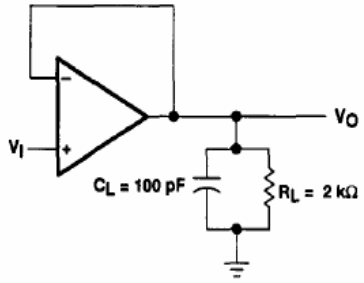


Figure 1. Unity-Gain Amplifier

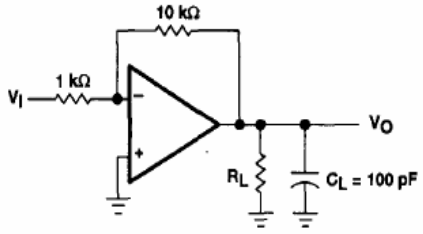


Figure 2. Gain-of-10 Inverting Amplifier

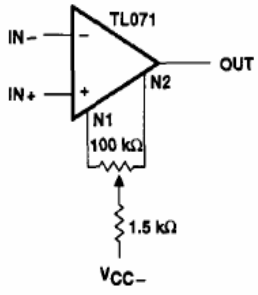


Figure 3. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	4
V_{OM}	Maximum output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
CMRR	Common-mode rejection ratio	vs Free-air temperature	14
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	15 16
P_D	Total power dissipation	vs Free-air temperature	17
	Normalized slew rate	vs Free-air temperature	18
V_n	Equivalent input noise voltage	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20
	Large-signal pulse response	vs Time	21
V_O	Output voltage	vs Time	22

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

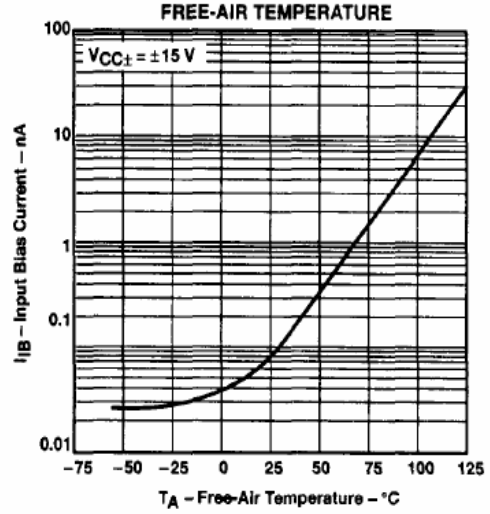


Figure 4

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

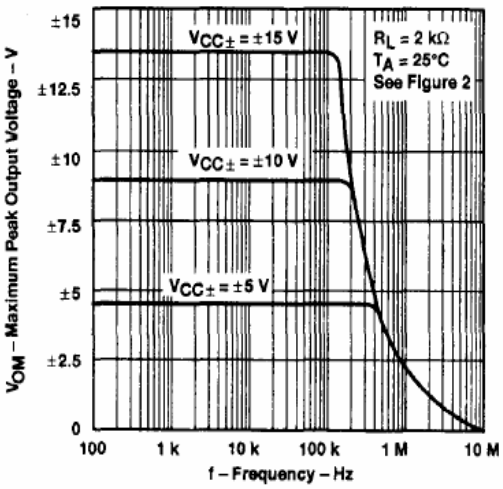


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

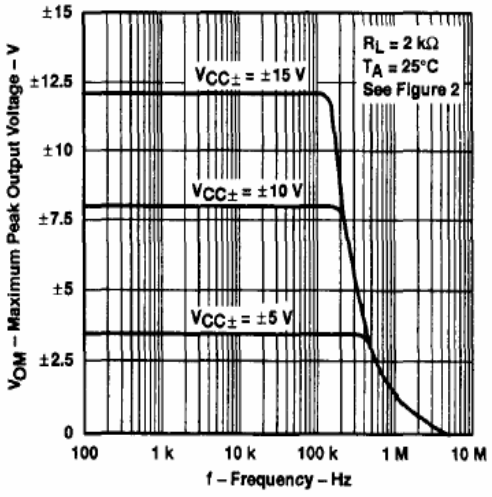


Figure 6

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

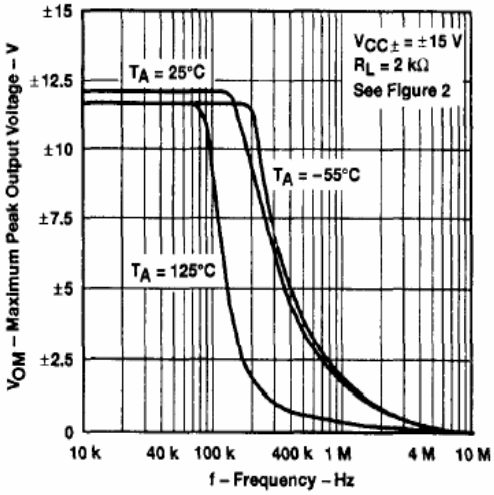


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

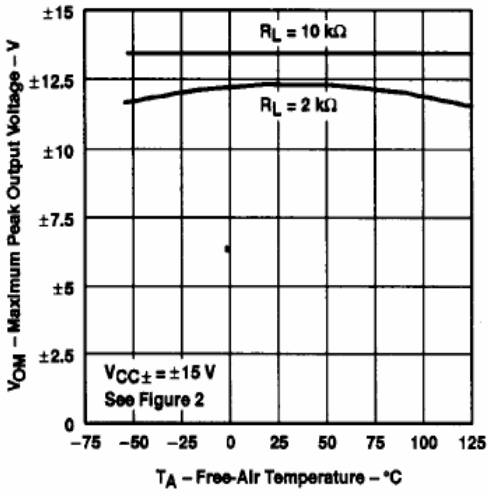


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

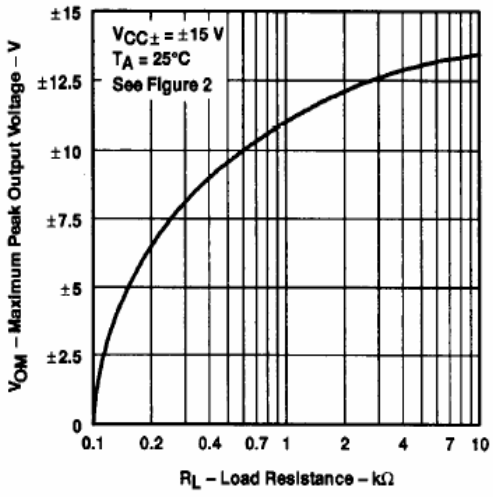


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

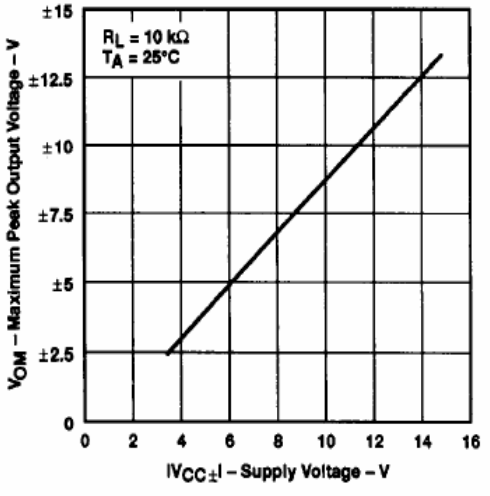


Figure 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

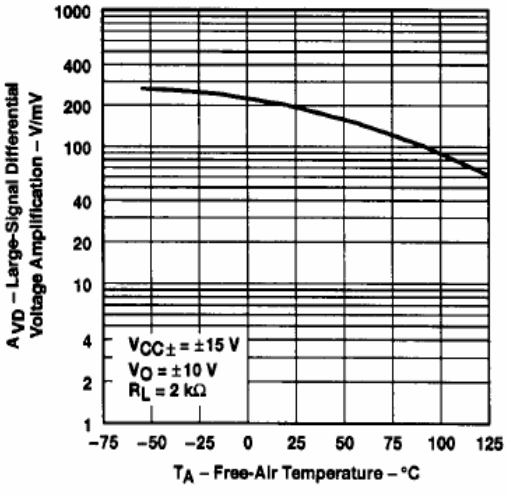


Figure 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

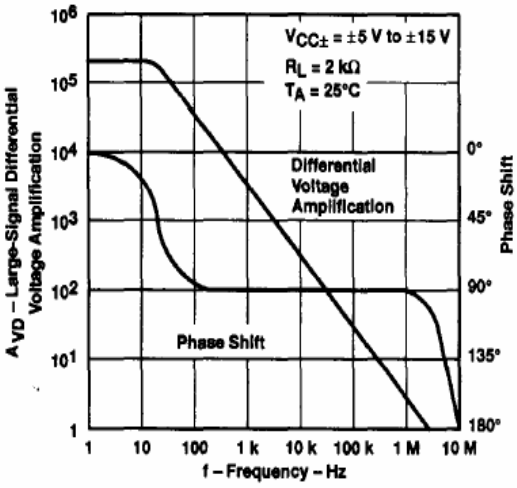


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH AND PHASE SHIFT vs FREE-AIR TEMPERATURE

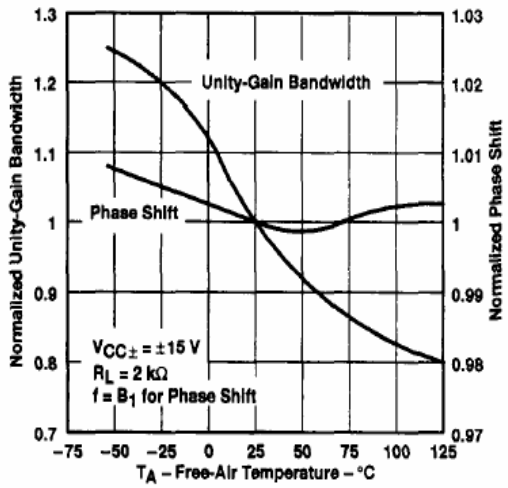


Figure 13

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

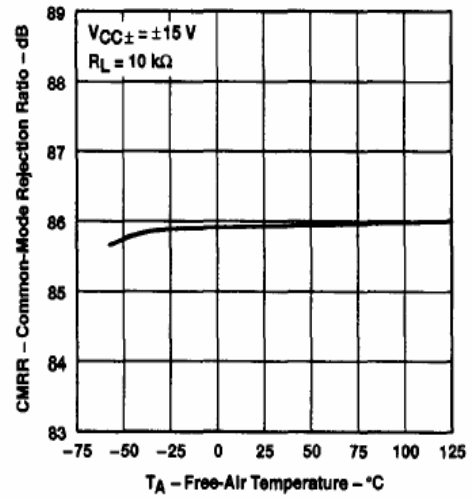


Figure 14

SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

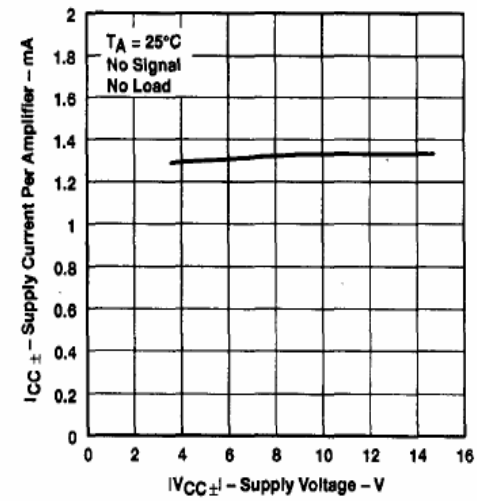


Figure 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

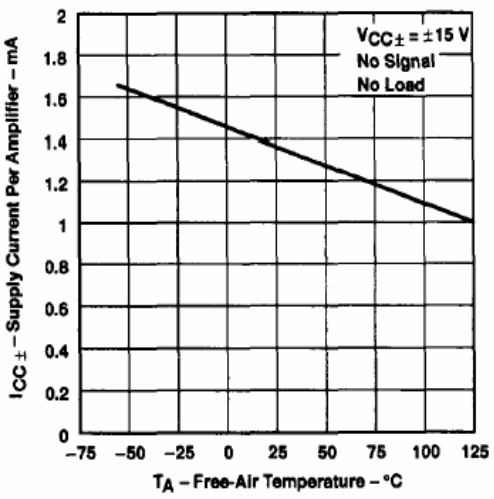


Figure 16

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

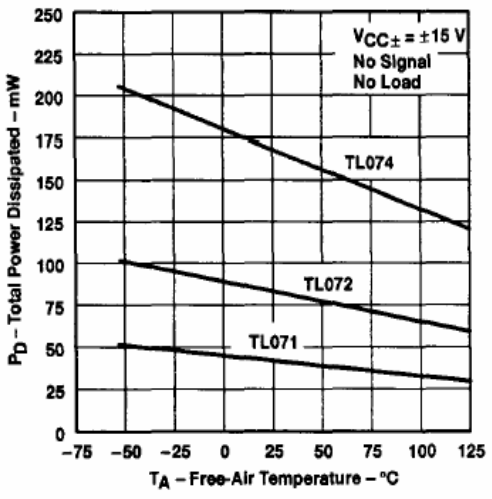


Figure 17

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

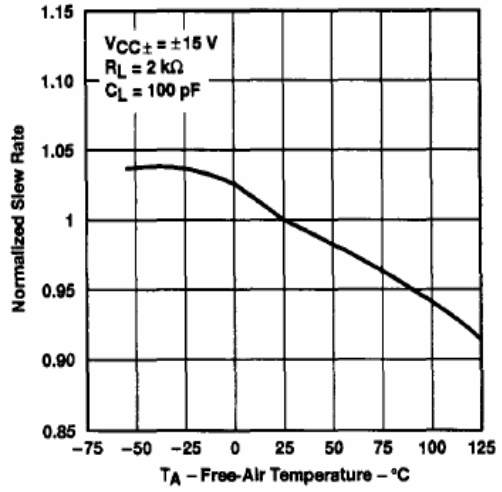


Figure 18

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

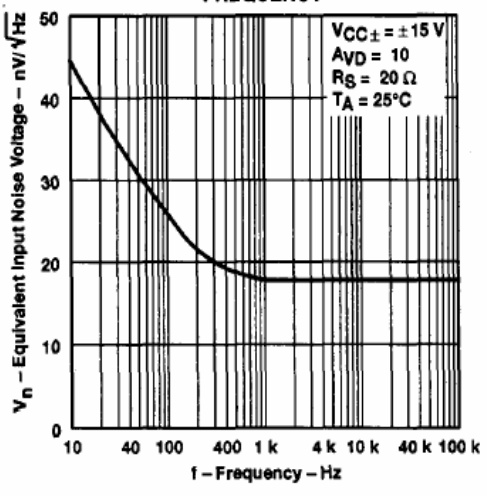


Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs FREQUENCY

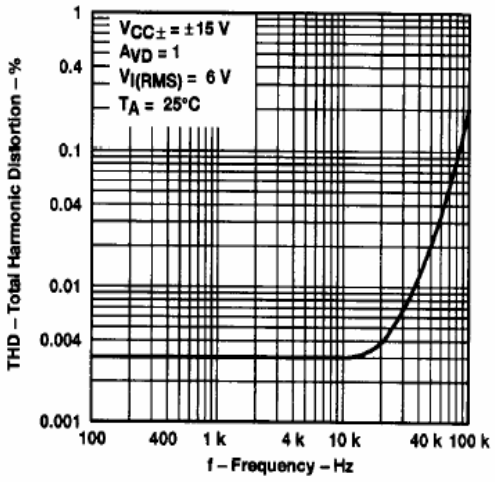


Figure 20

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

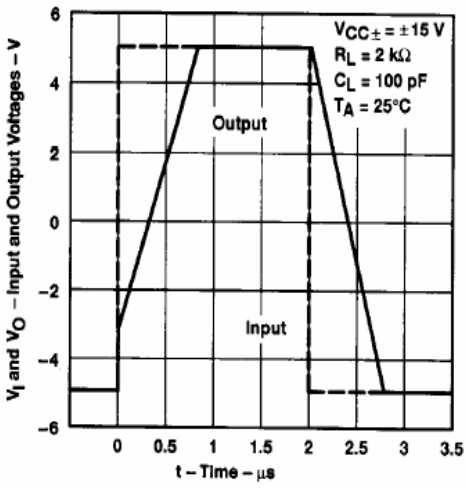


Figure 21

OUTPUT VOLTAGE vs ELAPSED TIME

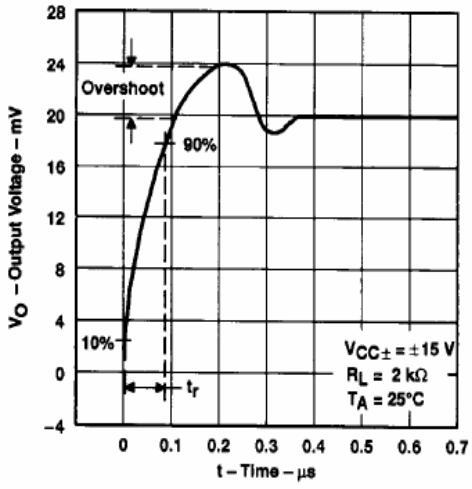


Figure 22

APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

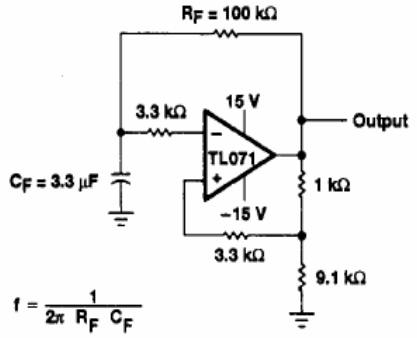


Figure 23. 0.5-Hz Square-Wave Oscillator

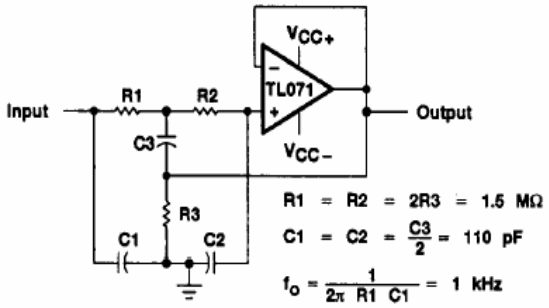


Figure 24. High-Q Notch Filter

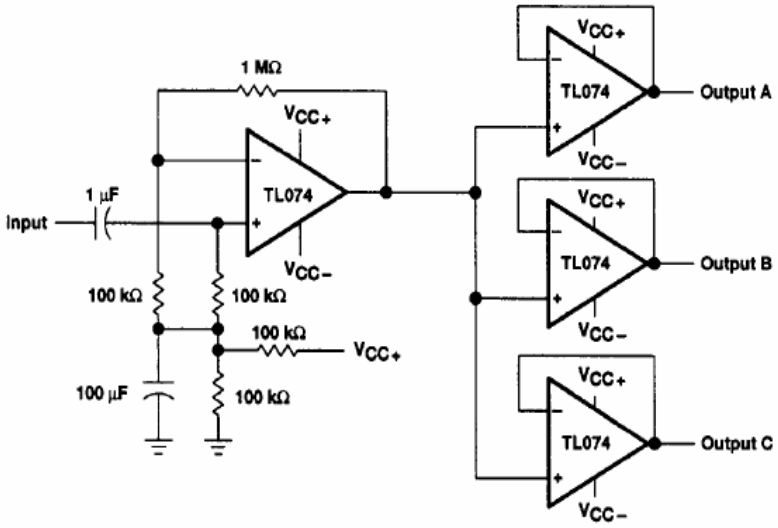
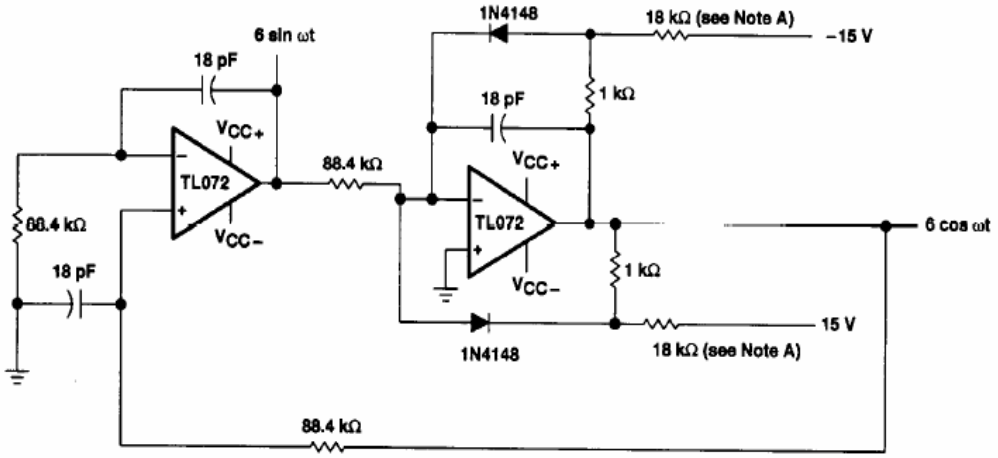


Figure 25. Audio-Distribution Amplifier

APPLICATION INFORMATION



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-kHz Quadrature Oscillator

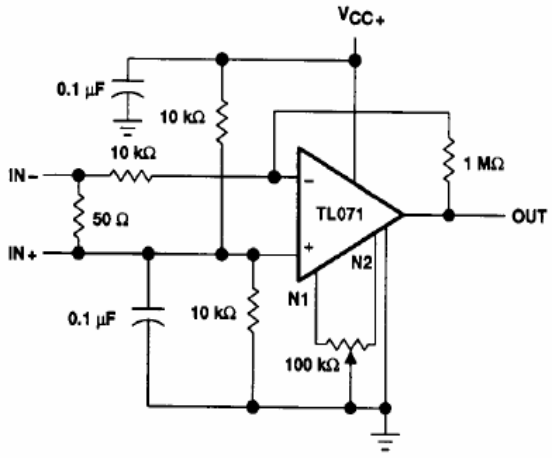


Figure 27. AC Amplifier

TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- High Input Impedance . . . JFET-Input Stage
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

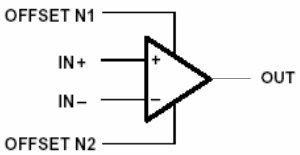
description

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

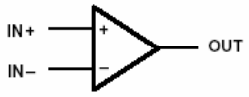
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

symbols

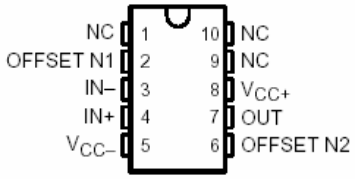
TL081



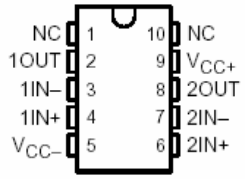
TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)



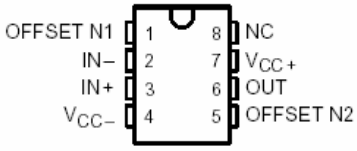
TL081M
U PACKAGE
(TOP VIEW)



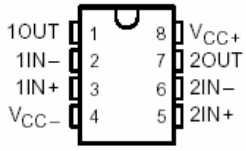
TL082M
U PACKAGE
(TOP VIEW)



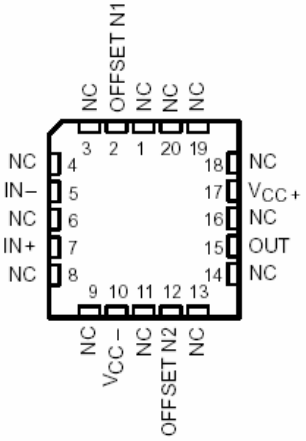
TL081, TL081A, TL081B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



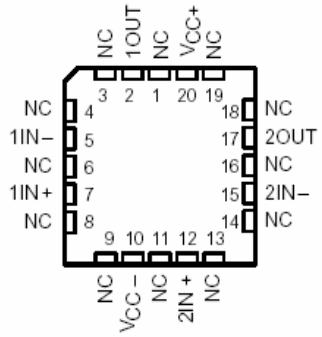
TL082, TL082A, TL082B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



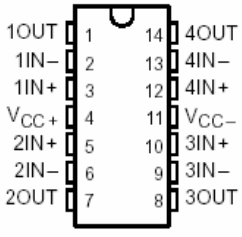
TL081M . . . FK PACKAGE
(TOP VIEW)



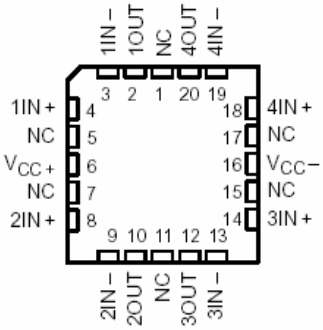
TL082M . . . FK PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, PW, OR W PACKAGE
(TOP VIEW)



TL084M . . . FK PACKAGE
(TOP VIEW)



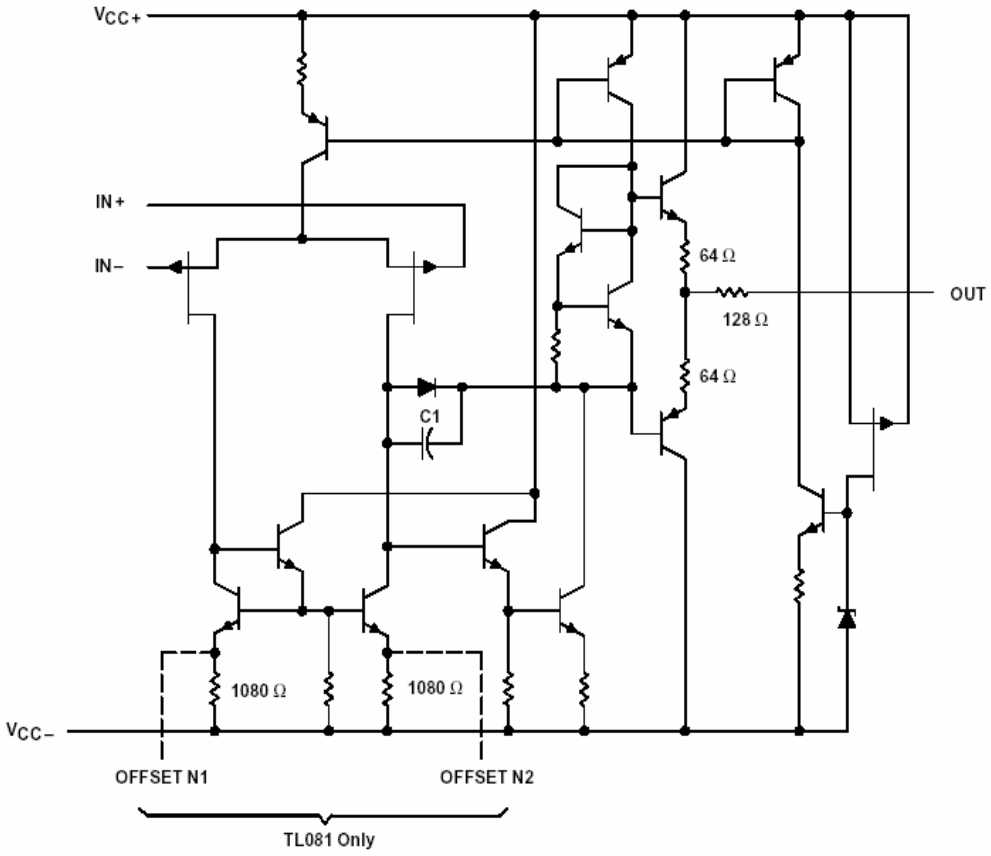
NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES										CHIP FORM (Y)
		SMALL OUTLINE (D008)	SMALL OUTLINE (D014)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	FLAT PACK (W)	
0°C to 70°C	15 mV	TL081CD	—	—	—	—	—	TL081CP	TL081CPW	—	—	—
	6 mV	TL081ACD						TL081ACP				
	3 mV	TL081BCD						TL081BCP				
	15 mV	TL082CD	—	—	—	—	—	TL082CP	TL082CPW	—	—	TL082Y
	6 mV	TL082ACD						TL082ACP				
	3 mV	TL082BCD						TL082BCP				
	15 mV	—	TL084CD	—	—	—	TL084CN	—	TL084CPW	—	—	TL084Y
	6 mV		TL084ACD				TL084ACN					
	3 mV		TL084BCD				TL084BCN					
−40°C to 85°C	6 mV	TL081ID	—	—	—	—	TL084IN	TL081IP	—	—	—	—
	6 mV	TL082ID						TL082IP				
	6 mV	TL084ID	TL084ID									
−40°C to 125°C	9 mV	—	TL084QD	—	—	—	—	—	—	—	—	—
−55°C to 125°C	6 mV	—	—	TL081MFK	TL084MJ	TL081MJG	—	—	—	TL081MU	TL084MW	—
	6 mV			TL082MFK		TL082MJG				TL082MU		
	9 mV			TL084MFK								

The D package is available taped and reeled. Add R suffix to the device type (e.g., TL081CDR).

schematic (each amplifier)

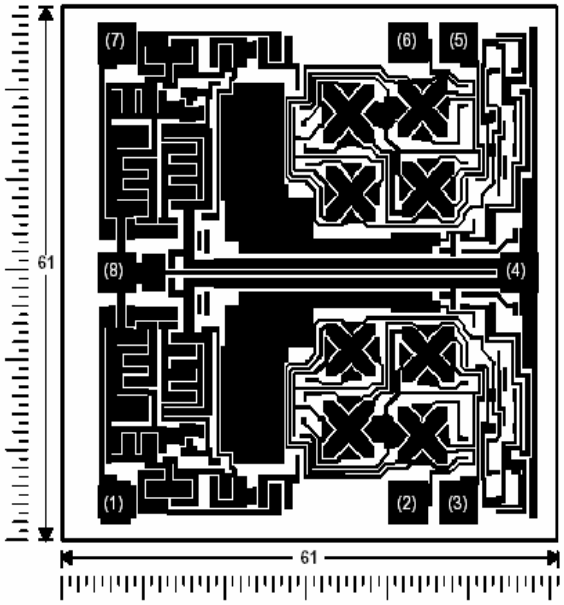


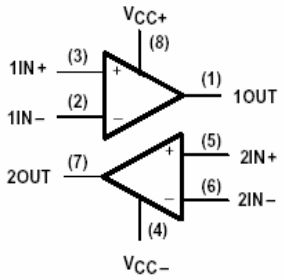
Component values shown are nominal.

TL082Y chip information

These chips, when properly assembled, display characteristics similar to the TL082. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ± 10%.

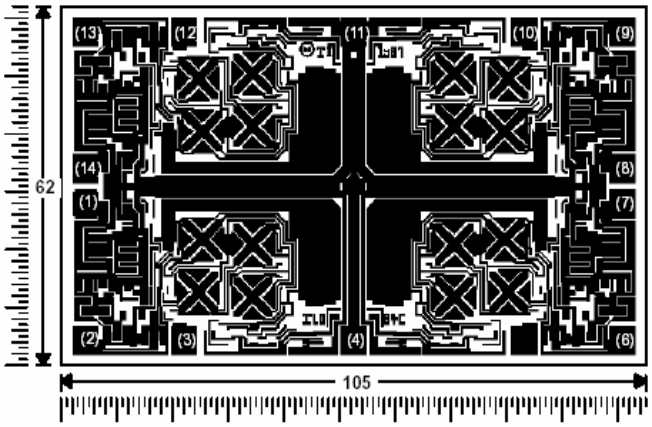
ALL DIMENSIONS ARE IN MILS.

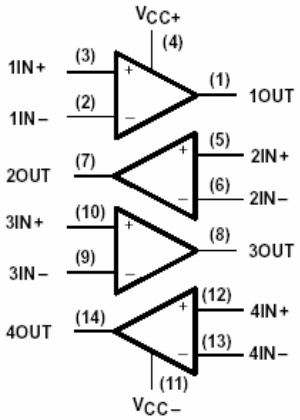
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL084Y chip information

These chips, when properly assembled, display characteristics similar to the TL084. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	18	V
Supply voltage V_{CC-} (see Note 1)		–18	–18	–18	–18	V
Differential input voltage, V_{ID} (see Note 2)		± 30	± 30	± 30	± 30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table				
Operating free-air temperature range, T_A		0 to 70	– 40 to 85	– 40 to 125	– 55 to 125	°C
Storage temperature range, T_{stg}		– 65 to 150	– 65 to 150	– 65 to 150	– 65 to 150	°C
Case temperature for 60 seconds, T_C	FK package				260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package				300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, P, or PW package	260	260	260		°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	32°C	460 mW	373 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	25°C	448 mW	N/A	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 mW	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TL081C, TL082C, TL084C			TL081AC, TL082AC, TL084AC			TL081BC, TL082BC, TL084BC			TL081I, TL082I, TL084I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
				Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0	R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current‡	V_O = 0		25°C		5	200		5	100		5	100		5	100	pA
				Full range			2			2			2			10	nA
I_{IB}	Input bias current‡	V_O = 0		25°C		30	400		30	200		30	200		30	200	pA
				Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range			25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ		Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ			±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
		V_O = ±10 V,	R_L ≥ 2 kΩ	Full range	15			25			25			25			
B_1	Unity-gain bandwidth			25°C		3			3			3			3		MHz
r_i	Input resistance			25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0,	R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0,	R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB
I_{OC}	Supply current (per amplifier)	V_O = 0,	No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and −40°C to 85°C for TL08_I.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0 R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current‡	V_O = 0	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	±12 to 15		±11	±12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		25	200		V/mV
		V_O = ±10 V, R_L ≥ 2 kΩ	Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		8*	13		V/µs
		V_I = 10 V, T_A = –55°C to 125°C, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		5*			
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1			0.05		µs
	Overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	R_S = 20 Ω, f = 1 kHz			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, f = 1 kHz, A_{VD} = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ,			0.003%		

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

electrical characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL082Y, TL084Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω		3	15	mV
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω		18		µV/°C
I_{IO}	Input offset current‡	V_O = 0,		5	200	pA
I_{IB}	Input bias current‡	V_O = 0,		30	400	pA
V_{ICR}	Common-mode input voltage range		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,	±12	±13.5		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25	200		V/mV
B_1	Unity-gain bandwidth			3		MHz
r_i	Input resistance			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	70 70	86 86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	70 70	86 86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0, No load		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		8	13		V/µs
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1			0.05		µs
	Overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		µV
I_n	Equivalent input noise current	R_S = 20 Ω, f = 1 kHz			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, f = 1 kHz	A_{VD} = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ,		0.003%		

PARAMETER MEASUREMENT INFORMATION

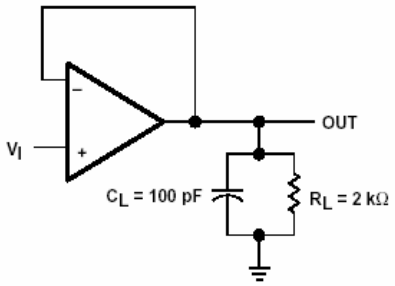


Figure 1

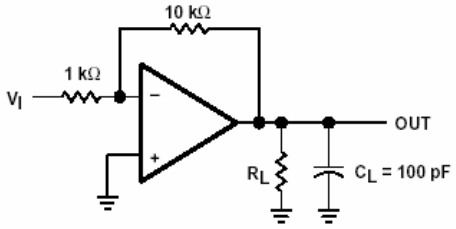


Figure 2

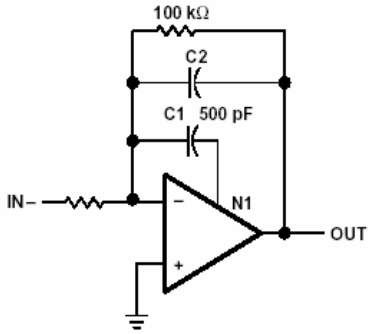


Figure 3

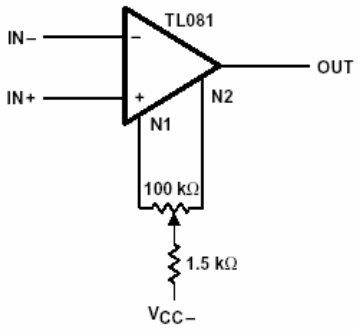


Figure 4

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Differential voltage amplification	vs Frequency with feed-forward compensation	13
P_D	Total power dissipation	vs Free-air temperature	14
I_{CC}	Supply current	vs Free-air temperature vs Supply voltage	15 16
I_{IB}	Input bias current	vs Free-air temperature	17
	Large-signal pulse response	vs Time	18
V_O	Output voltage	vs Elapsed time	19
CMRR	Common-mode rejection ratio	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD	Total harmonic distortion	vs Frequency	22

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

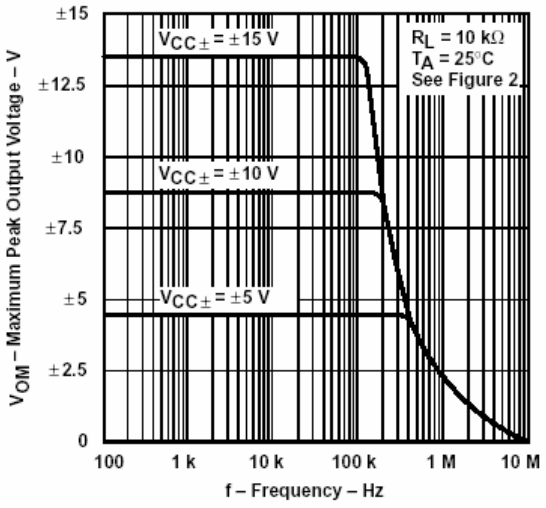


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

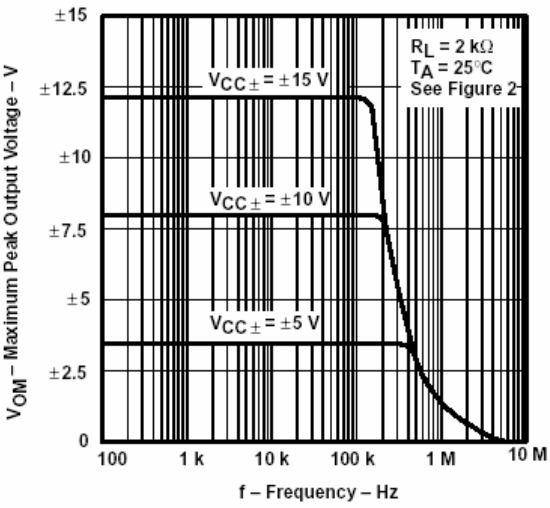


Figure 6

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

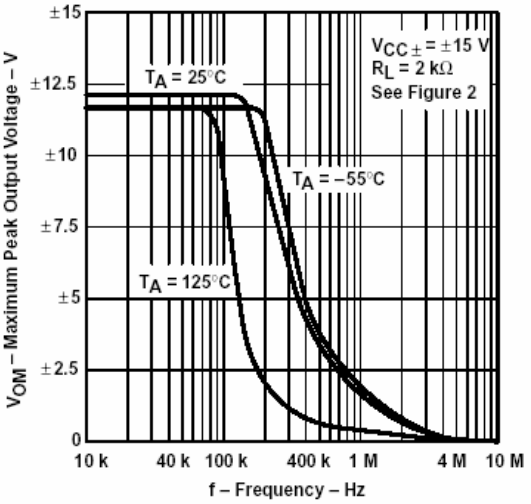


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

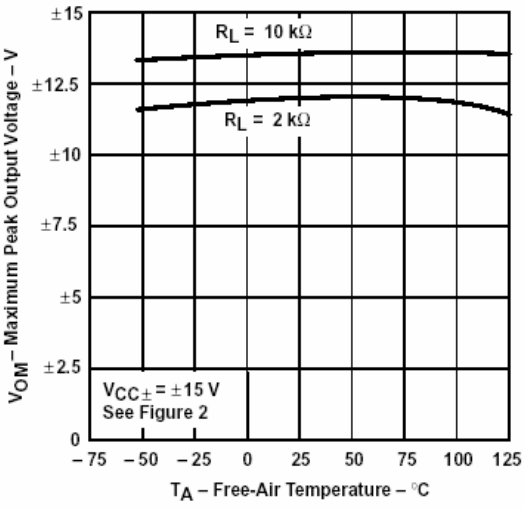


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

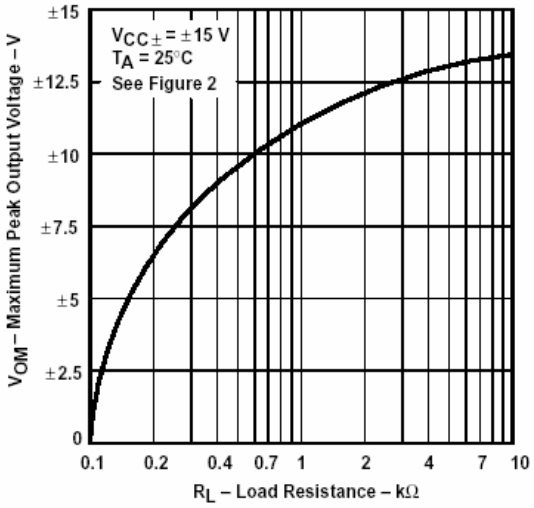


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

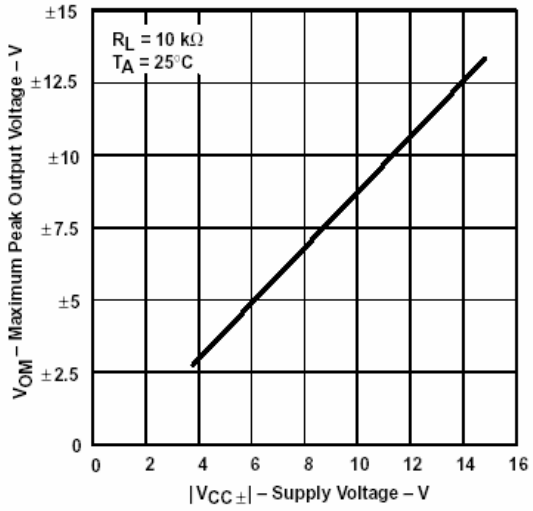


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

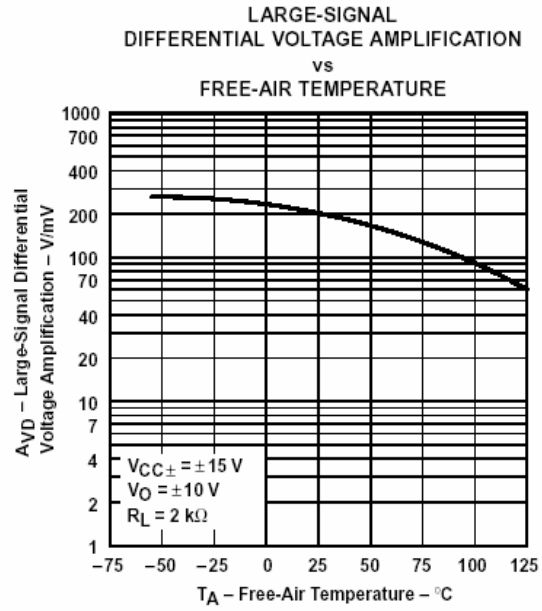


Figure 11

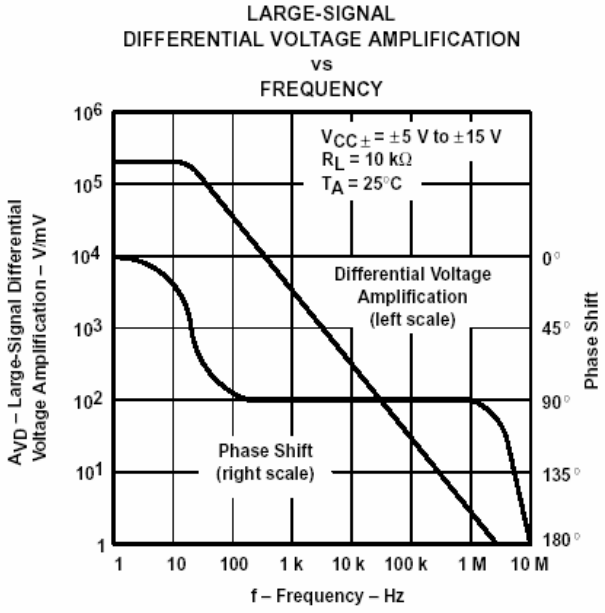


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION

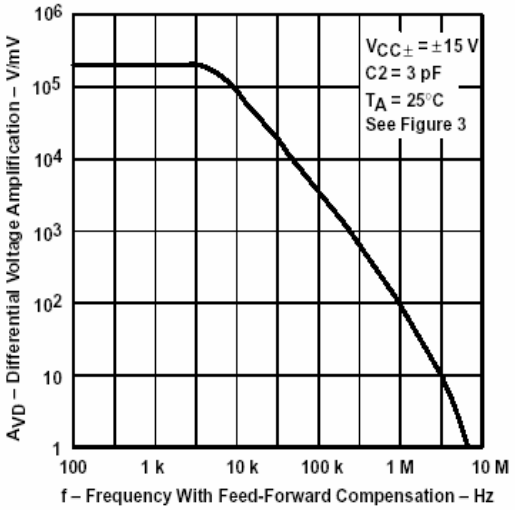


Figure 13

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

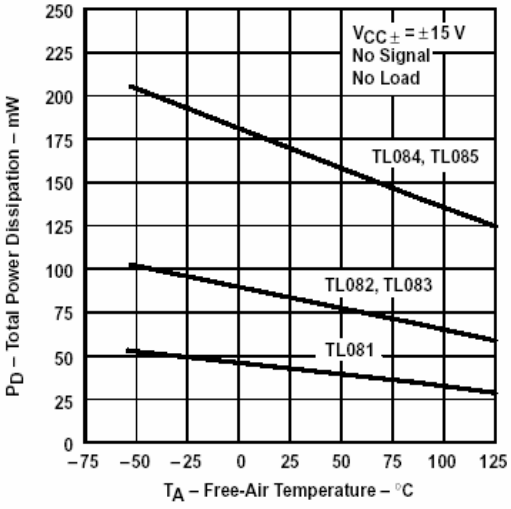


Figure 14

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

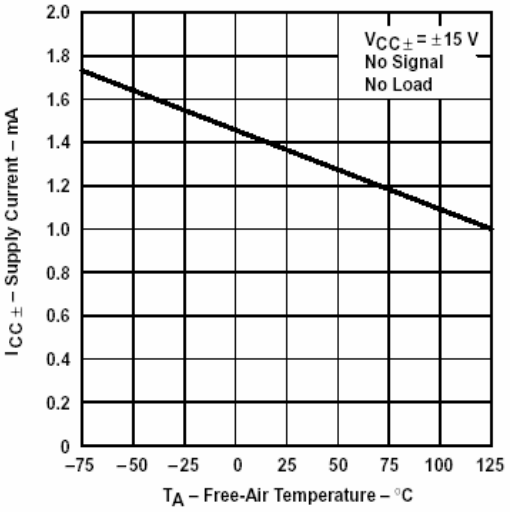


Figure 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

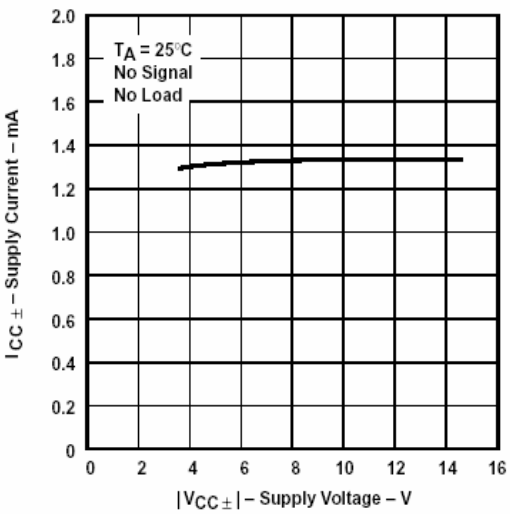


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

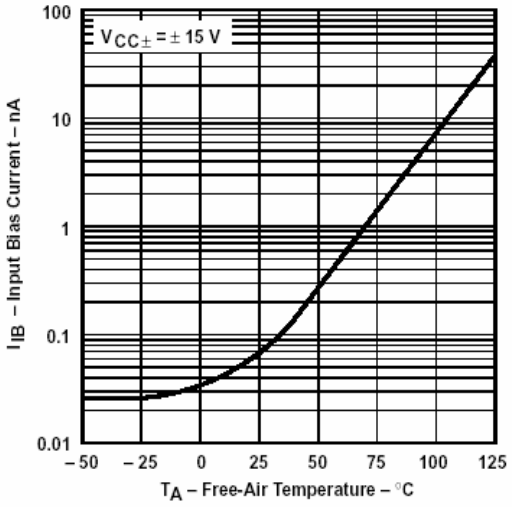


Figure 17

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

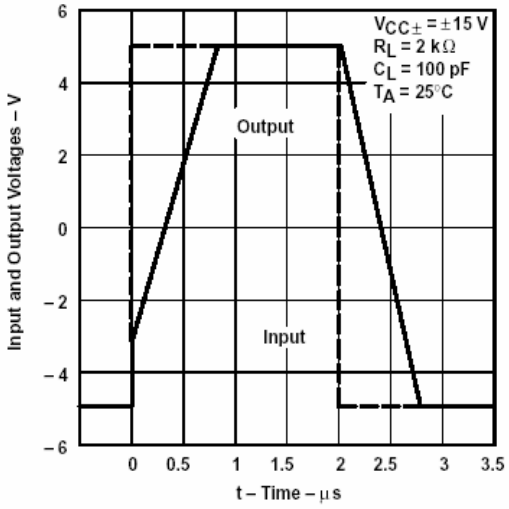


Figure 18

OUTPUT VOLTAGE
vs
ELAPSED TIME

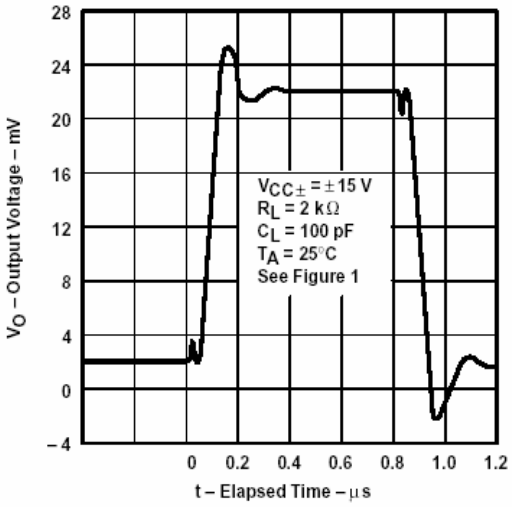


Figure 19

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

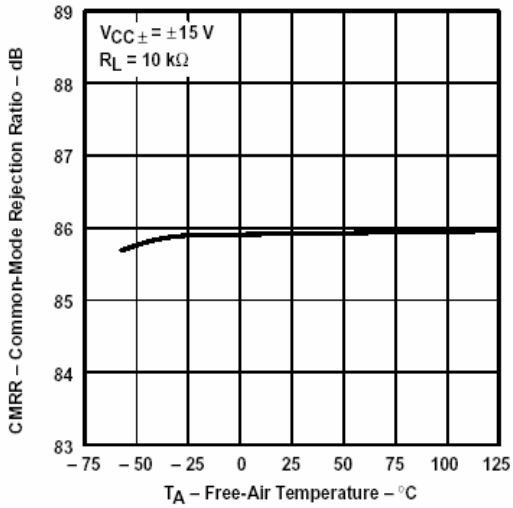


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

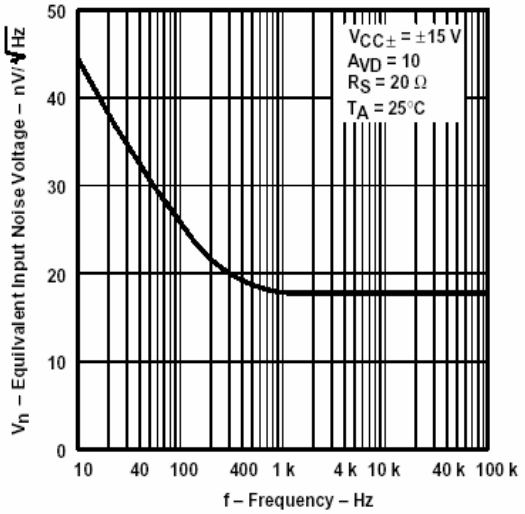


Figure 21

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

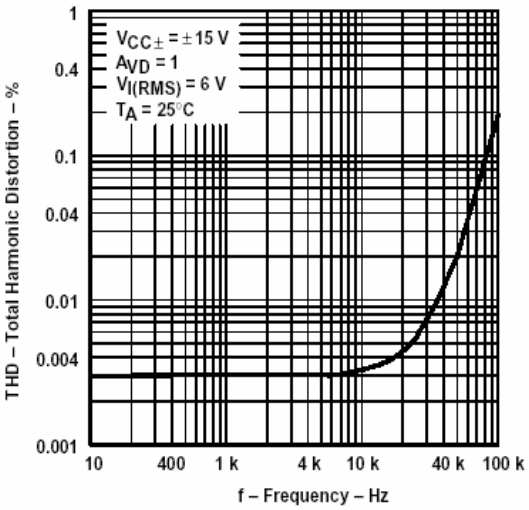


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

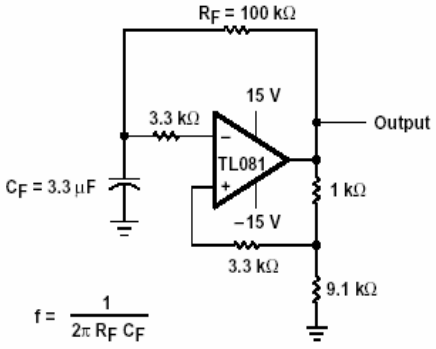


Figure 23

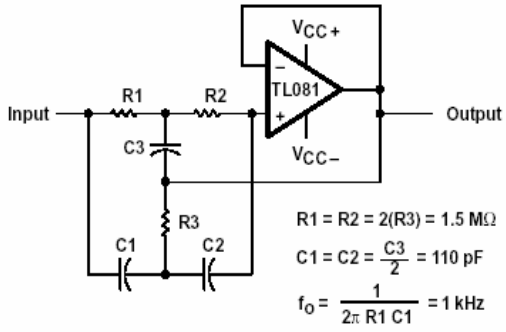


Figure 24

APPLICATION INFORMATION

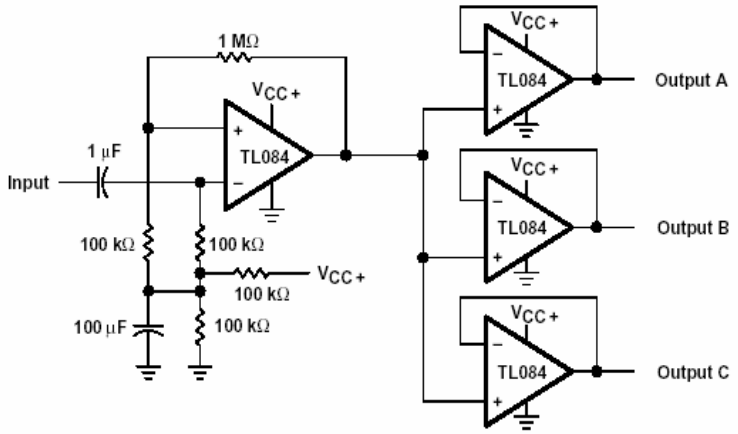
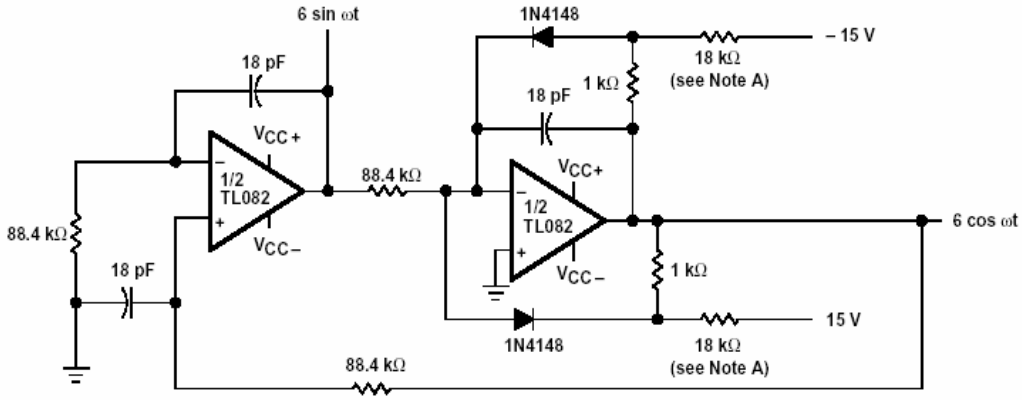


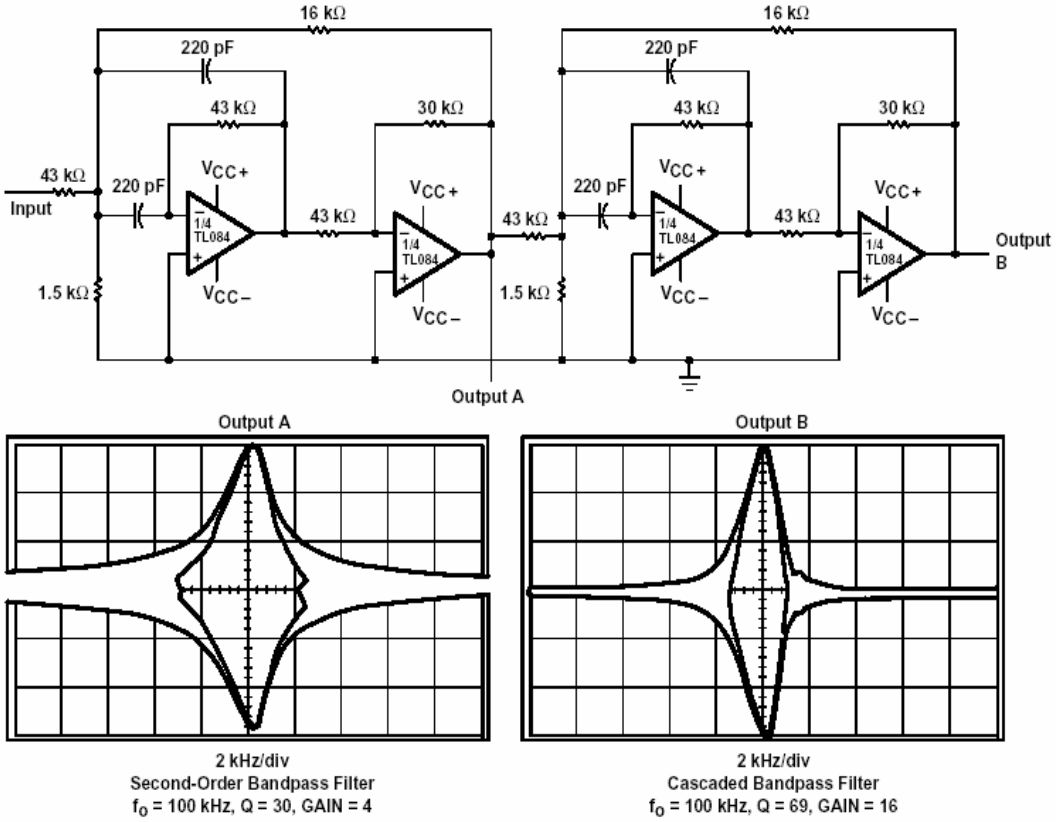
Figure 25. Audio-Distribution Amplifier



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

APPLICATION INFORMATION



2 kHz/div
Second-Order Bandpass Filter
f_0 = 100 kHz, Q = 30, GAIN = 4

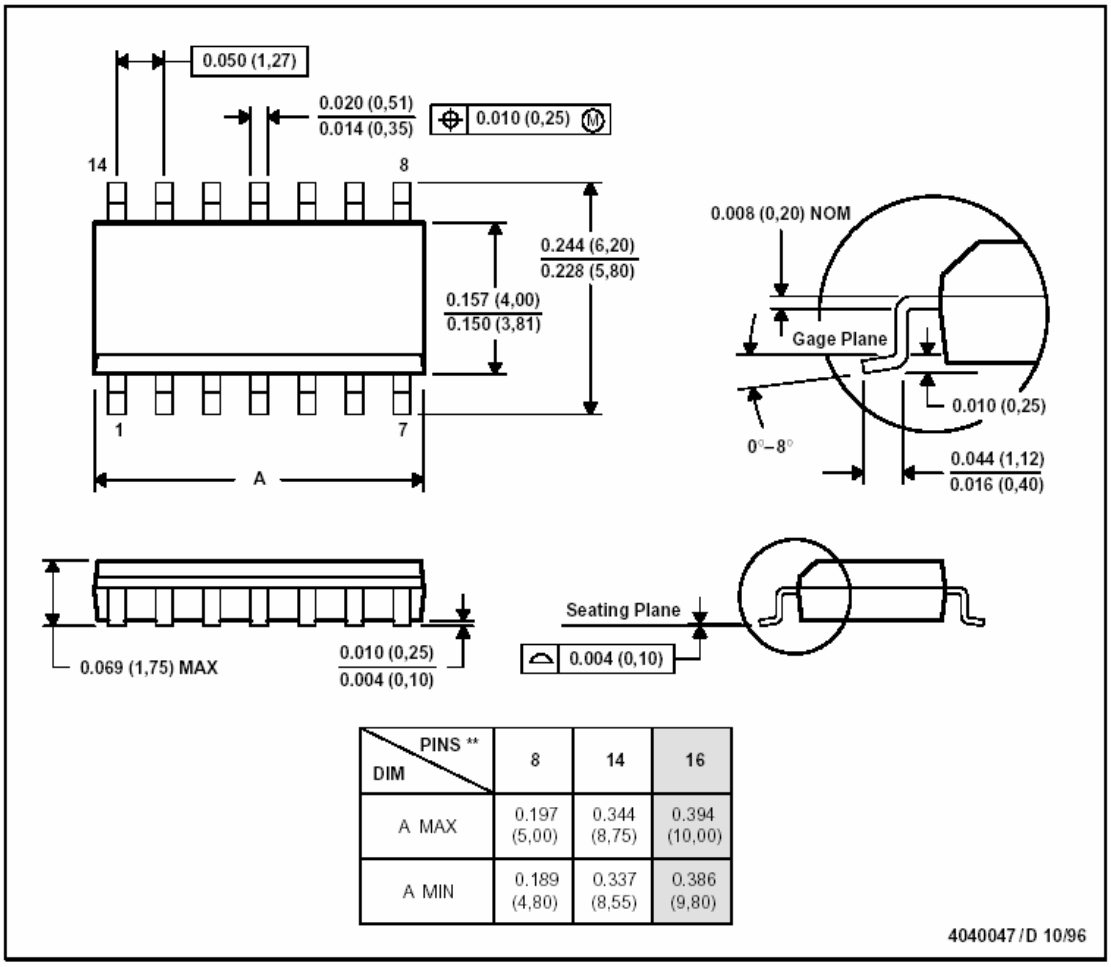
2 kHz/div
Cascaded Bandpass Filter
f_0 = 100 kHz, Q = 69, GAIN = 16

Figure 27. Positive-Feedback Bandpass Filter

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

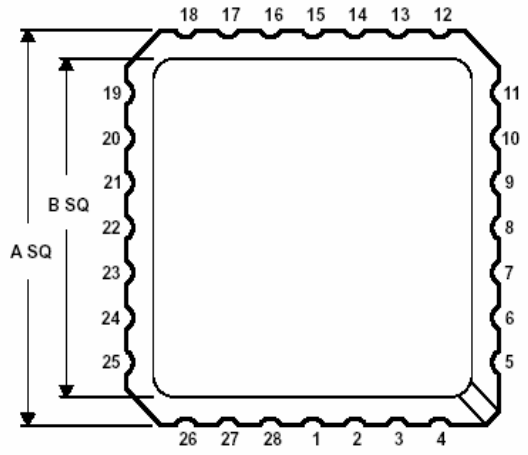
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

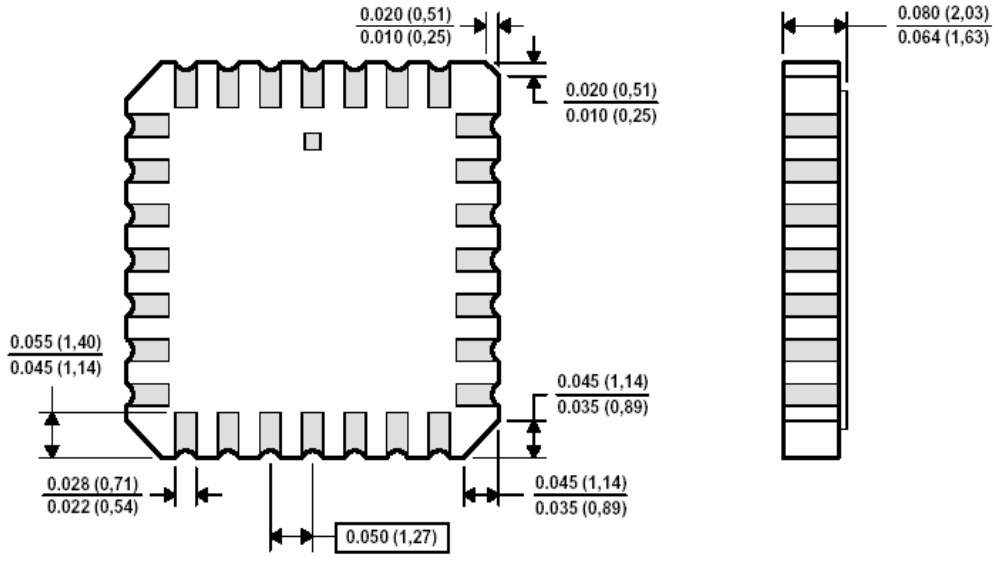
MECHANICAL DATA

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



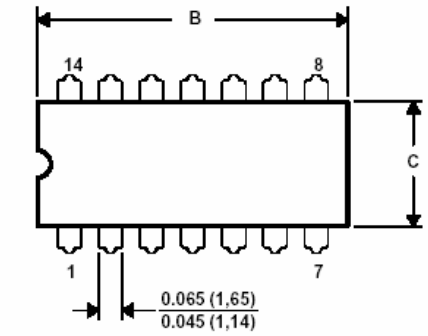
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

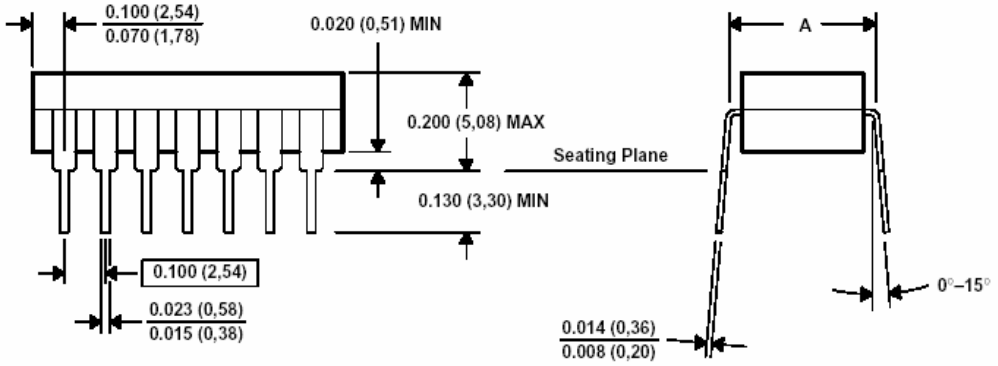
MECHANICAL DATA

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)

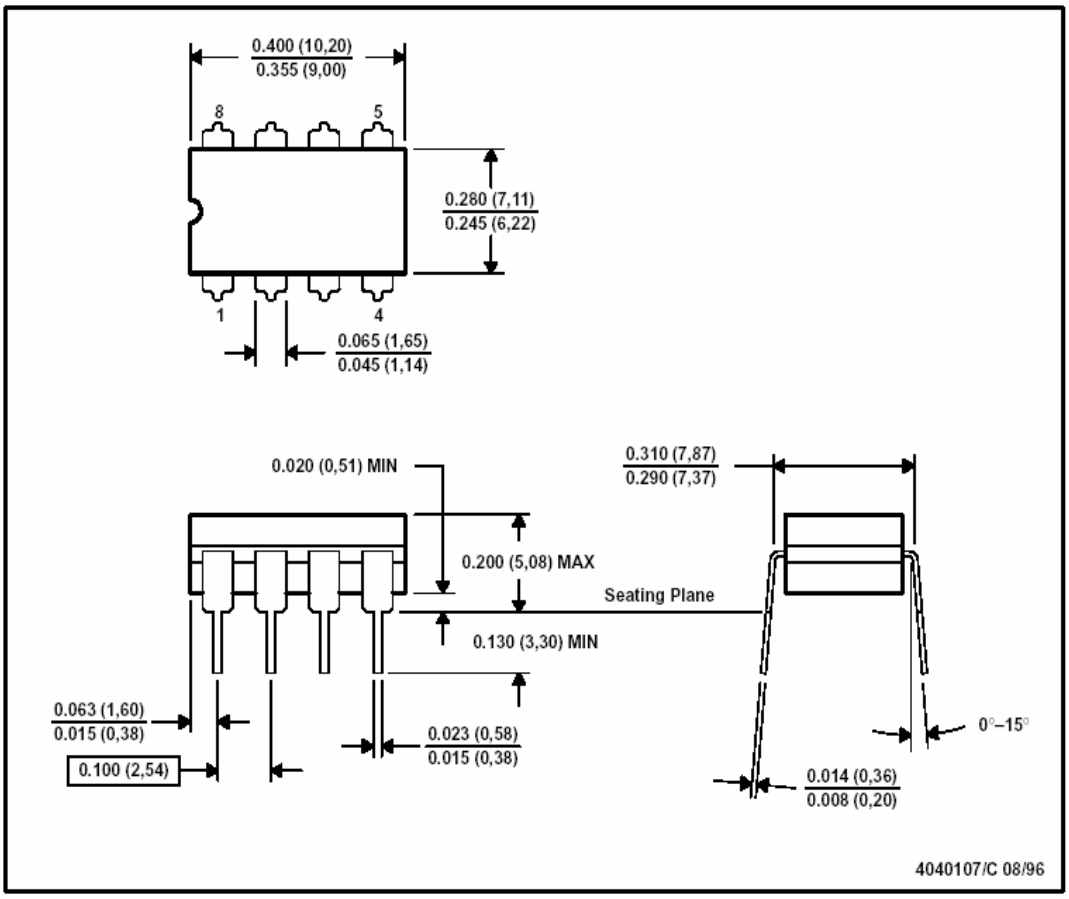


4040083/D 08/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

MECHANICAL DATA

JG (R-GDIP-T8) CERAMIC DUAL-IN-LINE PACKAGE



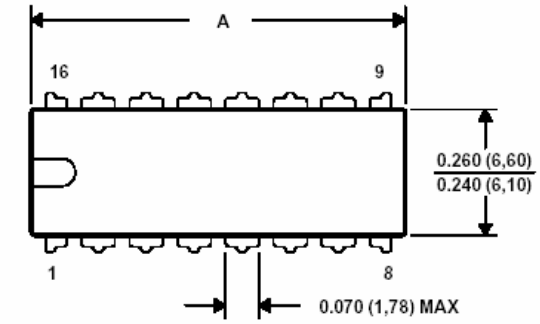
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

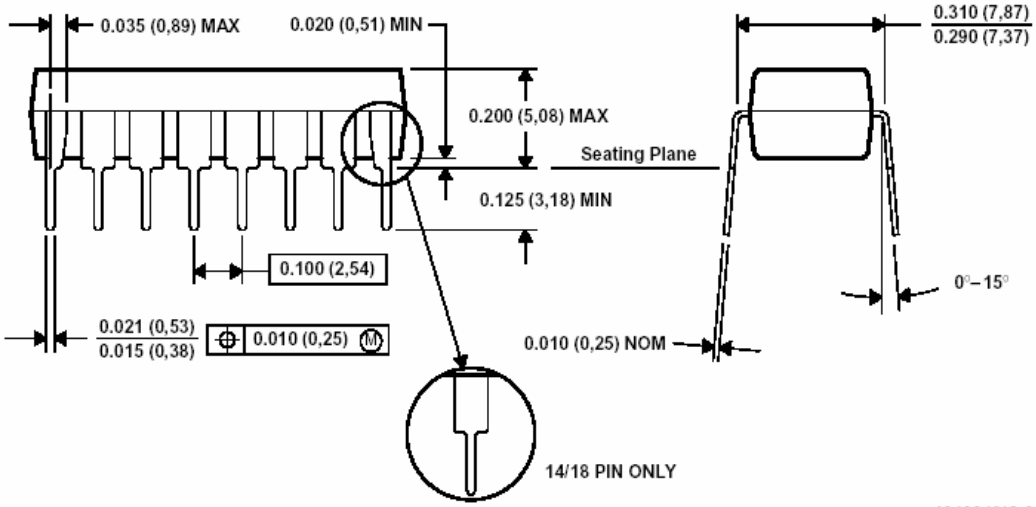
MECHANICAL DATA

N (R-PDIP-T)** — **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



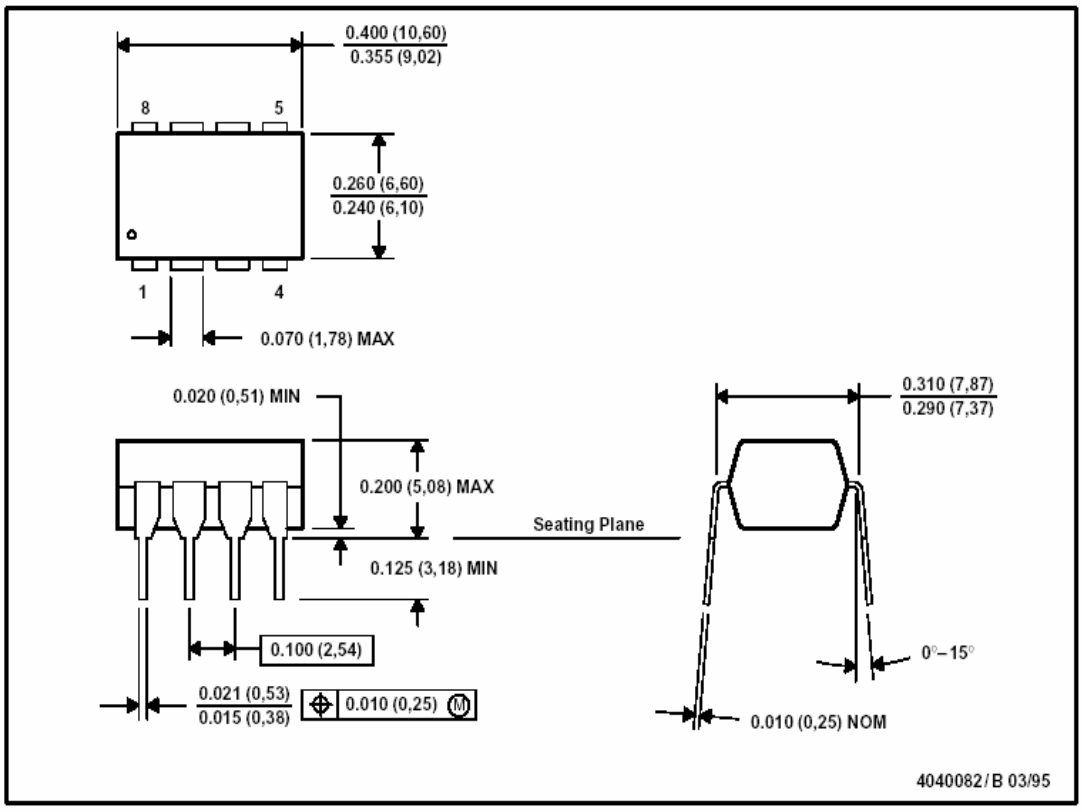


4040049/C 08/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

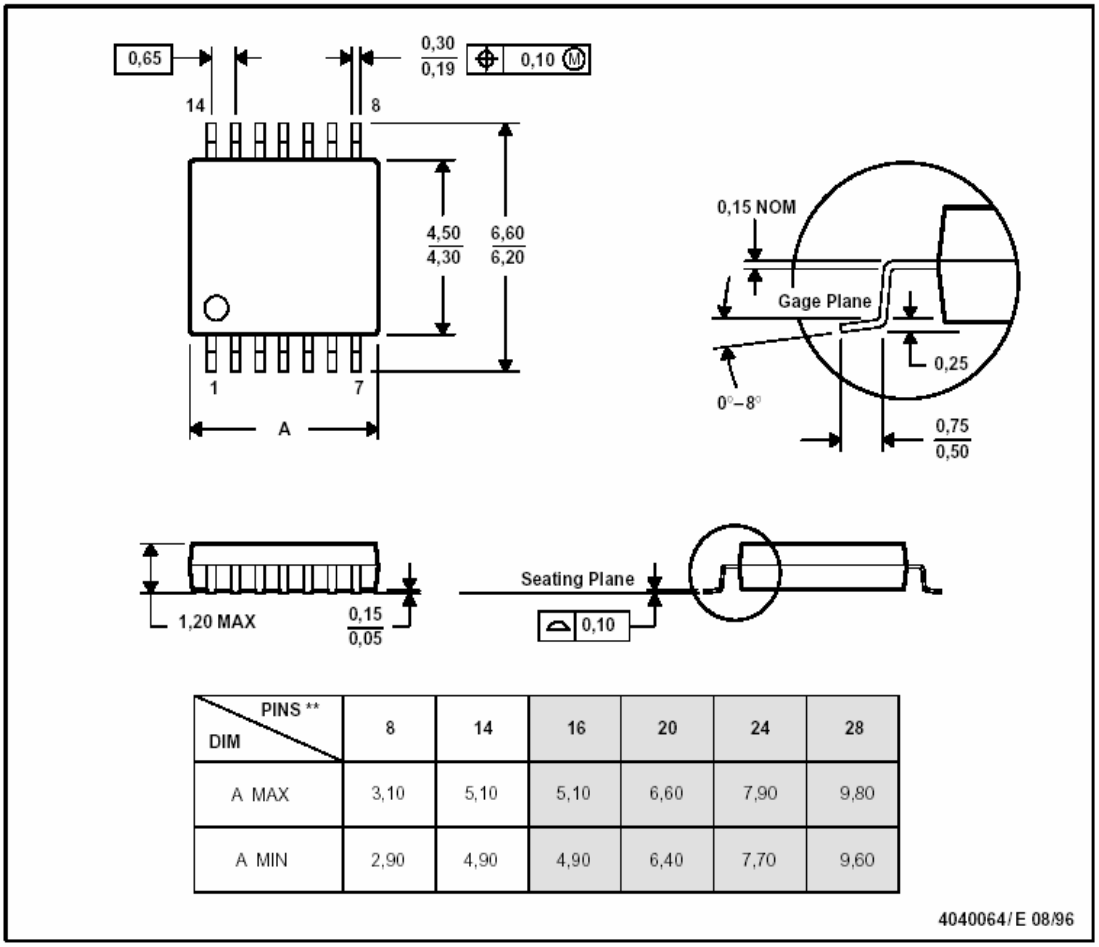


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL DATA

PW (R-PDSO-G)** — **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



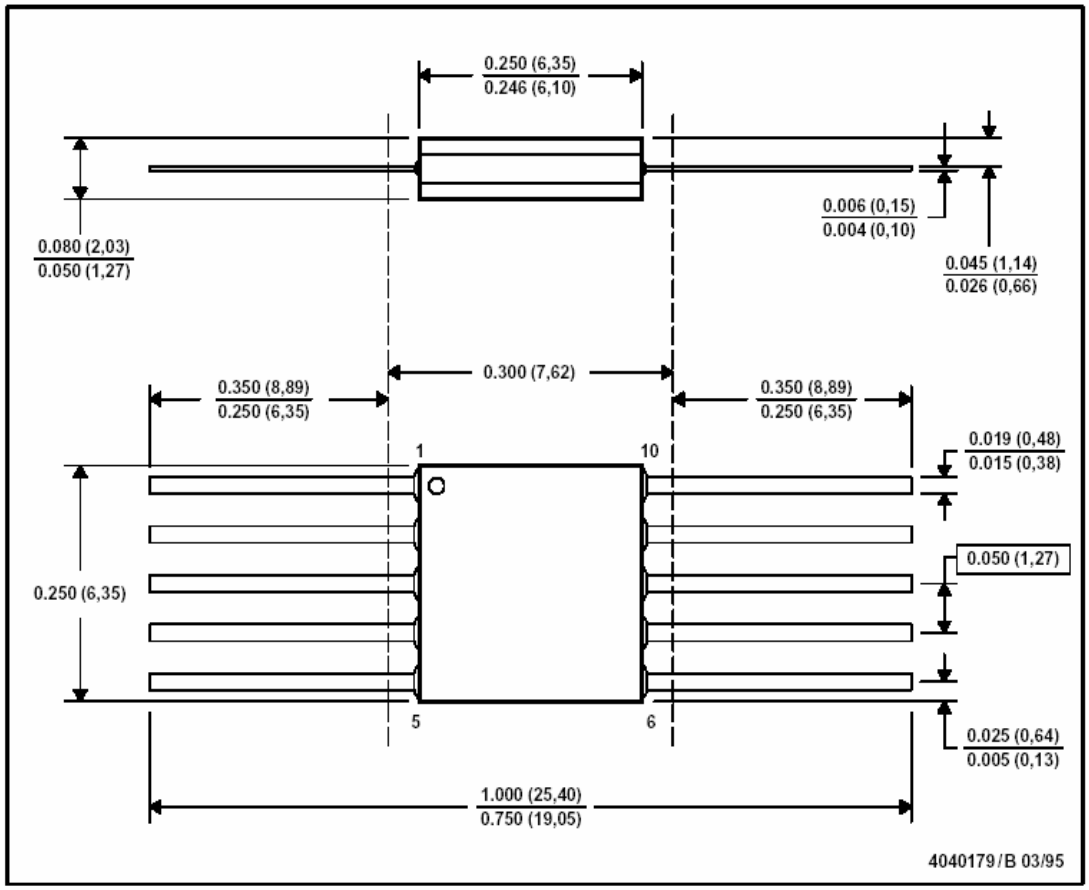
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

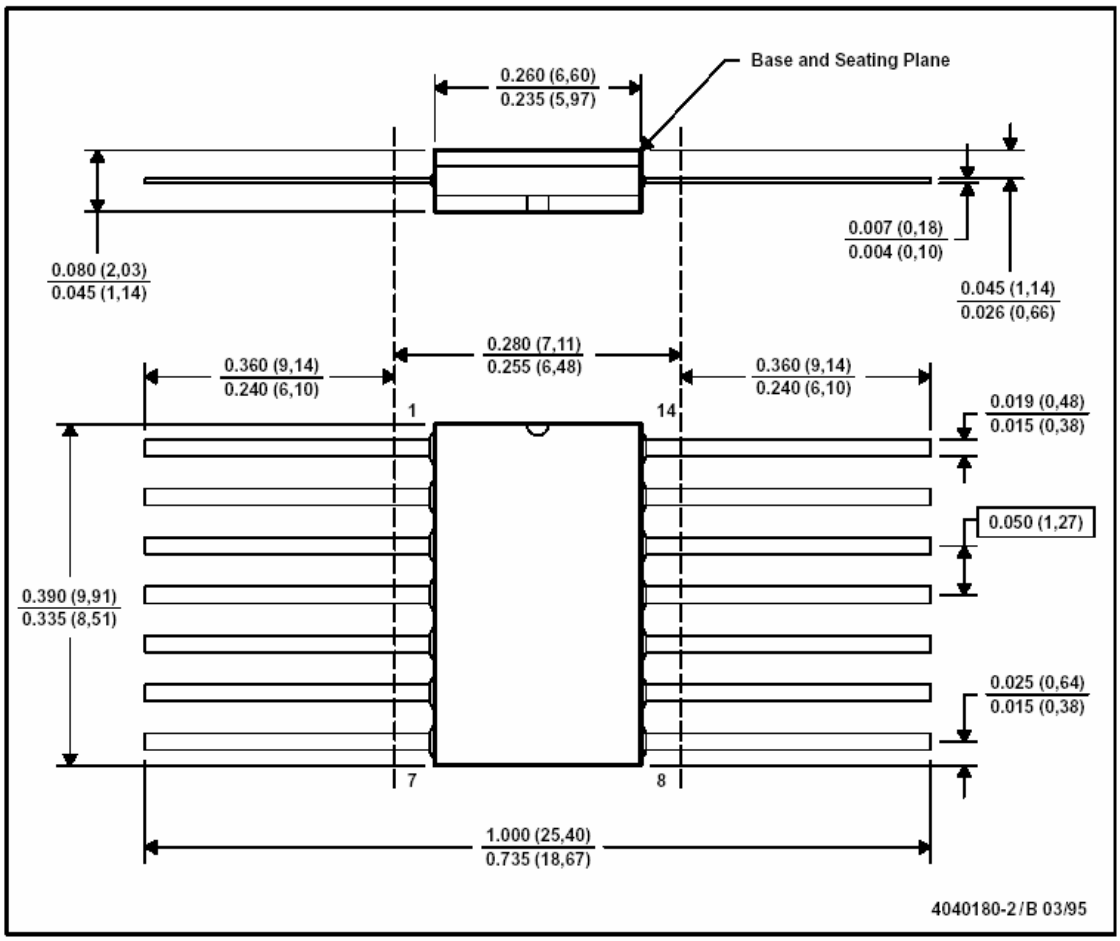
U (S-GDFP-F10) CERAMIC DUAL FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

MECHANICAL DATA

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

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