

DATA SHEET

74HC595; 74HCT595

8-bit serial-in, serial or parallel-out
shift register with output latches;
3-state

Product specification
Supersedes data of 1998 Jun 04

2003 Jun 25

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT595 is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_CP input. The data in each register is transferred to the storage register on a positive-going transition of the ST_CP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC	74HCT	
t _{PHL} /t _{PLH}	propagation delay SH_CP to Q7'	C _L = 50 pF; V _{CC} = 4.5 V	19	25	ns
	SH_CP to Qn		20	24	ns
	MR to Q7'		100	52	ns
f _{max}	maximum clock frequency SH_CP and ST_CP		100	57	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	115	130	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. For 74HC595 the condition is V_I = GND to V_{CC}.

For 74HCT595 the condition is V_I = GND to V_{CC} – 1.5 V.

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FUNCTION TABLE

See note 1.

INPUT					OUTPUT		FUNCTION
SH_CP	ST_CP	OE	MR	DS	Q7'	Qn	
X	X	L	L	X	L	n.c.	a LOW level on MR only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6'	n.c.	logic high level shifted into shift register stage 0; contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6') appears on the serial output (Q7')
X	↑	L	H	X	n.c.	Qn'	contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6'	Qn'	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note

1. H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH transition;
↓ = HIGH-to-LOW transition;
Z = high-impedance OFF-state;
n.c. = no change;
X = don't care.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC595N	−40 to +125 °C	16	DIP16	plastic	SOT38-4
74HCT595N	−40 to +125 °C	16	DIP16	plastic	SOT38-4
74HC595D	−40 to +125 °C	16	SO16	plastic	SOT109-1
74HCT595D	−40 to +125 °C	16	SO16	plastic	SOT109-1
74HC595DB	−40 to +125 °C	16	SSOP16	plastic	SOT338-1
74HCT595DB	−40 to +125 °C	16	SSOP16	plastic	SOT338-1
74HC595PW	−40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74HCT595PW	−40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74HC595BQ	−40 to +125 °C	16	DHVQFN16	plastic	SOT763-1
74HCT595BQ	−40 to +125 °C	16	DHVQFN16	plastic	SOT763-1

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PINNING

PIN	SYMBOL	DESCRIPTION
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0 V)
9	Q7'	serial data output
10	$\overline{\text{MR}}$	master reset (active LOW)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{\text{OE}}$	output enable (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V _{CC}	positive supply voltage

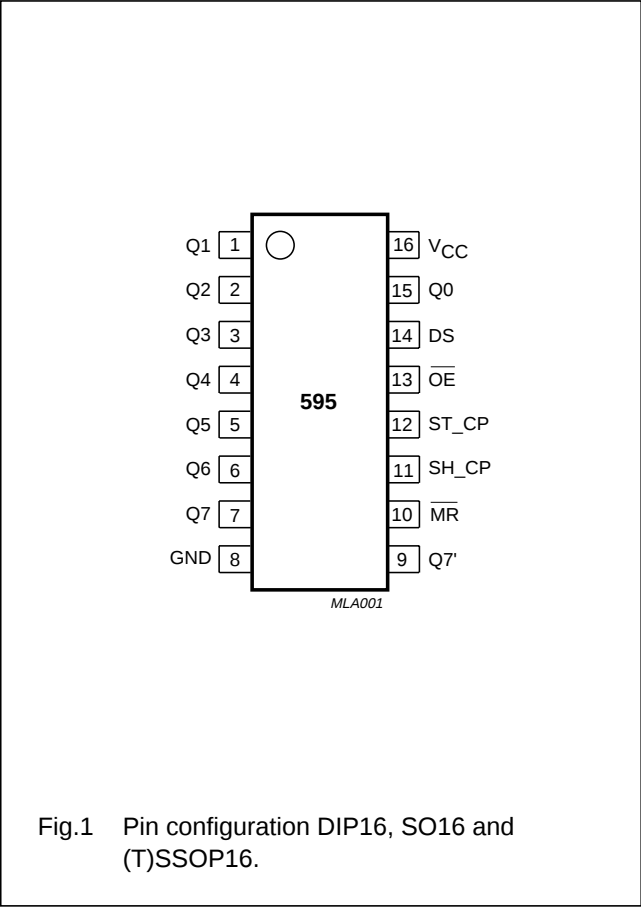
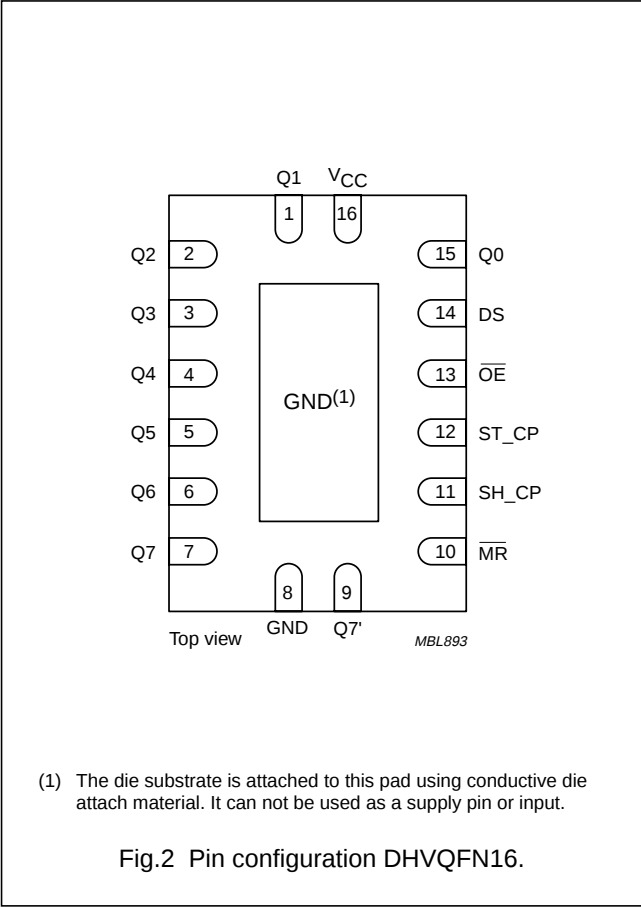


Fig.1 Pin configuration DIP16, SO16 and (T)SSOP16.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

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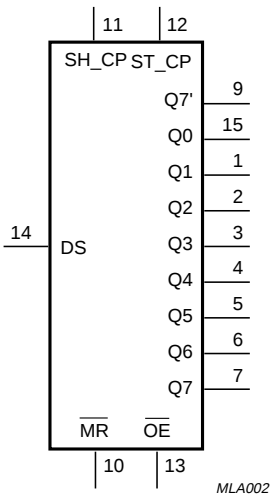


Fig.3 Logic symbol.

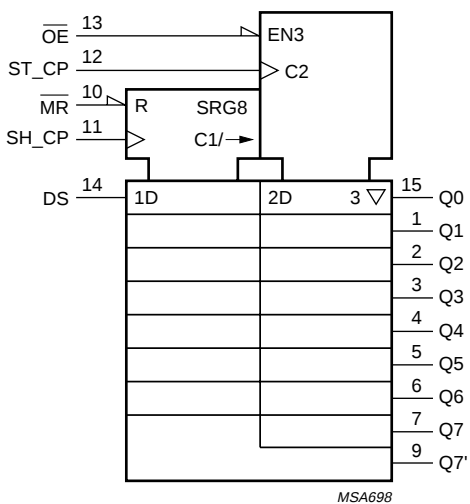


Fig.4 IEC logic symbol.

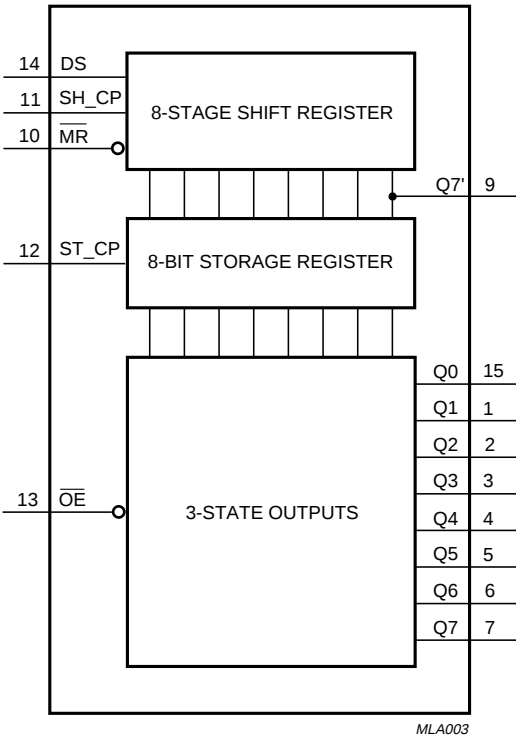


Fig.5 Functional diagram.

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

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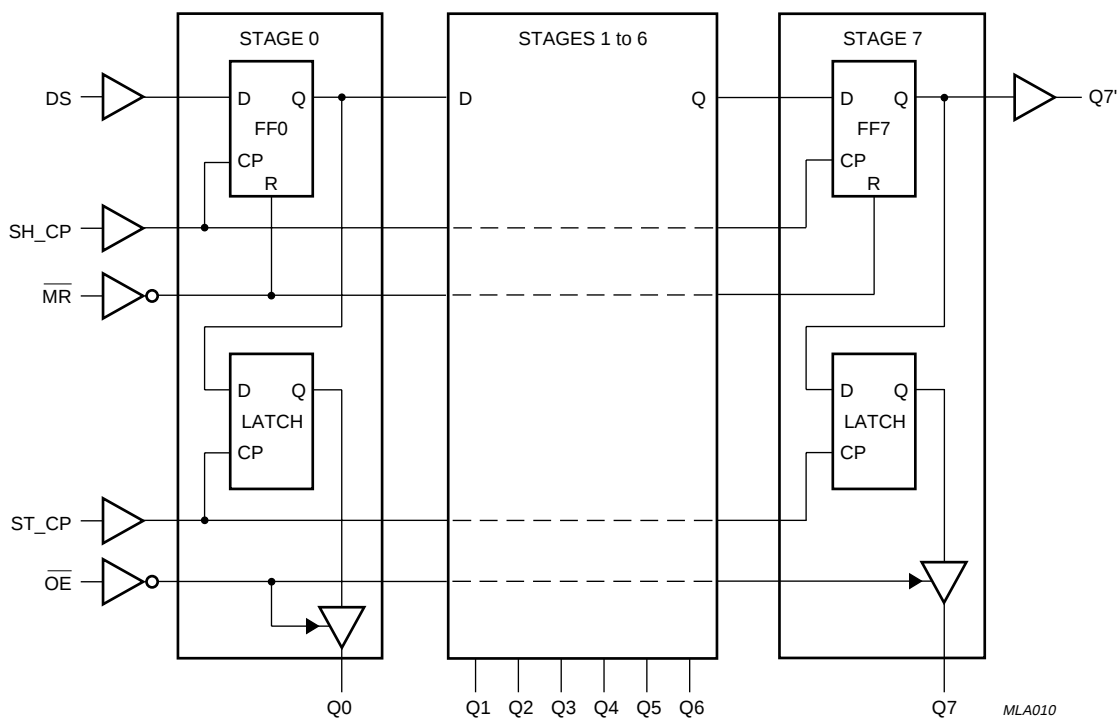
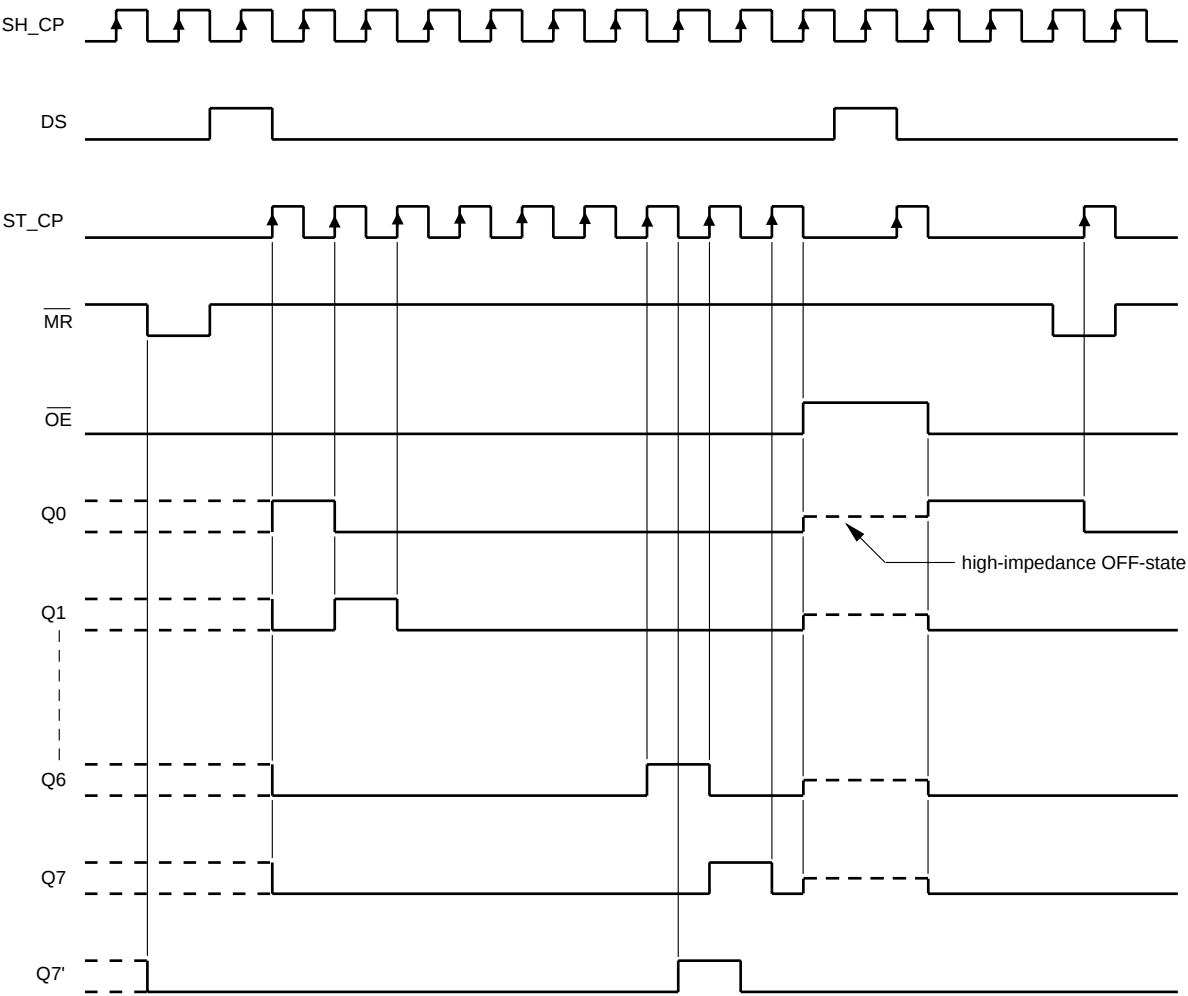


Fig.6 Logic diagram.

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MLA005-1

Fig.6 Timing diagram.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC			74HCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature		–40	–	+125	–40	–	+125	°C
t_r, t_f	input rise and fall time	$V_{CC} = 2.0$ V	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5$ V	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0$ V	–	–	400	–	–	–	ns

LIMITED VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5$ V to $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V to $V_O > V_{CC} + 0.5$ V	–	±20	mA
I_O	output source or sink current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V			
		Q7' standard output	–	±25	mA
		Qn bus driver outputs	–	±35	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±70	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 1	–	500	mW

Note

- For DIP16 packages: above 70 °C derate linearly with 12 mW/K.
 For SO16 packages: above 70 °C derate linearly with 8 mW/K.
 For SSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.
 For TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

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DC CHARACTERISTICS

Type 74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		2.0	1.5	1.2	−	V
			4.5	3.15	2.4	−	V
			6.0	4.2	3.2	−	V
V _{IL}	LOW-level input voltage		2.0	−	0.8	0.5	V
			4.5	−	2.1	1.35	V
			6.0	−	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs					
		I _O = −20 μA	2.0	1.9	2.0	−	V
			4.5	4.4	4.5	−	V
			6.0	5.9	6.0	−	V
		Q7' standard output					
		I _O = −4.0 mA	4.5	3.84	4.32	−	V
		I _O = −5.2 mA	6.0	5.34	5.81	−	V
		Qn bus driver outputs					
		I _O = −6.0 mA	4.5	3.84	4.32	−	V
		I _O = −7.8 mA	6.0	5.34	5.81	−	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs					
		I _O = 20 μA	2.0	−	0	0.1	V
			4.5	−	0	0.1	V
			6.0	−	0	0.1	V
		Q7' standard output					
		I _O = 4.0 mA	4.5	−	0.15	0.33	V
		I _O = 5.2 mA	6.0	−	0.16	0.33	V
		Qn bus driver outputs					
		I _O = 6.0 mA	4.5	−	0.16	0.33	V
		I _O = 7.8 mA	6.0	−	0.16	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	−	−	±1.0	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	−	−	±5.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	−	−	80	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs I _O = −20 μA	2.0	1.9	–	–	V
			4.5	4.4	–	–	V
			6.0	5.9	–	–	V
		Q7' standard output I _O = −4.0 mA I _O = −5.2 mA	4.5	3.7	–	–	V
			6.0	5.2	–	–	V
		Qn bus driver outputs I _O = −6.0 mA I _O = −7.8 mA	4.5	3.7	–	–	V
			6.0	5.2	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs I _O = 20 μA	4.5	–	–	0.1	V
		Q7' standard output I _O = 4.0 mA	4.5	–	–	0.4	V
		Qn bus driver outputs I _O = 6.0 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±10.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	160	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

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Type 74HCT

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = −40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs I _O = −20 μA	4.5	4.4	4.5	–	V
		Q7' standard output I _O = −4.0 mA	4.5	3.84	4.32	–	V
		Qn bus driver outputs I _O = −6.0 mA	4.5	3.7	4.32	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs I _O = 20 μA	4.5	–	0	0.33	V
		Q7' standard output I _O = 4.0 mA	4.5	–	0.15	0.33	V
		Qn bus driver outputs I _O = 6.0 mA	4.5	–	0.16	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±5.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	80	μA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} − 2.1 V; I _O = 0; note 2	4.5 to 5.5	–	100	450	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T _{amb} = –40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs I _O = –20 μA	4.5	4.4	–	–	V
		Q7' standard output I _O = –4.0 mA	4.5	3.7	–	–	V
		Qn bus driver outputs I _O = –6.0 mA	4.5	3.7	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		all outputs I _O = 20 μA	4.5	–	–	0.1	V
		Q7' standard output I _O = 4.0 mA	4.5	–	–	0.4	V
		Qn bus driver outputs I _O = 6.0 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	5.5	–	–	±10.0	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	160	μA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0; note 2	4.5 to 5.5	–	–	490	μA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient per input pin:
 - a. pin DS: 0.25
 - b. pins $\overline{\text{MR}}$, SH_CP, ST_CP and $\overline{\text{OE}}$: 1.50.

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AC CHARACTERISTICS

Family 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T _{amb} = 25 °C							
t _{PHL} /t _{PLH}	propagation delay SH_CP to Q7'	see Fig.7	2.0	–	52	160	ns
			4.5	–	19	32	ns
			6.0	–	15	27	ns
	propagation delay ST_CP to Qn	see Fig.8	2.0	–	55	175	ns
			4.5	–	20	35	ns
			6.0	–	16	30	ns
t _{PHL}	propagation delay MR to Q7'	see Fig.10	2.0	–	47	175	ns
			4.5	–	17	35	ns
			6.0	–	14	30	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	see Fig.11	2.0	–	47	150	ns
			4.5	–	17	30	ns
			6.0	–	14	26	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	see Fig.11	2.0	–	41	150	ns
			4.5	–	15	30	ns
			6.0	–	12	26	ns
t _w	shift clock pulse width HIGH or LOW	see Fig.7	2.0	75	17	–	ns
			4.5	15	6	–	ns
			6.0	13	5	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	75	11	–	ns
			4.5	15	4	–	ns
			6.0	13	3	–	ns
	master reset pulse width LOW	see Fig.10	2.0	75	17	–	ns
			4.5	15	6.0	–	ns
			6.0	13	5.0	–	ns
t _{su}	set-up time DS to SH_CP	see Fig.9	2.0	50	11	–	ns
			4.5	10	4.0	–	ns
			6.0	9.0	3.0	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	75	22	–	ns
			4.5	15	8	–	ns
			6.0	13	7	–	ns
t _h	hold time DS to SH_CP	see Fig.9	2.0	+3	–6	–	ns
			4.5	+3	–2	–	ns
			6.0	+3	–2	–	ns

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
t _{rem}	removal time MR to SH_CP	see Fig.10	2.0	+50	−19	−	ns
			4.5	+10	−7	−	ns
			6.0	+9	−6	−	ns
f _{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	9	30	−	MHz
			4.5	30	91	−	MHz
			6.0	35	108	−	MHz
T _{amb} = −40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay SH_CP to Q7'	see Fig.7	2.0	−	−	200	ns
			4.5	−	−	40	ns
			6.0	−	−	34	ns
	propagation delay ST_CP to An	see Fig.8	2.0	−	−	220	ns
			4.5	−	−	44	ns
			6.0	−	−	37	ns
t _{PHL}	propagation delay MR to Q7'	see Fig.10	2.0	−	−	220	ns
			4.5	−	−	44	ns
			6.0	−	−	37	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	see Fig.11	2.0	−	−	190	ns
			4.5	−	−	38	ns
			6.0	−	−	33	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	see Fig.11	2.0	−	−	190	ns
			4.5	−	−	38	ns
			6.0	−	−	33	ns
t _w	shift clock pulse width HIGH or LOW	see Fig.7	2.0	95	−	−	ns
			4.5	19	−	−	ns
			6.0	16	−	−	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	95	−	−	ns
			4.5	19	−	−	ns
			6.0	16	−	−	ns
	master reset pulse width LOW	see Fig.10	2.0	95	−	−	ns
			4.5	19	−	−	ns
			6.0	16	−	−	ns
t _{su}	set-up time DS to SH_CP	see Fig.9	2.0	65	−	−	ns
			4.5	13	−	−	ns
			6.0	11	−	−	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	95	−	−	ns
			4.5	19	−	−	ns
			6.0	16	−	−	ns

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
t _h	hold time DS to SH_CP	see Fig.9	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
t _{rem}	removal time $\overline{MR}$ to SH_CP	see Fig.10	2.0	65	–	–	ns
			4.5	13	–	–	ns
			6.0	11	–	–	ns
f _{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	4.8	–	–	MHz
			4.5	24	–	–	MHz
			6.0	28	–	–	MHz
T _{amb} = –40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay SH_CP to Q7'	see Fig.7	2.0	–	–	240	ns
			4.5	–	–	48	ns
			6.0	–	–	41	ns
	propagation delay ST_CP to Qn	see Fig.8	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
t _{PHL}	propagation delay MR to Q7'	see Fig.10	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
t _{PZH} /t _{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
t _{PHZ} /t _{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
t _w	shift clock pulse width HIGH or LOW	see Fig.7	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
	master reset pulse width LOW	see Fig.10	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns

8-bit serial-in, serial or parallel-out shift
register with output latches; 3-state

74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
t _{su}	set-up time DS to SH_CP	see Fig.9	2.0	75	–	–	ns
			4.5	15	–	–	ns
			6.0	13	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
t _h	hold time DS to SH_CP	see Fig.9	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
t _{rem}	removal time MR to SH_CP	see Fig.10	2.0	75	–	–	ns
			4.5	15	–	–	ns
			6.0	13	–	–	ns
f _{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	4	–	–	MHz
			4.5	20	–	–	MHz
			6.0	24	–	–	MHz

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

Family 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T _{amb} = 25 °C							
t _{PHL} /t _{PLH}	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	25	42	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	24	40	ns
t _{PHL}	propagation delay MR to Q7'	see Fig.10	4.5	–	23	40	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	see Fig.11	4.5	–	21	35	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	see Fig.11	4.5	–	18	30	ns
t _w	shift clock pulse width HIGH or LOW	see Fig.7	4.5	16	6	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	16	5	–	ns
	master reset pulse width LOW	see Fig.10	4.5	20	8	–	ns
t _{su}	set-up time DS to SH_CP	see Fig.9	4.5	16	5	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	16	8	–	ns
t _h	hold time DS to SH_CP	see Fig.9	4.5	+3	–2	–	ns
t _{rem}	removal time MR to SH_CP	see Fig.10	4.5	+10	–7	–	ns
f _{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	30	52	–	MHz
T _{amb} = –40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	–	53	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	–	50	ns
t _{PHL}	propagation delay MR to Q7'	see Fig.10	4.5	–	–	50	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	see Fig.11	4.5	–	–	44	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	see Fig.11	4.5	–	–	38	ns

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

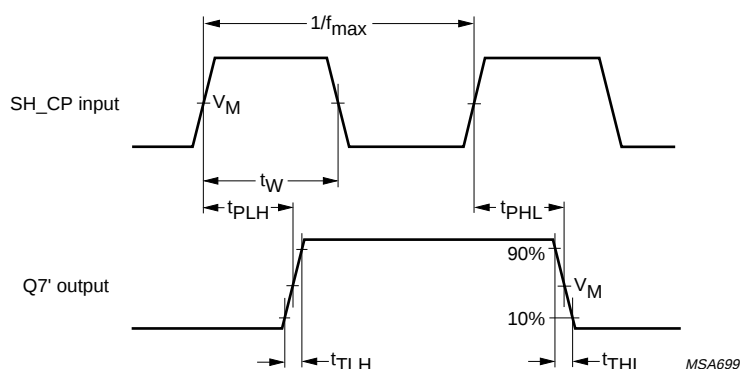
74HC595; 74HCT595

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
t _w	shift clock pulse width HIGH or LOW	see Fig.7	4.5	20	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	20	–	–	ns
	master reset pulse width LOW	see Fig.10	4.5	25	–	–	ns
t _{su}	set-up time DS to SH_CP	see Fig.9	4.5	20	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	20	–	–	ns
t _h	hold time DS to SH_CP	see Fig.9	4.5	3	–	–	ns
t _{rem}	removal time MR to SH_CP	see Fig.10	4.5	13	–	–	ns
f _{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	24	–	–	MHz
T_{amb} = –40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	–	63	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	–	60	ns
t _{PHL}	propagation delay MR to Q7'	see Fig.10	4.5	–	–	60	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	see Fig.11	4.5	–	–	53	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	see Fig.11	4.5	–	–	45	ns
t _w	shift clock pulse width HIGH or LOW	see Fig.7	4.5	24	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	24	–	–	ns
	master reset pulse width LOW	see Fig.10	4.5	30	–	–	ns
t _{su}	set-up time DS to SH_CP	see Fig.9	4.5	24	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	24	–	–	ns
t _h	hold time DS to SH_CP	see Fig.9	4.5	3	–	–	ns
t _{rem}	removal time MR to SH_CP	see Fig.10	4.5	15	–	–	ns
f _{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	20	–	–	MHz

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

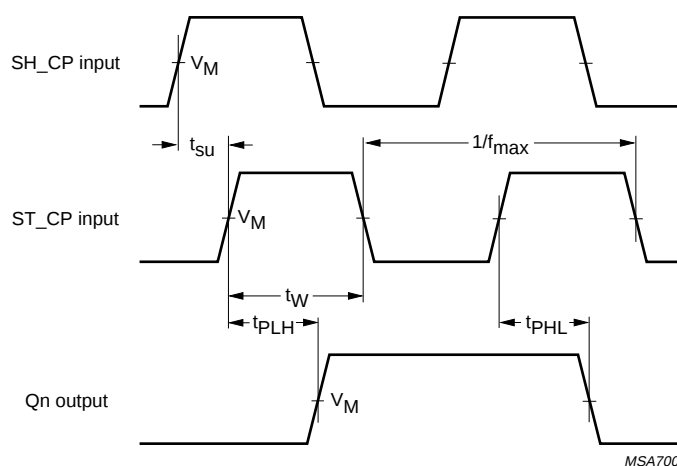
74HC595; 74HCT595

AC WAVEFORMS



74HC595: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 74HCT595: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.7 Waveforms showing the clock (SH_CP) to output (Q7') propagation delays, the shift clock pulse width and maximum shift clock frequency.

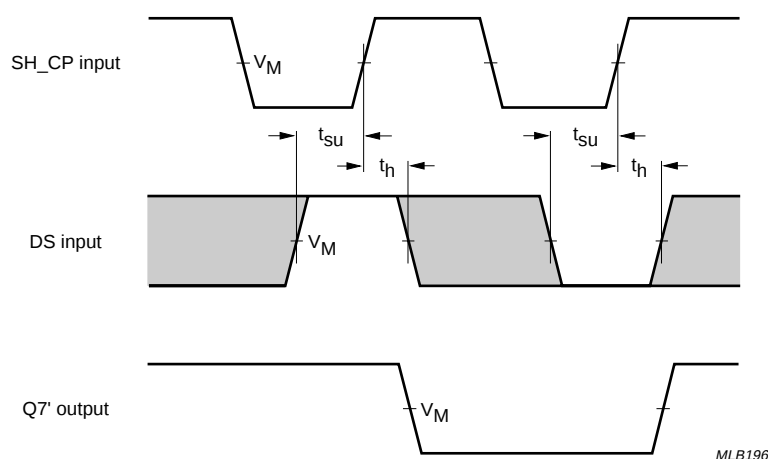


74HC595: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 74HCT595: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.8 Waveforms showing the storage clock (ST_CP) to output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

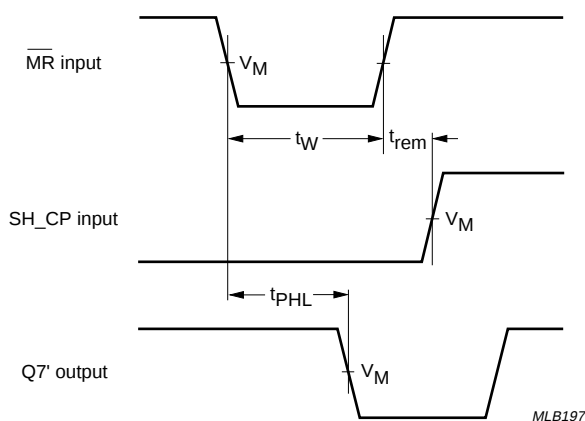
74HC595; 74HCT595



74HC595: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 74HCT595: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.9 Waveforms showing the data set-up and hold times for the DS input.

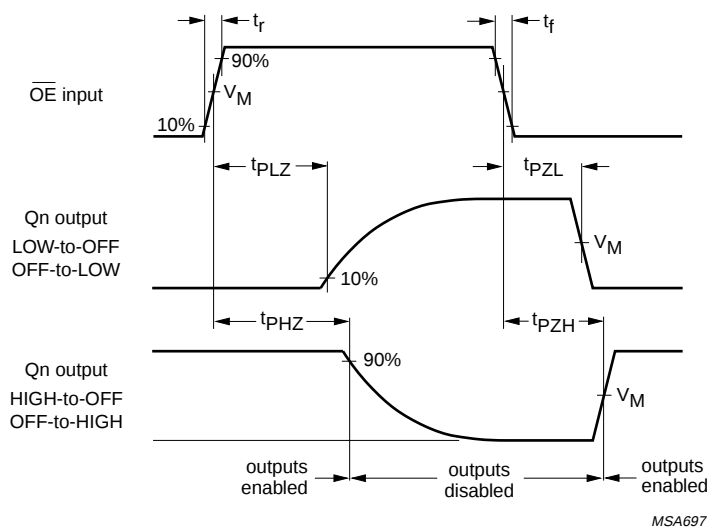


74HC595: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 74HCT595: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.10 Waveforms showing the Master Reset ($\overline{\text{MR}}$) pulse width, the master reset to output (Q7') propagation delay and the master reset to shift clock (SH_CP) removal time.

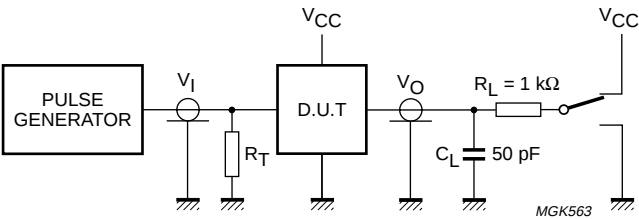
8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595



74HC595: $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
74HCT595: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Fig.11 Waveforms showing the 3-state enable and disable times for input $\overline{\text{OE}}$.



TEST	SWITCH
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.12 Test circuit for 3-state outputs.

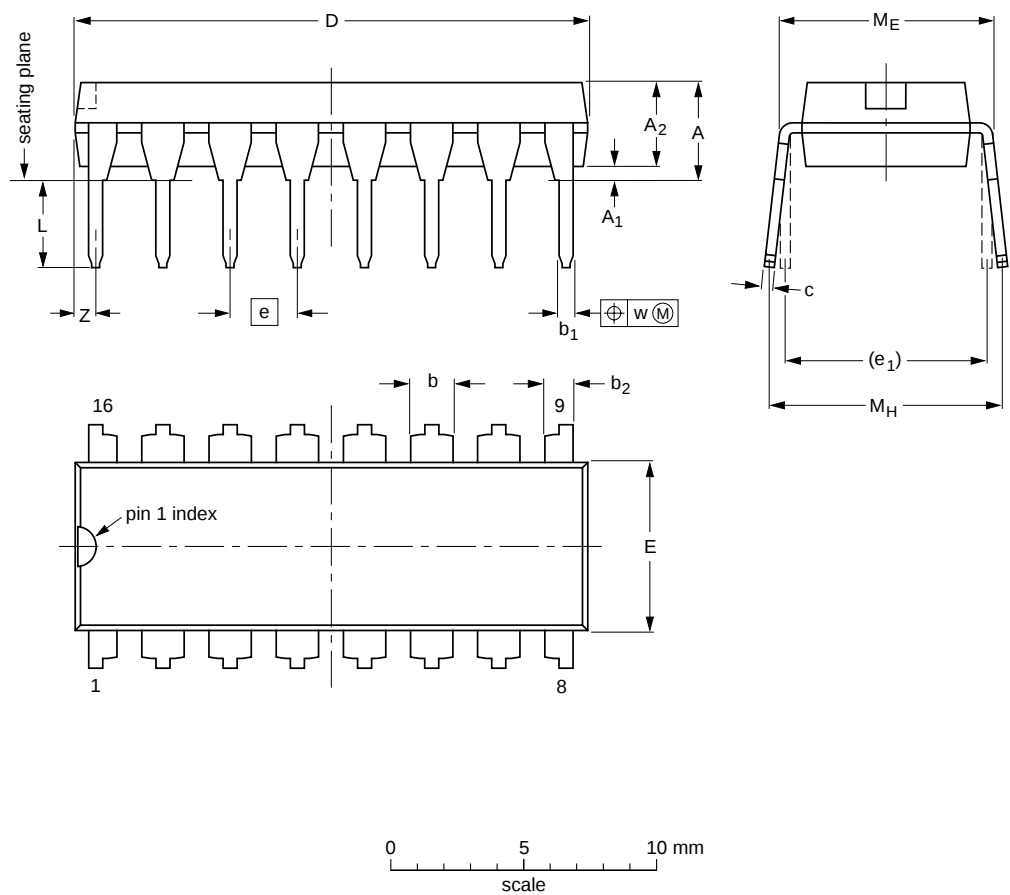
8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

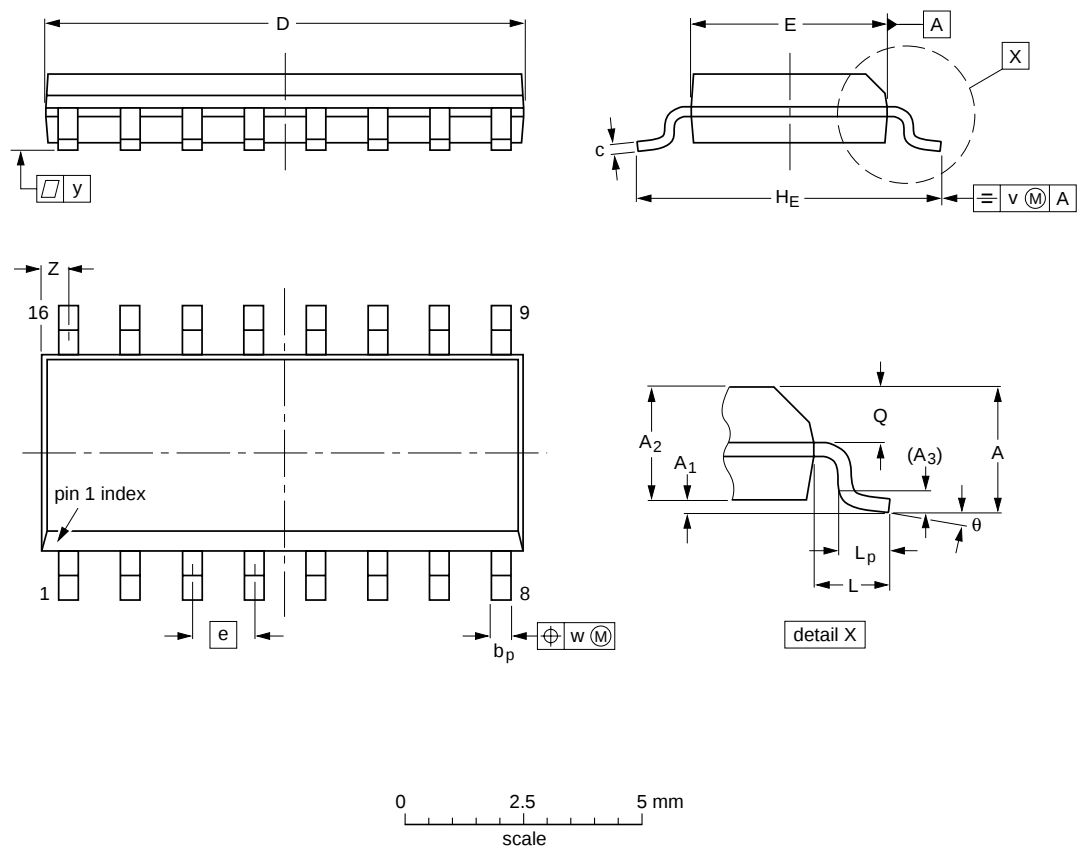
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						95-01-14 03-02-13

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

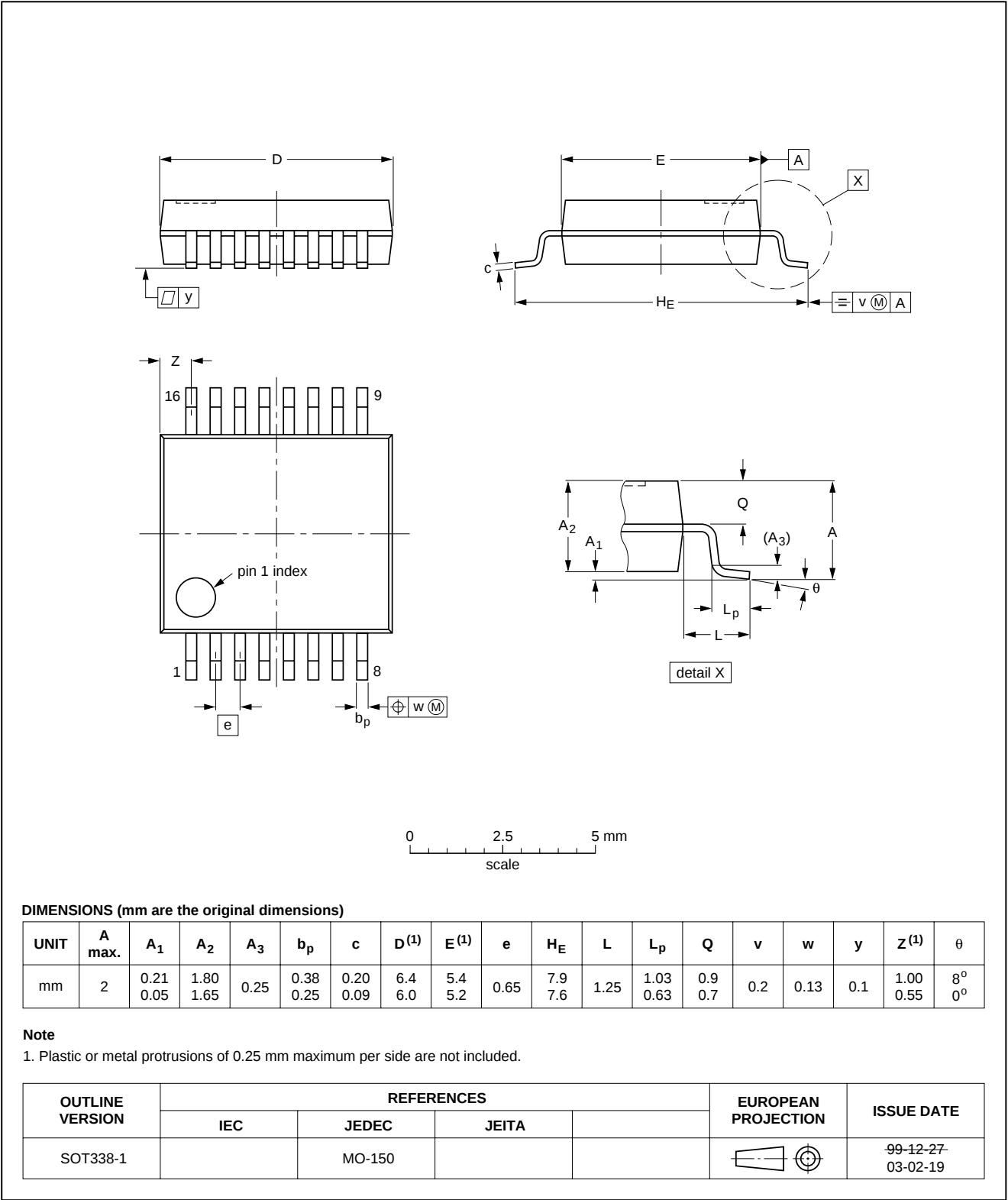
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

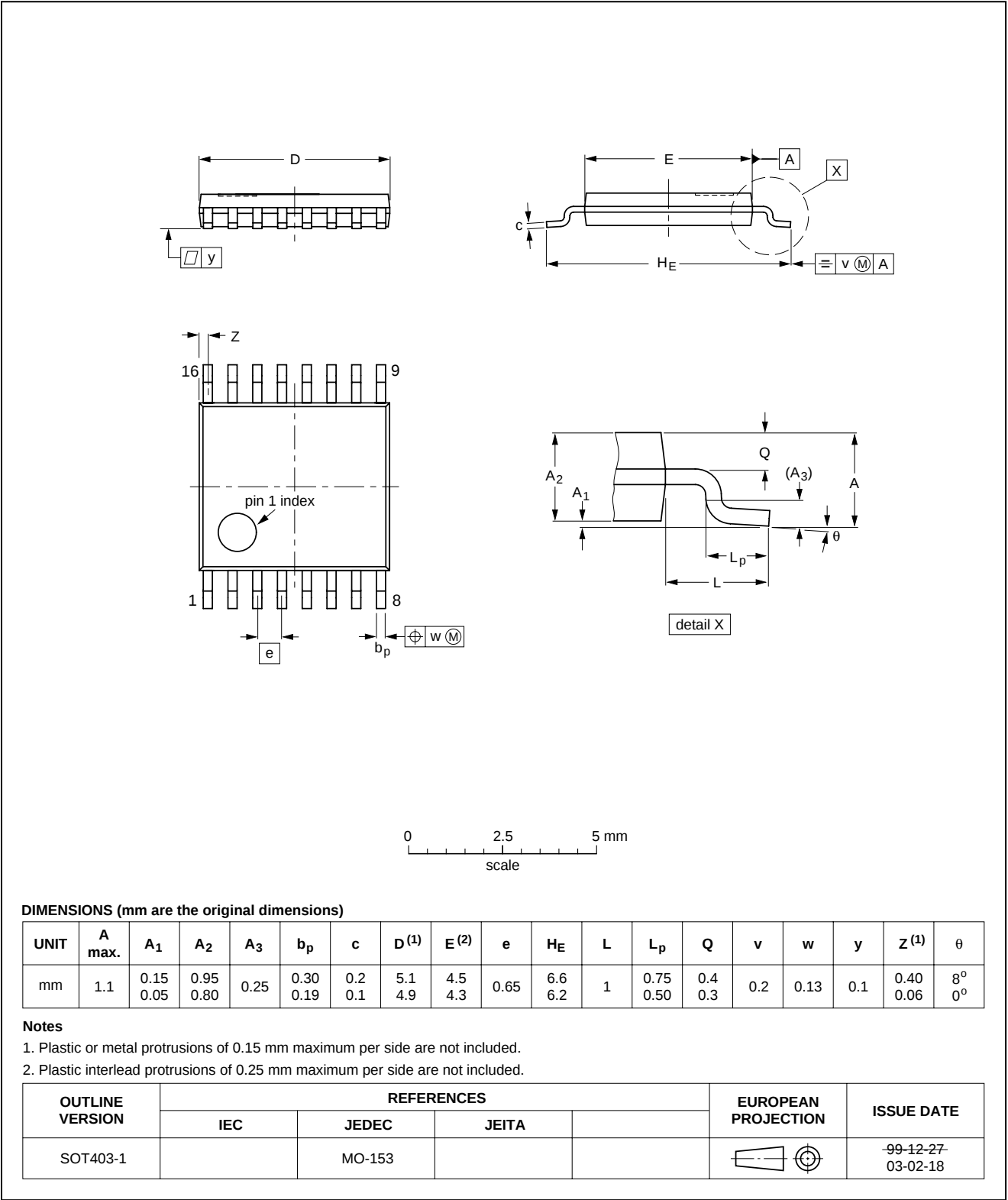


8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

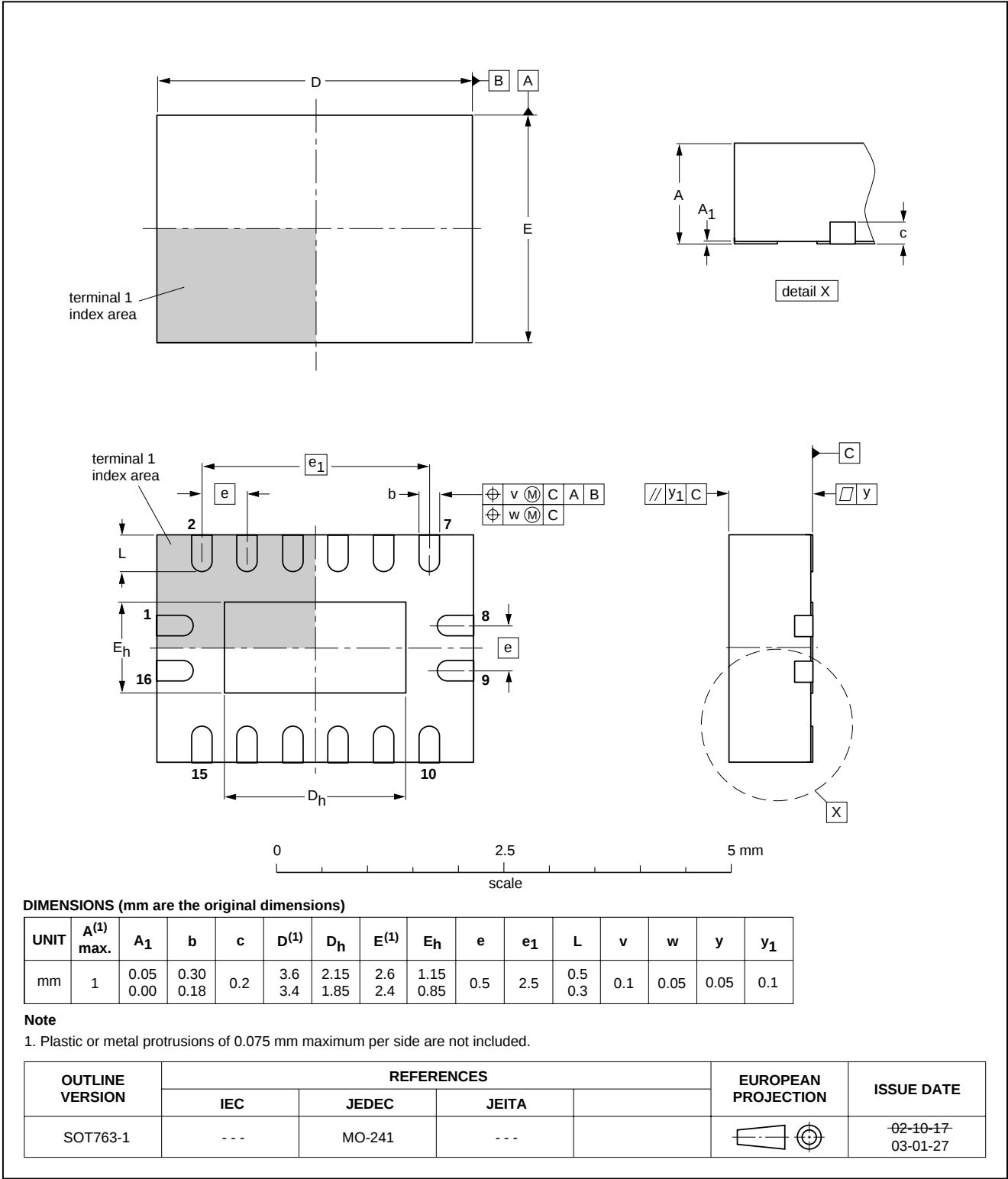


8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

74HC595; 74HCT595

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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GP2D02

Compact, High Sensitive Distance Measuring Sensor

■ Features

1. Impervious to color and reflectivity of reflective object
2. High precision distance measurement output for direct connection to microcomputer
3. Low dissipation current at OFF-state
(dissipation current at OFF-state : TYP. 3 μ A)
4. Capable of changing of distance measuring range through change the optical portion (lens)

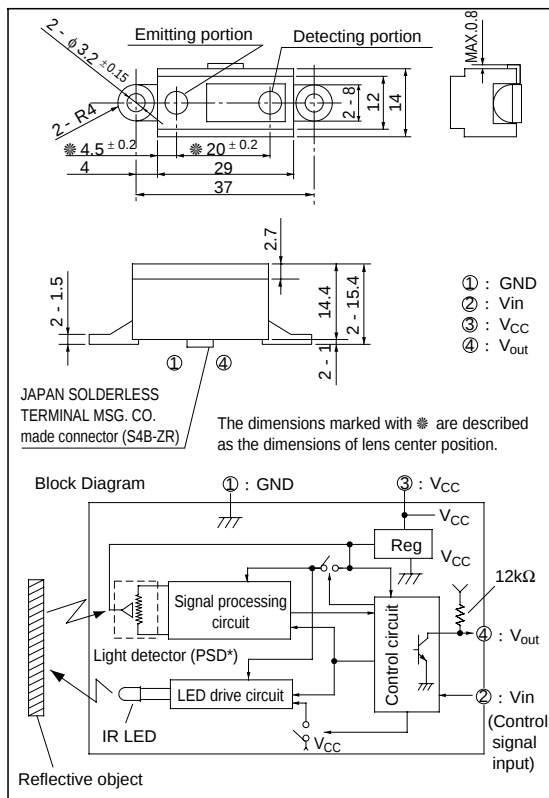
■ Applications

1. Sanitary sensors
2. Human body sensors for consumer products such as electric fans and air conditioners
3. Garage sensors

* PSD : Position Sensitive Detector

■ Outline Dimensions

(Unit : mm)



■ Absolute Maximum Ratings (Ta=25°C, VCC=5V)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.3 to + 10	V
*1 Input terminal voltage	V _{in}	- 0.3 to + 3	V
Output terminal voltage	BV _O	- 0.3 to + 10	V
Operating temperature	T _{opr}	- 10 to + 60	°C
Storage temperature	T _{stg}	- 40 to + 70	°C

*1 Open drain operation input

■ Operating Supply Voltage

Symbol	Rating	Unit
V _{CC}	4.4 to 7	V

Electro-optical Characteristics

(Ta=25°C,Vcc=5V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Distance measuring range		ΔL	*1	10	-	80	cm
Output terminal voltage		V_{OH}	Output voltage at High	$V_{CC} - 0.3$	-	-	V
		V_{OL}	Output voltage at Low				
Distance characteristics of output		D	L = 80cm, *1	-	75	-	DEC
		ΔD	Output change at L=80 cm to 20 cm,*1	48	58	68	DEC
Dissipation current	at operating	I_{CC}	L = 20cm, *1, *2	-	22	35	mA
	at OFF-state	I_{off}	L = 20cm, *1	-	3	8	μA
Vin terminal current		I_{vin}	Vin = 0V	-	- 170	- 280	μA

Note) L : Distance to reflective object

DEC : Decimalized value of sensor output (8-bit serial)

*1 Reflective object : White paper (reflectivity : 90%)

*2 Average dissipation current value during distance measuring operation when detecting of input signal, Vin as shown in the timing chart

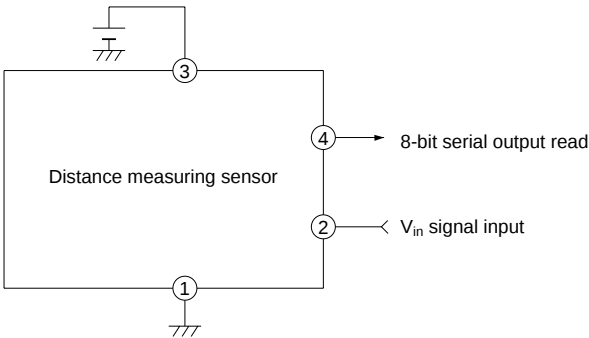
*3 Vin terminal : Open drain drive input.

Conditions : Vin terminal current at Vin OFF-state : -1 μA

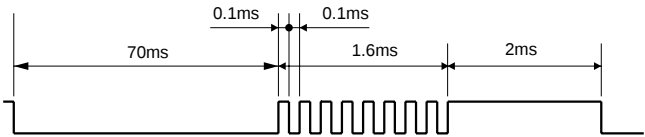
Vin terminal current at Vin ON-state : 0.3V

Test Circuit

1. Test circuit



2. Vin input signal for measurement



■ Timing Chart

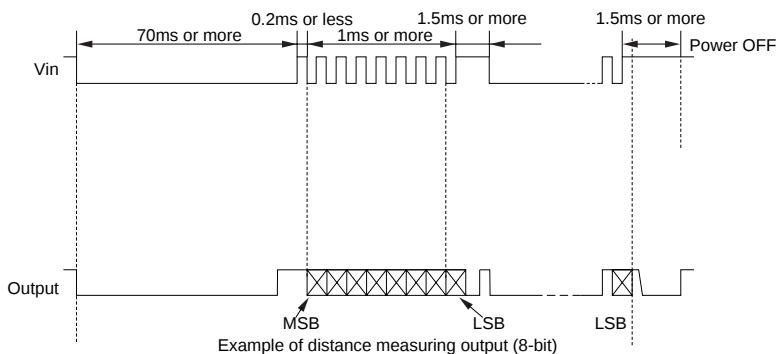


Fig. 1 Distance Measuring Output vs. Distance to Reflective Object

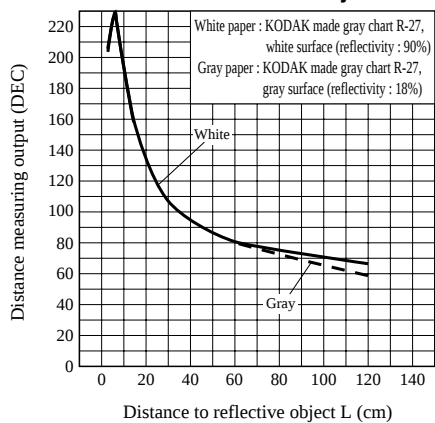
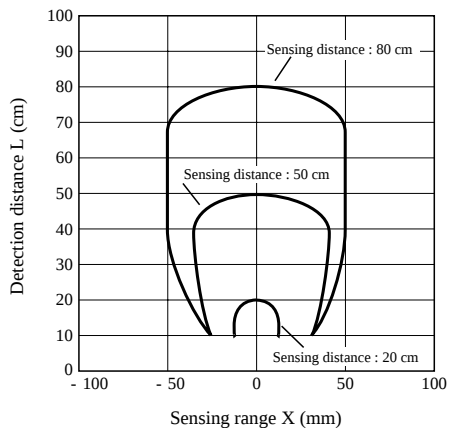


Fig. 2 Detection Distance vs. Sensing Range



Test Method for Sensing Range Characteristics

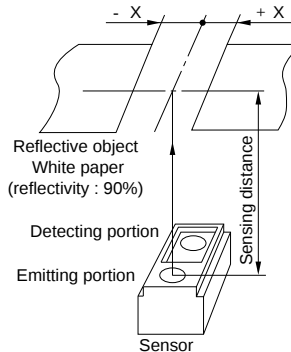
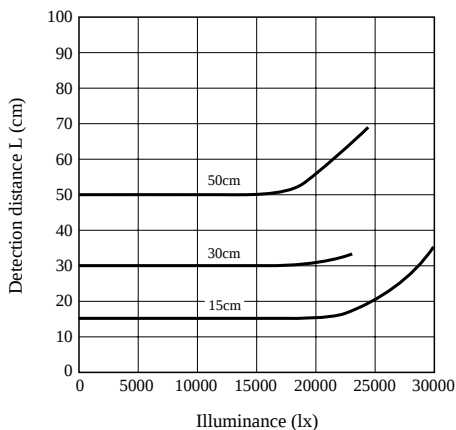
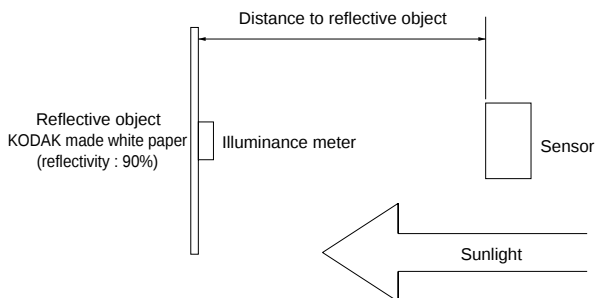


Fig. 3 Detection Distance vs. Illuminance



Test Method for Anti External Disturbing Light Characteristics



LM555 Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

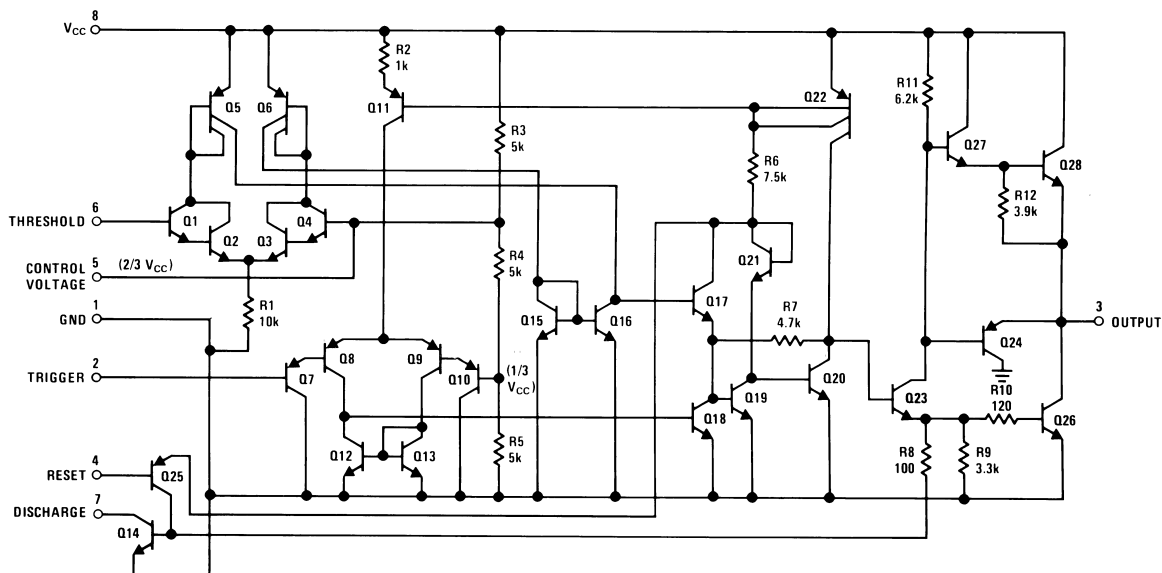
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

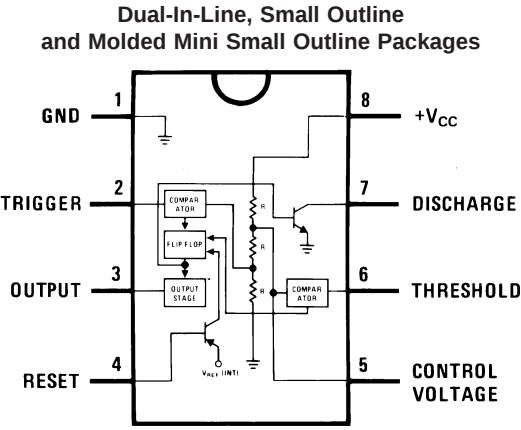
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



DS007851-1

Connection Diagram



Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages (SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

($T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V _{CC} = 5V, R _L = ∞ V _{CC} = 15V, R _L = ∞ (Low State) (Note 4)		3 10	6 15	mA
Timing Error, Monostable	R _A = 1k to 100kΩ, C = 0.1μF, (Note 5)				
Initial Accuracy			1		%
Drift with Temperature			50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable	R _A , R _B = 1k to 100kΩ, C = 0.1μF, (Note 5)				
Initial Accuracy			2.25		%
Drift with Temperature			150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V _{CC}
Trigger Voltage	V _{CC} = 15V		5		V
	V _{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	μA
Control Voltage Level	V _{CC} = 15V	9	10	11	V
	V _{CC} = 5V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V _{CC} = 15V, I ₇ = 15mA		180		mV
Output Low	V _{CC} = 4.5V, I ₇ = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

($T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V _{CC} = 15V				
	I _{SINK} = 10mA		0.1	0.25	V
	I _{SINK} = 50mA		0.4	0.75	V
	I _{SINK} = 100mA		2	2.5	V
	I _{SINK} = 200mA		2.5		V
	V _{CC} = 5V				
	I _{SINK} = 8mA				V
	I _{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I _{SOURCE} = 200mA, V _{CC} = 15V		12.5		V
	I _{SOURCE} = 100mA, V _{CC} = 15V	12.75	13.3		V
	V _{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (SO-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at $V_{CC} = 5\text{V}$.

Note 5: Tested at $V_{CC} = 5\text{V}$ and $V_{CC} = 15\text{V}$.

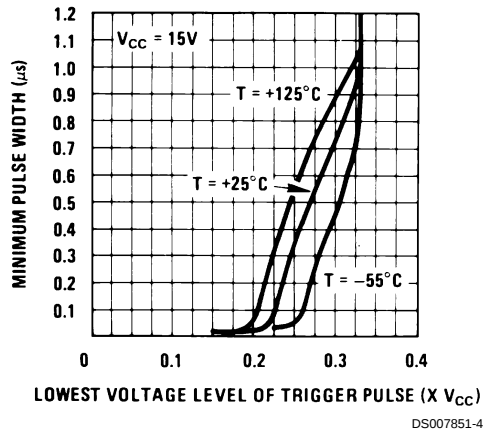
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is $20\text{M}\Omega$.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

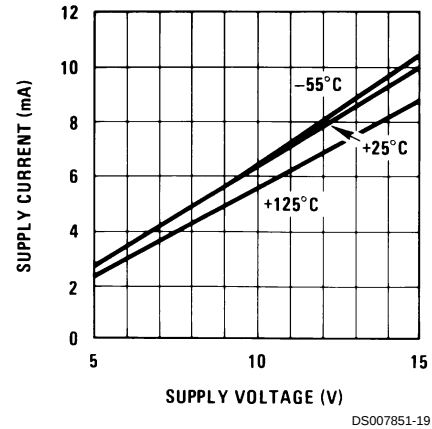
Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics

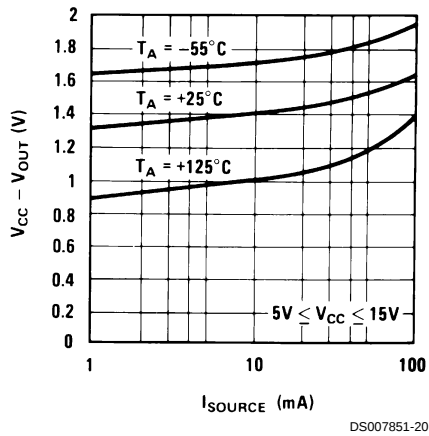
Minimum Pulse Width
Required for Triggering



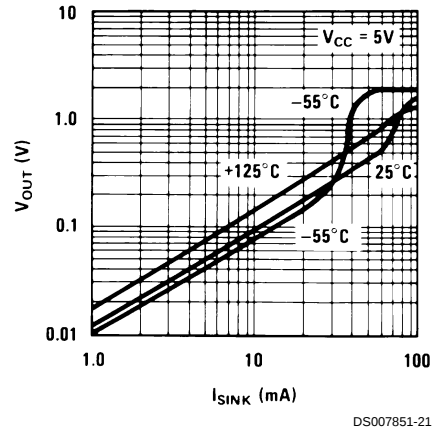
Supply Current vs.
Supply Voltage



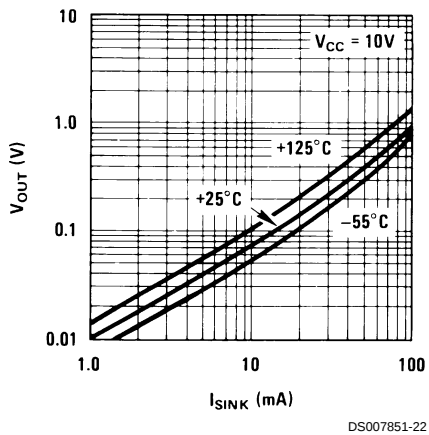
High Output Voltage vs.
Output Source Current



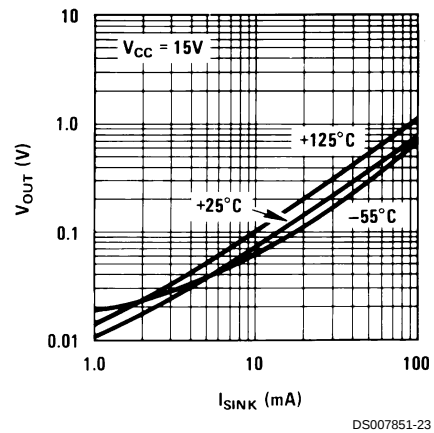
Low Output Voltage vs.
Output Sink Current



Low Output Voltage vs.
Output Sink Current

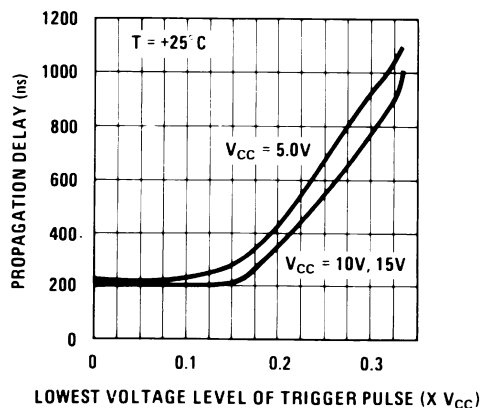


Low Output Voltage vs.
Output Sink Current



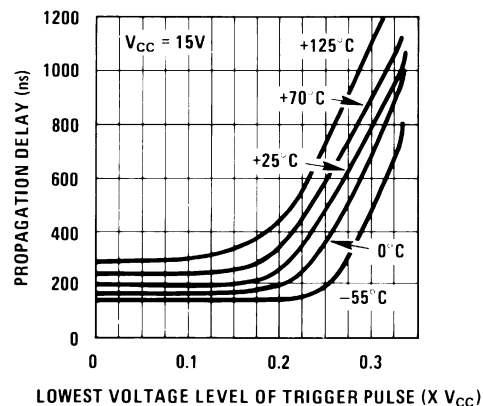
Typical Performance Characteristics (Continued)

Output Propagation Delay vs.
Voltage Level of Trigger Pulse



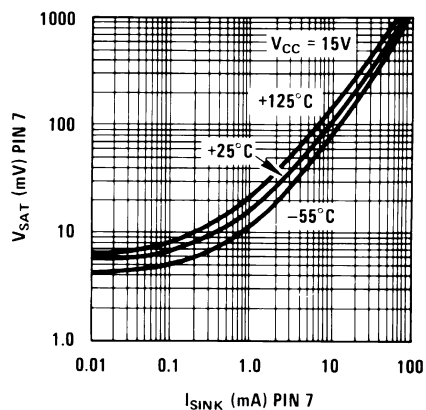
DS007851-24

Output Propagation Delay vs.
Voltage Level of Trigger Pulse



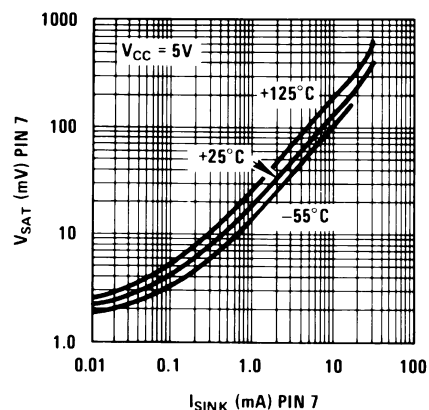
DS007851-25

Discharge Transistor (Pin 7)
Voltage vs. Sink Current



DS007851-26

Discharge Transistor (Pin 7)
Voltage vs. Sink Current

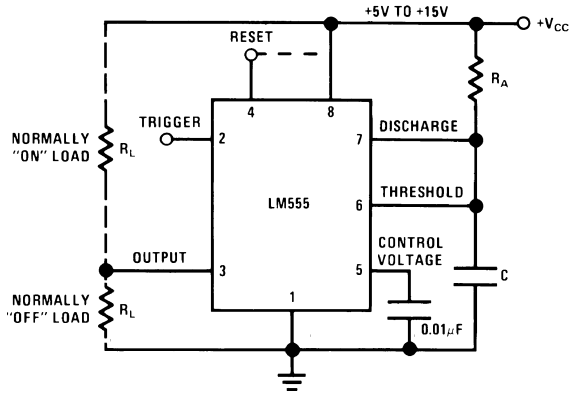


DS007851-27

Applications Information

MONOSTABLE OPERATION

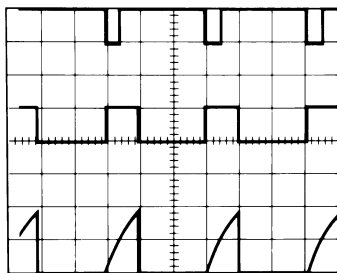
In this mode of operation, the timer functions as a one-shot (Figure 1). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than $1/3 V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



DS007851-5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1 R_A C$, at the end of which time the voltage equals $2/3 V_{CC}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 2 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



DS007851-6

$V_{CC} = 5V$
 TIME = 0.1 ms/DIV.
 $R_A = 9.1k\Omega$
 $C = 0.01\mu F$

Top Trace: Input 5V/Div.
 Middle Trace: Output 5V/Div.
 Bottom Trace: Capacitor Voltage 2V/Div.

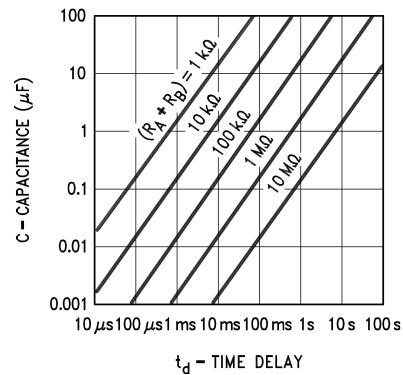
FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least $10\mu s$ before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

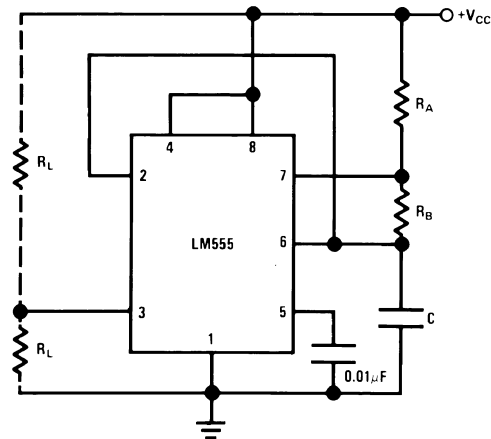


DS007851-7

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in Figure 4 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B . Thus the duty cycle may be precisely set by the ratio of these two resistors.



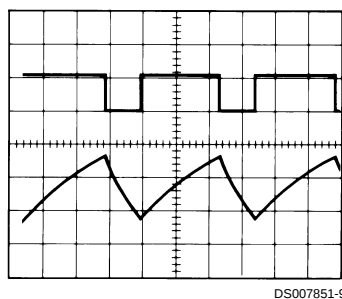
DS007851-8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between $1/3 V_{CC}$ and $2/3 V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



$V_{CC} = 5V$
 TIME = 20 μ s/DIV. Top Trace: Output 5V/Div.
 $R_A = 3.9k\Omega$ Bottom Trace: Capacitor Voltage 1V/Div.
 $R_B = 3k\Omega$
 $C = 0.01\mu F$

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

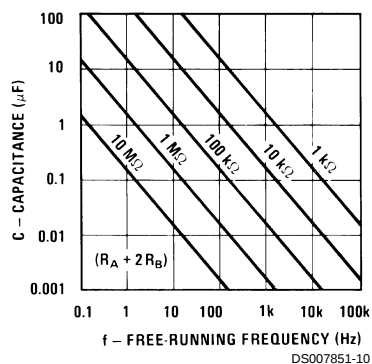
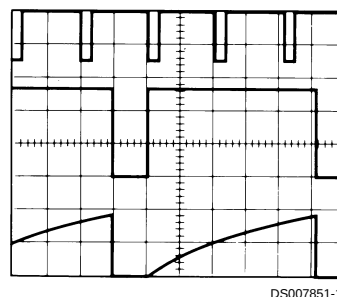


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of Figure 1 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 7 shows the waveforms generated in a divide by three circuit.



$V_{CC} = 5V$ Top Trace: Input 4V/Div.
 TIME = 20 μ s/DIV. Middle Trace: Output 2V/Div.
 $R_A = 9.1k\Omega$ Bottom Trace: Capacitor 2V/Div.
 $C = 0.01\mu F$

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 8 shows the circuit, and in Figure 9 are some waveform examples.

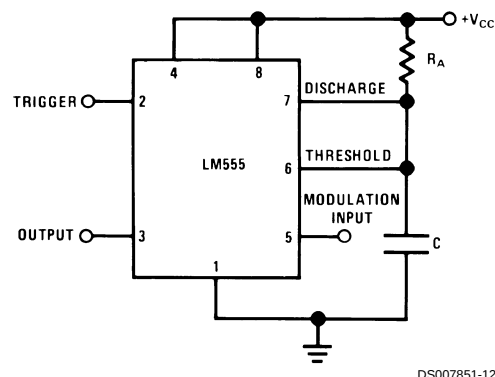
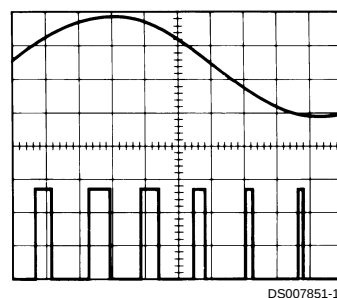


FIGURE 8. Pulse Width Modulator



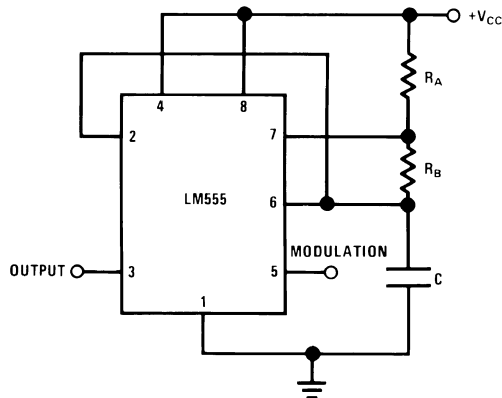
$V_{CC} = 5V$ Top Trace: Modulation 1V/Div.
 TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
 $R_A = 9.1k\Omega$
 $C = 0.01\mu F$

FIGURE 9. Pulse Width Modulator

Applications Information (Continued)

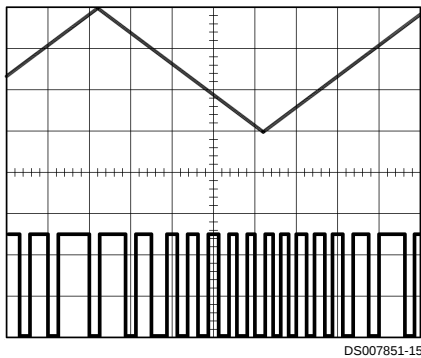
PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.



DS007851-14

FIGURE 10. Pulse Position Modulator



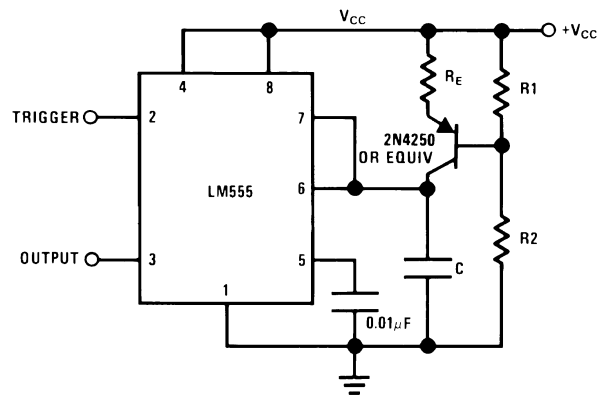
DS007851-15

$V_{CC} = 5V$
 $TIME = 0.1 \text{ ms/DIV.}$
 $R_A = 3.9k\Omega$
 $R_B = 3k\Omega$
 $C = 0.01\mu F$

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A , in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



DS007851-16

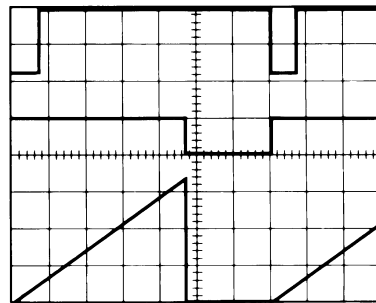
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3 V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE} (R_1 + R_2)}$$

$$V_{BE} \approx 0.6V$$

$$V_{BE} \approx 0.6V$$



DS007851-17

$V_{CC} = 5V$
 $TIME = 20\mu s/DIV.$
 $R_1 = 47k\Omega$
 $R_2 = 100k\Omega$
 $R_E = 2.7 k\Omega$
 $C = 0.01 \mu F$

FIGURE 13. Linear Ramp

Applications Information (Continued)

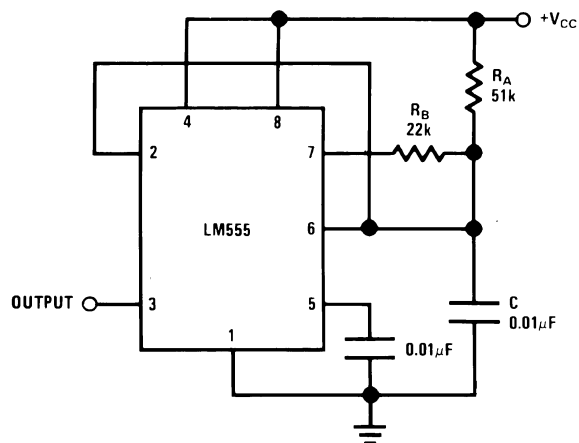
50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693 R_A C$. For the output low it is $t_2 =$

$$\left[(R_A R_B) / (R_A + R_B) \right] C \ln \left[\frac{R_B - 2R_A}{2R_B - R_A} \right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$



DS007851-18

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than $1/2 R_A$ because the junction of R_A and R_B cannot bring pin 2 down to $1/3 V_{CC}$ and trigger the lower comparator.

ADDITIONAL INFORMATION

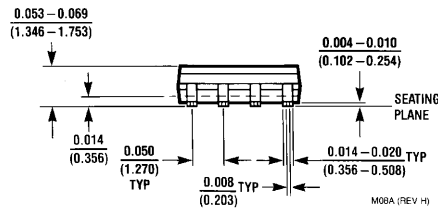
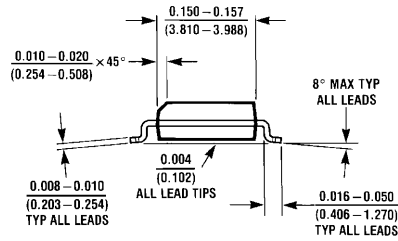
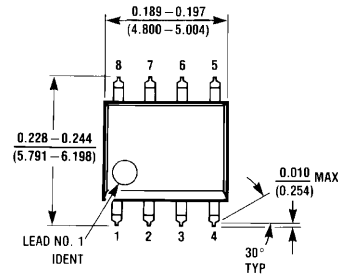
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is $0.1\mu F$ in parallel with $1\mu F$ electrolytic.

Lower comparator storage time can be as long as $10\mu s$ when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to $10\mu s$ minimum.

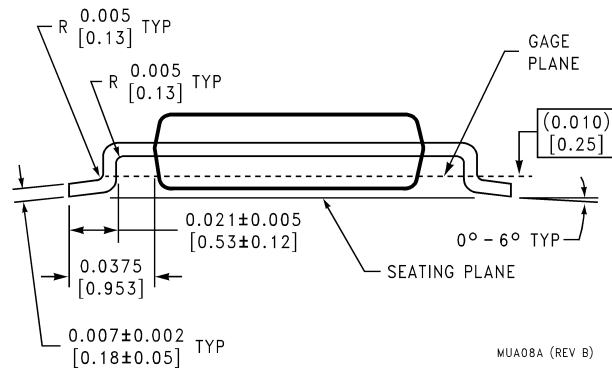
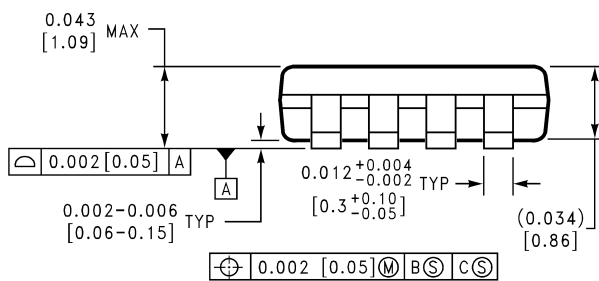
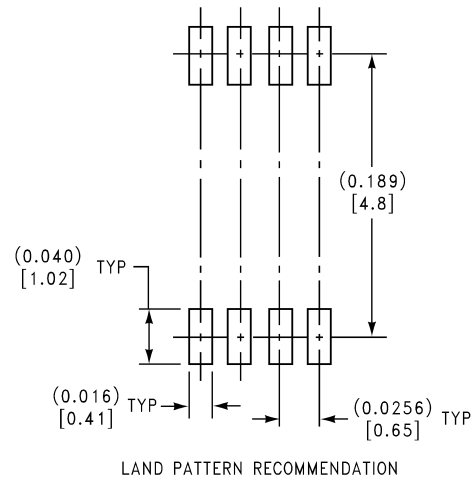
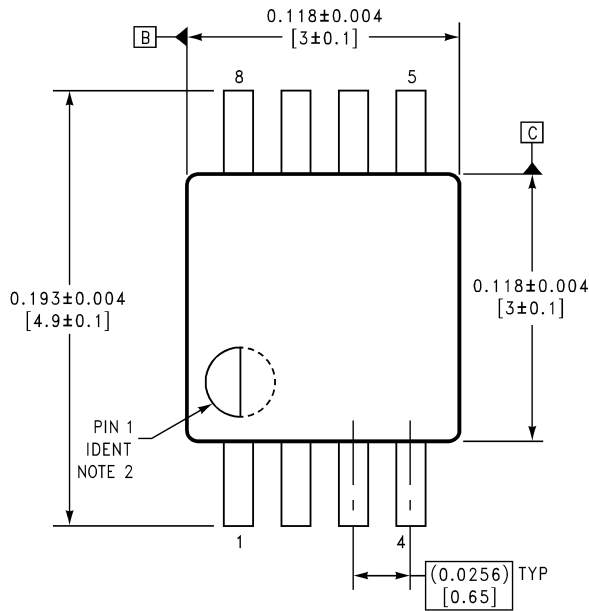
Delay time reset to output is $0.47\mu s$ typical. Minimum reset pulse width must be $0.3\mu s$, typical.

Pin 7 current switches within $30ns$ of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

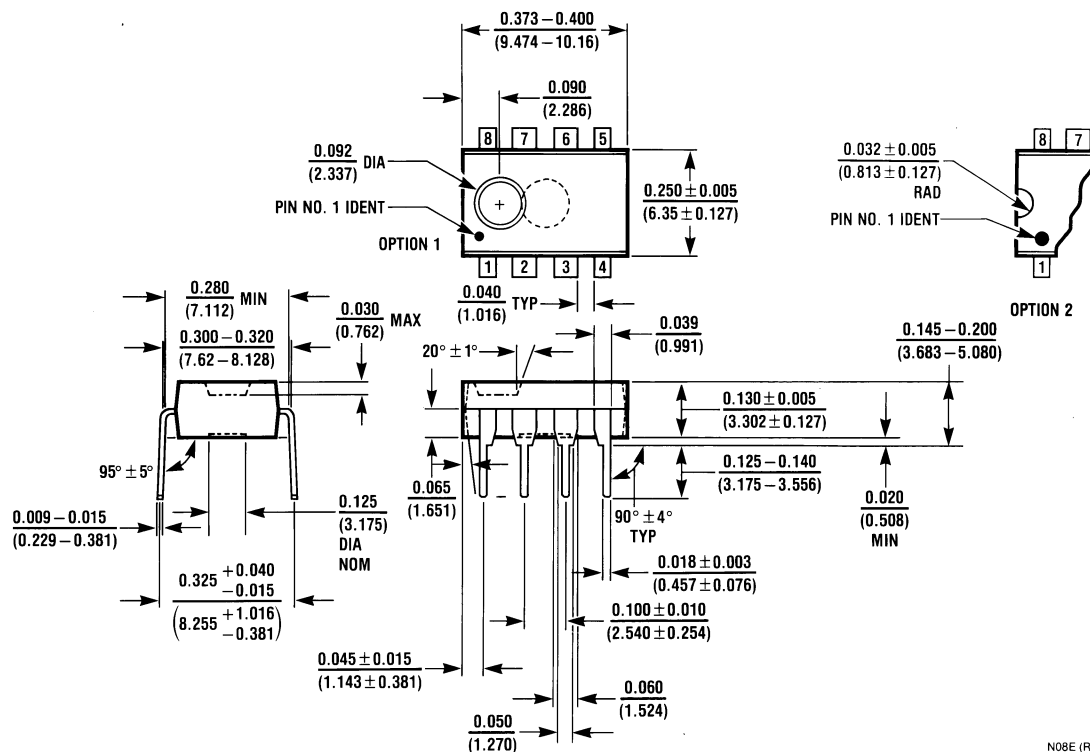


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

N08E (REV F)

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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Fax: 81-3-5639-7507

8-Bit CMOS Flash/EEPROM Microcontrollers

Devices Included in this Data Sheet:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84
- Extended voltage range devices available (PIC16LF8X, PIC16LCR8X)

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single cycle (400 ns @ 10 MHz) except for program branches which are two-cycle
- Operating speed: DC - 10 MHz clock input
DC - 400 ns instruction cycle

Device	Memory			Freq Max.
	Flash	Data		
		RAM	EEPROM	
PIC16F83	512 words	36	64	10 MHz
PIC16CR83	512 words	36	64	10 MHz
PIC16F84	1 K-words	68	64	10 MHz
PIC16CR84	1 K-words	68	64	10 MHz

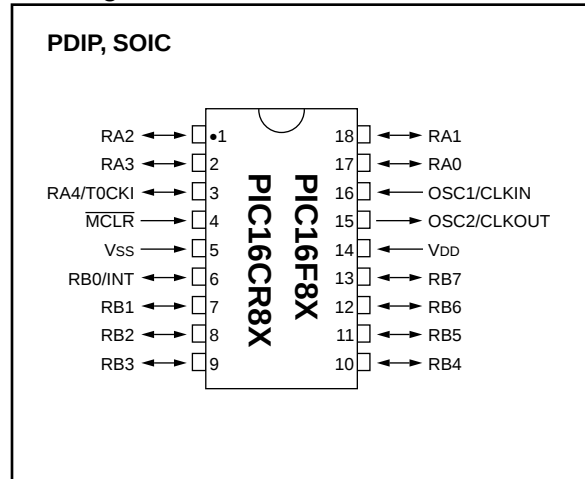
F = Flash; CR = ROM

- 14-bit wide instructions
- 8-bit wide data path
- 15 special function hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
 - External RB0/INT pin
 - TMR0 timer overflow
 - PORTB<7:4> interrupt on change
 - Data EEPROM write complete
- 1,000,000 data memory EEPROM ERASE/WRITE cycles
- EEPROM Data Retention > 40 years

Peripheral Features:

- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
 - 25 mA sink max. per pin
 - 20 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Pin Diagram



Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Code-protection
- Power saving SLEEP mode
- Selectable oscillator options
- Serial In-System Programming - via two pins (ROM devices support only Data EEPROM programming)

CMOS Technology:

- Low-power, high-speed CMOS Flash/EEPROM technology
- Fully static design
- Wide operating voltage range:
 - Commercial: 2.0V to 6.0V
 - Industrial: 2.0V to 6.0V
- Low power consumption:
 - < 2 mA typical @ 5V, 4 MHz
 - 15 µA typical @ 2V, 32 kHz
 - < 1 µA typical standby current @ 2V

PIC16F8X

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To Our Valued Customers

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1.0 GENERAL DESCRIPTION

The PIC16F8X is a group in the PIC16CXX family of low-cost, high-performance, CMOS, fully-static, 8-bit microcontrollers. This group contains the following devices:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84

All PIC16/17 microcontrollers employ an advanced RISC architecture. PIC16CXX devices have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with a separate 8-bit wide data bus. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set is used to achieve a very high performance level.

PIC16F8X microcontrollers typically achieve a 2:1 code compression and up to a 2:1 speed improvement (at 10 MHz) over other 8-bit microcontrollers in their class.

The PIC16F8X has up to 68 bytes of RAM, 64 bytes of Data EEPROM memory, and 13 I/O pins. A timer/counter is also available.

The PIC16CXX family has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. There are four oscillator options, of which the single pin RC oscillator provides a low-cost solution, the LP oscillator minimizes power consumption, XT is a standard crystal, and the HS is for High Speed crystals. The SLEEP (power-down) mode offers power saving. The user can wake the chip from sleep through several external and internal interrupts and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

The devices with Flash program memory allow the same device package to be used for prototyping and production. In-circuit reprogrammability allows the code to be updated without the device being removed from the end application. This is useful in the development of many applications where the device may not be easily accessible, but the prototypes may require code updates. This is also useful for remote applications where the code may need to be updated (such as rate information).

Table 1-1 lists the features of the PIC16F8X, and Appendix D: list the features of all of the Microchip microcontrollers.

A simplified block diagram of the PIC16F8X is shown in Figure 3-1.

The PIC16F8X fits perfectly in applications ranging from high speed automotive and appliance motor control to low-power remote sensors, electronic locks, security devices and smart cards. The Flash/EEPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, security codes, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16F8X very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, serial communication, capture and compare, PWM functions and co-processor applications).

The serial in-system programming feature (via two pins) offers flexibility of customizing the product after complete assembly and testing. This feature can be used to serialize a product, store calibration data, or program the device with the current firmware before shipping.

1.1 Family and Upward Compatibility

Those users familiar with the PIC16C5X family of microcontrollers will realize that this is an enhanced version of the PIC16C5X architecture. Please refer to Appendix A: for a detailed list of enhancements. Code written for PIC16C5X can be easily ported to the PIC16F8X (Appendix B:).

1.2 Development Support

The PIC16CXX family is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

PIC16F8X

TABLE 1-1: PIC16F8X FAMILY OF DEVICES

	Clock				Memory				Peripherals		Features
	Maximum Frequency of Operation (MHz)				Program Memory						
	Flash	EEPROM	ROM		Data Memory (bytes)	Data EEPROM (bytes)	Timer Module(s)	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Packages
PIC16C84	10	—	1K	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F84 ⁽¹⁾	10	1K	—	—	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR84 ⁽¹⁾	10	—	—	1K	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16F83 ⁽¹⁾	10	512	—	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC
PIC16CR83 ⁽¹⁾	10	—	—	512	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16C8X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

2.0 PIC16F8X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements the proper device option can be selected using the information in this section. When placing orders, please use the "PIC16F8X Product Identification System" at the back of this data sheet to specify the correct part number.

There are four device "types" as indicated in the device number.

1. **F**, as in PIC16**F**84. These devices have Flash program memory and operate over the standard voltage range.
2. **LF**, as in PIC16**LF**84. These devices have Flash program memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**83. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**84. These devices have ROM program memory and operate over an extended voltage range.

When discussing memory maps and other architectural features, the use of **F** and **CR** also implies the **LF** and **LCR** versions.

2.1 Electrically Erasable Devices

These devices are offered in the lower cost plastic package, even though the device can be erased and reprogrammed. This allows the same device to be used for prototype development and pilot programs as well as production.

A further advantage of the electrically erasable version is that they can be erased and reprogrammed in-circuit, or by device programmers, such as Microchip's PICSTART® Plus or PRO MATE® II programmers.

2.2 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices have all Flash locations and configuration options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available.

For information on submitting a QTP code, please contact your Microchip Regional Sales Office.

2.3 Serialized Quick-Turnaround-Production (SQTPSM) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password or ID number.

For information on submitting a SQTP code, please contact your Microchip Regional Sales Office.

2.4 ROM Devices

Some of Microchip's devices have a corresponding device where the program memory is a ROM. These devices give a cost savings over Microchip's traditional user programmed devices (EPROM, EEPROM).

ROM devices (PIC16CR8X) do not allow serialization information in the program memory space. The user may program this information into the Data EEPROM.

For information on submitting a ROM code, please contact your Microchip Regional Sales Office.

PIC16F8X

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16CXX family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16CXX uses a Harvard architecture. This architecture has the program and data accessed from separate memories. So the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC16CXX opcodes are 14-bits wide, enabling single word instructions. The full 14-bit wide program memory bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions execute in a single cycle (400 ns @ 10 MHz) except for program branches.

The PIC16F83 and PIC16CR83 address 512 x 14 of program memory, and the PIC16F84 and PIC16CR84 address 1K x 14 program memory. All program memory is internal.

The PIC16CXX can directly or indirectly address its register files or data memory. All special function registers including the program counter are mapped in the data memory. An orthogonal (symmetrical) instruction set makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16CXX simple yet efficient. In addition, the learning curve is reduced significantly.

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), and the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram for the PIC16F8X is shown in Figure 3-1, its corresponding pin description is shown in Table 3-1.

PIC16F8X

FIGURE 3-1: PIC16F8X BLOCK DIAGRAM

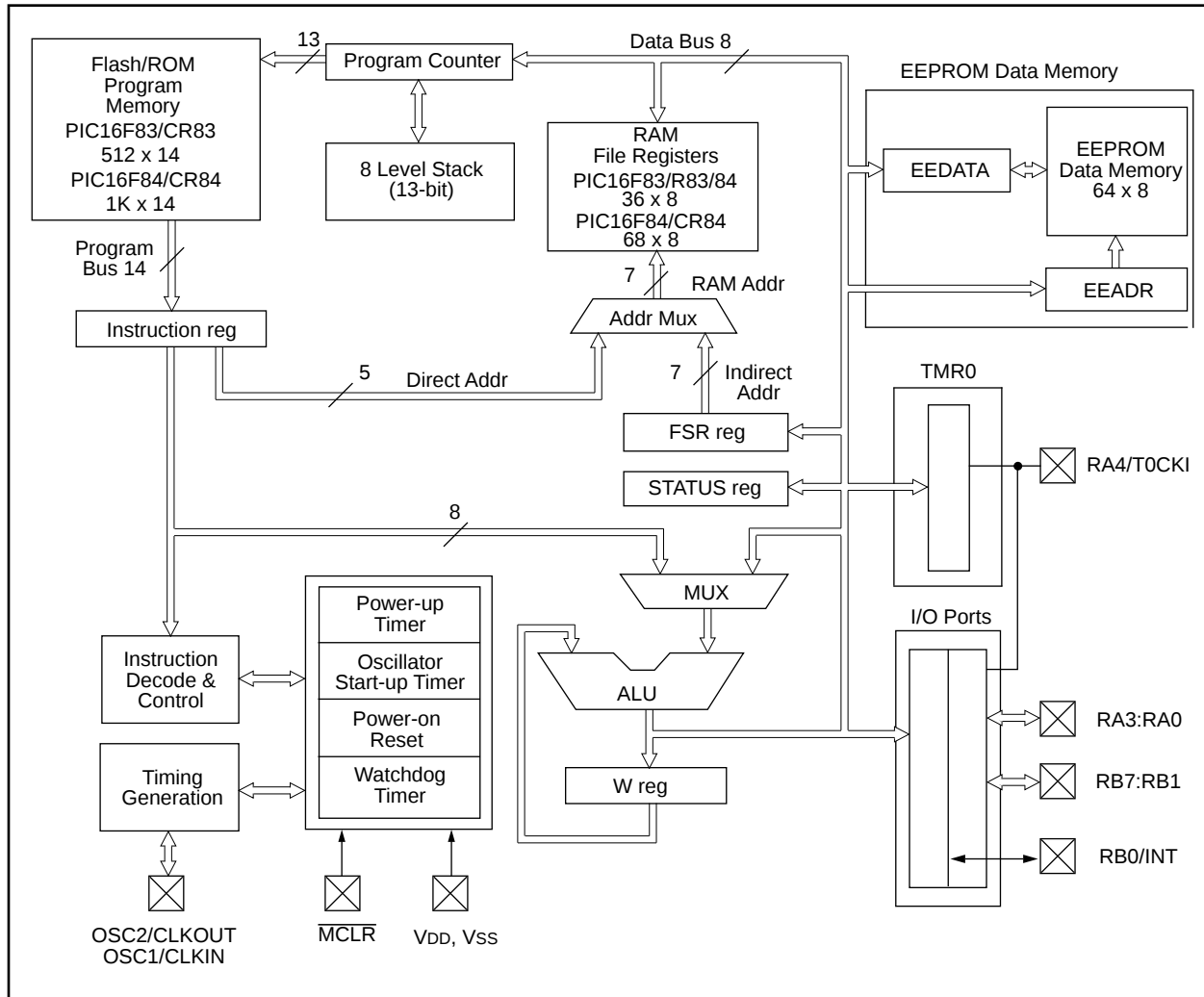


TABLE 3-1: PIC16F8X PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
RA0	17	17	I/O	TTL	PORTA is a bi-directional I/O port. Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	
RB0/INT	6	6	I/O	TTL/ST ⁽¹⁾	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0/INT can also be selected as an external interrupt pin. Interrupt on change pin. Interrupt on change pin. Interrupt on change pin. Serial programming clock. Interrupt on change pin. Serial programming data.
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	
RB5	11	11	I/O	TTL	
RB6	12	12	I/O	TTL/ST ⁽²⁾	
RB7	13	13	I/O	TTL/ST ⁽²⁾	
Vss	5	5	P	—	Ground reference for logic and I/O pins.
Vdd	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = Input/Output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 2: This buffer is a Schmitt Trigger input when used in serial programming mode.
 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

PIC16F8X

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

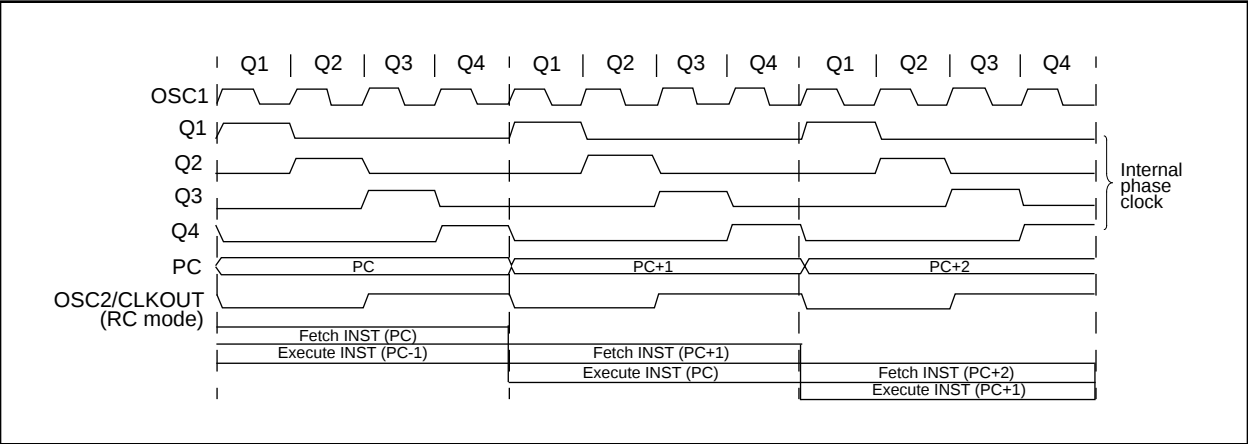
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

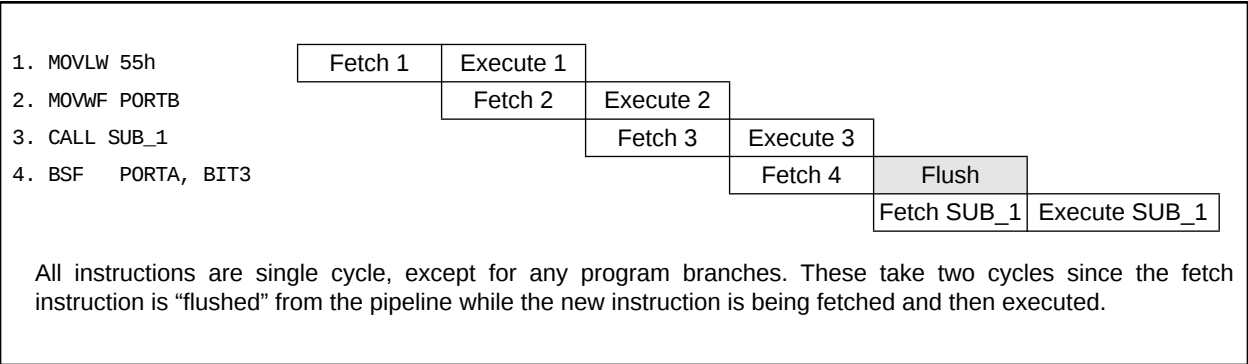
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



4.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F8X. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 7.0.

4.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F83 and PIC16CR83, the first 512 x 14 (0000h-01FFh) are physically implemented (Figure 4-1). For the PIC16F84 and PIC16CR84, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 4-2). Accessing a location above the physically implemented address will cause a wrap-around. For example, for the PIC16F84 locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK - PIC16F83/CR83

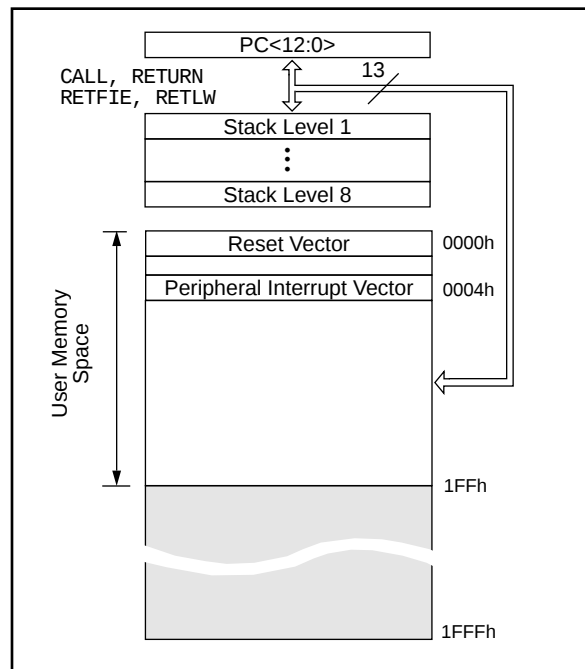
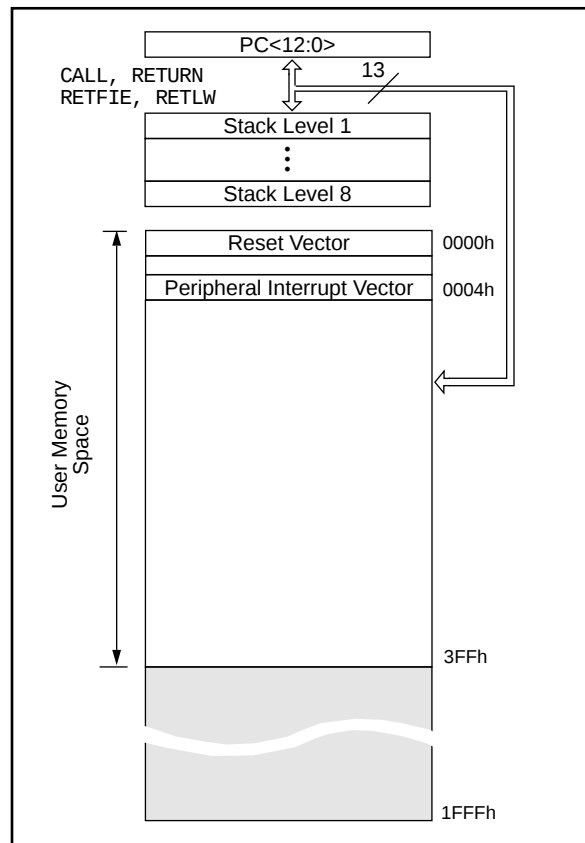


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK - PIC16F84/CR84



4.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 4-3 and Figure 4-4 show the data memory map organization.

Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 4.5). Indirect addressing uses the present value of the RP1:RP0 bits for access into the banked areas of data memory.

Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers implemented as static RAM.

4.2.1 GENERAL PURPOSE REGISTER FILE

All devices have some amount of General Purpose Register (GPR) area. Each GPR is 8 bits wide and is accessed either directly or indirectly through the FSR (Section 4.5).

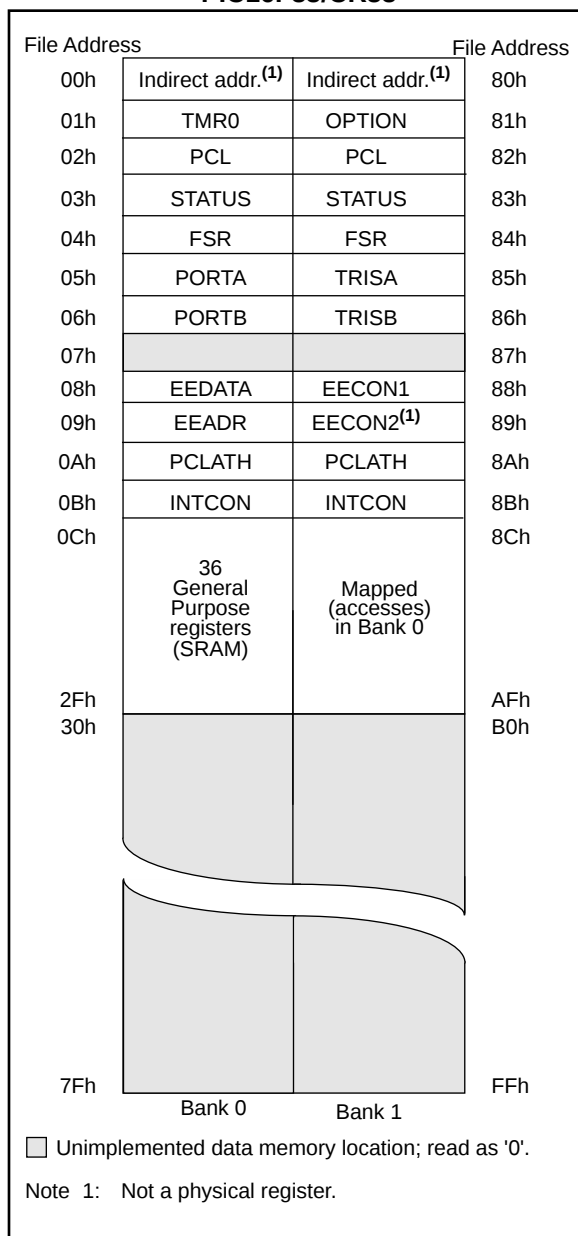
The GPR addresses in bank 1 are mapped to addresses in bank 0. As an example, addressing location 0Ch or 08h will access the same GPR.

4.2.2 SPECIAL FUNCTION REGISTERS

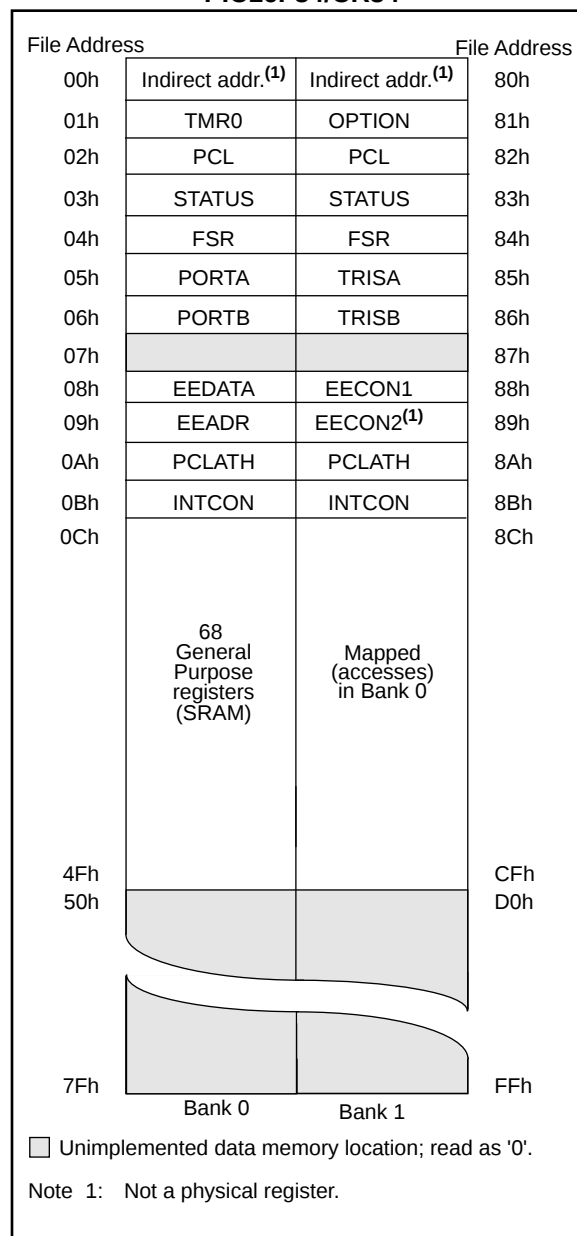
The Special Function Registers (Figure 4-3, Figure 4-4 and Table 4-1) are used by the CPU and Peripheral functions to control the device operation. These registers are static RAM.

The special function registers can be classified into two sets, core and peripheral. Those associated with the core functions are described in this section. Those related to the operation of the peripheral features are described in the section for that specific feature.

**FIGURE 4-3: REGISTER FILE MAP -
PIC16F83/CR83**



**FIGURE 4-4: REGISTER FILE MAP -
PIC16F84/CR84**



PIC16F8X

TABLE 4-1: REGISTER FILE SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets (Note3)
Bank 0											
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- --	---- --
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h	PCL	Low order 8 bits of the Program Counter (PC)								0000 0000	0000 0000
03h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	--x xxxx	--u uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
07h		Unimplemented location, read as '0'								---- --	---- --
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾				--0 0000	--0 0000	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
80h	INDF	Uses contents of FSR to address data memory (not a physical register)								---- --	---- --
81h	OPTION	RBP $\overline{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h	PCL	Low order 8 bits of Program Counter (PC)								0000 0000	0000 0000
83h	STATUS ⁽²⁾	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
84h	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
85h	TRISA	—	—	—	PORTA data direction register				--1 1111	--1 1111	
86h	TRISB	PORTB data direction register								1111 1111	1111 1111
87h		Unimplemented location, read as '0'								---- --	---- --
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	--0 x000	--0 q000
89h	EECON2	EEPROM control register 2 (not a physical register)								---- --	---- --
0Ah	PCLATH	—	—	—	Write buffer for upper 5 bits of the PC ⁽¹⁾				--0 0000	--0 0000	
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged. - = unimplemented read as '0', q = value depends on condition.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a slave register for PC<12:8>. The contents of PCLATH can be transferred to the upper byte of the program counter, but the contents of PC<12:8> is never transferred to PCLATH.

2: The $\overline{TO}$ and $\overline{PD}$ status bits in the STATUS register are not affected by a $\overline{MCLR}$ reset.

3: Other (non power-up) resets include: external reset through $\overline{MCLR}$ and the Watchdog Timer Reset.

4.2.2.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u = unchanged).

Only the BCF, BSF, SWAPF and MOVWF instructions should be used to alter the STATUS register (Table 9-2) because these instructions do not affect any status bit.

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F8X and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

Note 3: When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

FIGURE 4-5: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **IRP:** Register Bank Select bit (used for indirect addressing)
0 = Bank 0, 1 (00h - FFh)
1 = Bank 2, 3 (100h - 1FFh)
The IRP bit is not used by the PIC16F8X. IRP should be maintained clear.

bit 6-5: **RP1:RP0:** Register Bank Select bits (used for direct addressing)
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
10 = Bank 2 (100h - 17Fh)
11 = Bank 3 (180h - 1FFh)
Each bank is 128 bytes. Only bit RP0 is used by the PIC16F8X. RP1 should be maintained clear.

bit 4: **$\overline{TO}$:** Time-out bit
1 = After power-up, CLRWDI instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$:** Power-down bit
1 = After power-up or by the CLRWDI instruction
0 = By execution of the SLEEP instruction

bit 2: **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (for ADDWF and ADDLW instructions) (For borrow the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0: **C:** Carry/borrow bit (for ADDWF and ADDLW instructions)
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred

Note:For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register.

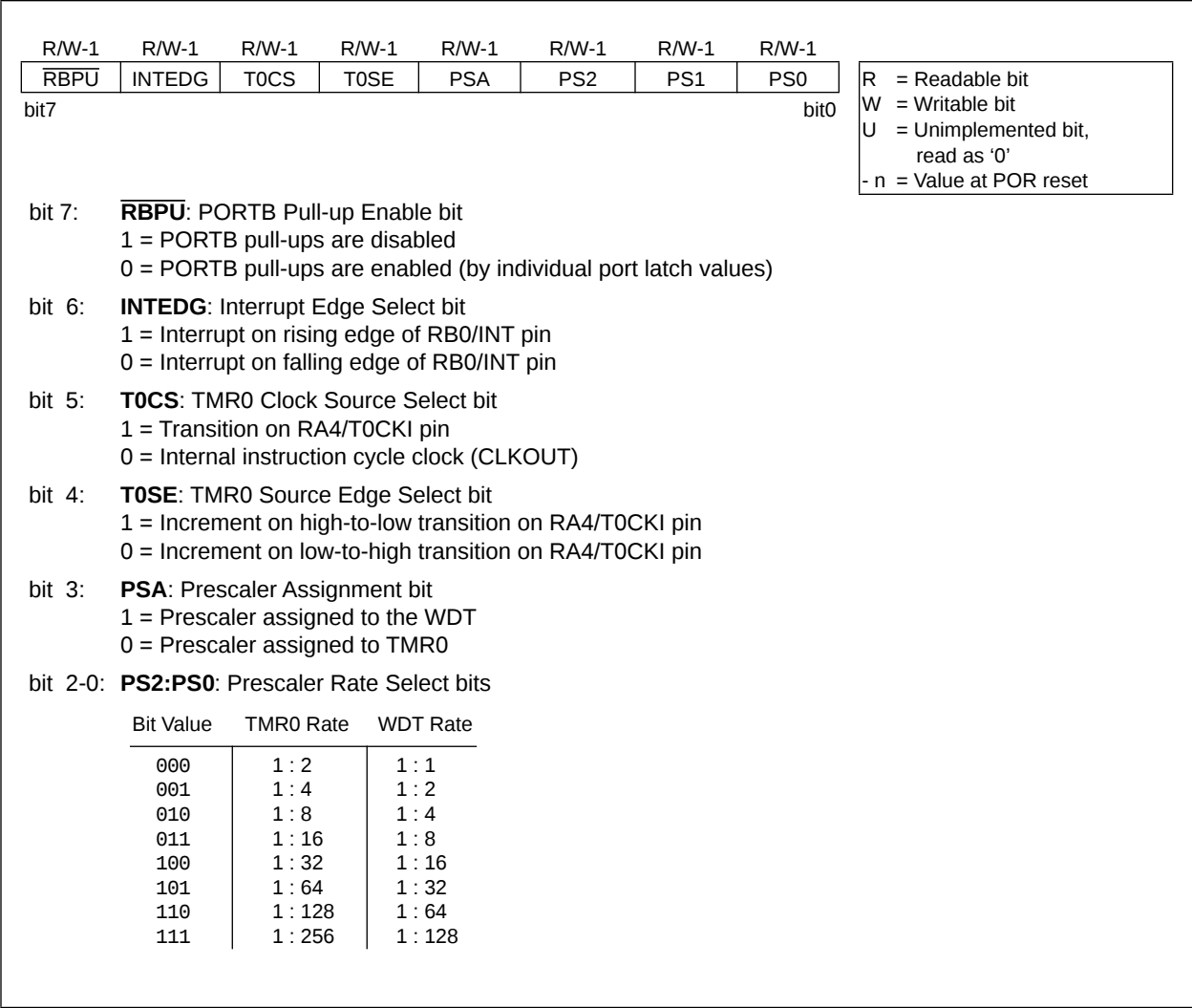
PIC16F8X

4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the external INT interrupt, TMR0, and the weak pull-ups on PORTB.

Note: When the prescaler is assigned to the WDT (PSA = '1'), TMR0 has a 1:1 prescaler assignment.

FIGURE 4-6: OPTION REGISTER (ADDRESS 81h)



4.2.2.3 INTCON REGISTER

The INTCON register is a readable and writable register which contains the various enable bits for all interrupt sources.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-7: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF
bit7							bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7: **GIE:** Global Interrupt Enable bit
1 = Enables all un-masked interrupts
0 = Disables all interrupts

Note: For the operation of the interrupt structure, please refer to Section 8.5.

bit 6: **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 5: **TOIE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4: **INTE:** RB0/INT Interrupt Enable bit
1 = Enables the RB0/INT interrupt
0 = Disables the RB0/INT interrupt

bit 3: **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2: **TOIF:** TMR0 overflow interrupt flag bit
1 = TMR0 has overflowed (must be cleared in software)
0 = TMR0 did not overflow

bit 1: **INTF:** RB0/INT Interrupt Flag bit
1 = The RB0/INT interrupt occurred
0 = The RB0/INT interrupt did not occur

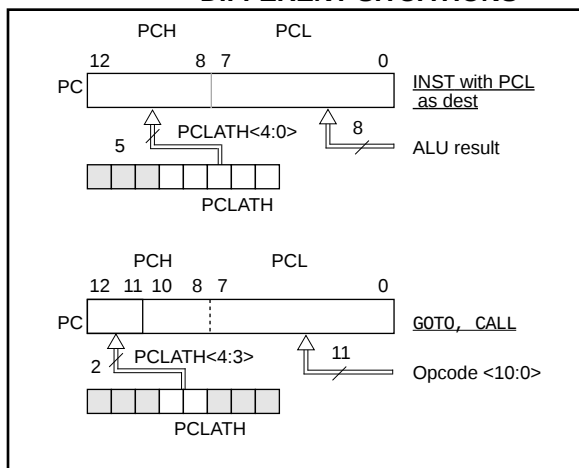
bit 0: **RBIF:** RB Port Change Interrupt Flag bit
1 = When at least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

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4.3 Program Counter: PCL and PCLATH

The Program Counter (PC) is 13-bits wide. The low byte is the PCL register, which is a readable and writable register. The high byte of the PC (PC<12:8>) is not directly readable nor writable and comes from the PCLATH register. The PCLATH (PC latch high) register is a holding register for PC<12:8>. The contents of PCLATH are transferred to the upper byte of the program counter when the PC is loaded with a new value. This occurs during a CALL, GOTO or a write to PCL. The high bits of PC are loaded from PCLATH as shown in Figure 4-8.

FIGURE 4-8: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 word block). Refer to the application note "Implementing a Table Read" (AN556).

4.3.2 PROGRAM MEMORY PAGING

The PIC16F83 and PIC16CR83 have 512 words of program memory. The PIC16F84 and PIC16CR84 have 1K of program memory. The CALL and GOTO instructions have an 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. For future PIC16F8X program memory expansion, there must be another two bits to specify the program memory page. These paging bits come from the PCLATH<4:3> bits (Figure 4-8). When doing a CALL or a GOTO instruction, the user must ensure that these page bits (PCLATH<4:3>) are programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is "pushed" onto the stack (see next section). Therefore,

manipulation of the PCLATH<4:3> is not required for the return instructions (which "pops" the PC from the stack).

Note: The PIC16F8X ignores the PCLATH<4:3> bits, which are used for program memory pages 1, 2 and 3 (0800h - 1FFFh). The use of PCLATH<4:3> as general purpose R/W bits is not recommended since this may affect upward compatibility with future products.

4.4 Stack

The PIC16FXX has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable.

The entire 13-bit PC is "pushed" onto the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is "popped" in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a push or a pop operation.

Note: There are no instruction mnemonics called push or pop. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

The stack operates as a circular buffer. That is, after the stack has been pushed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

If the stack is effectively popped nine times, the PC value is the same as the value from the first pop.

Note: There are no status bits to indicate stack overflow or stack underflow conditions.

4.5 Indirect Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

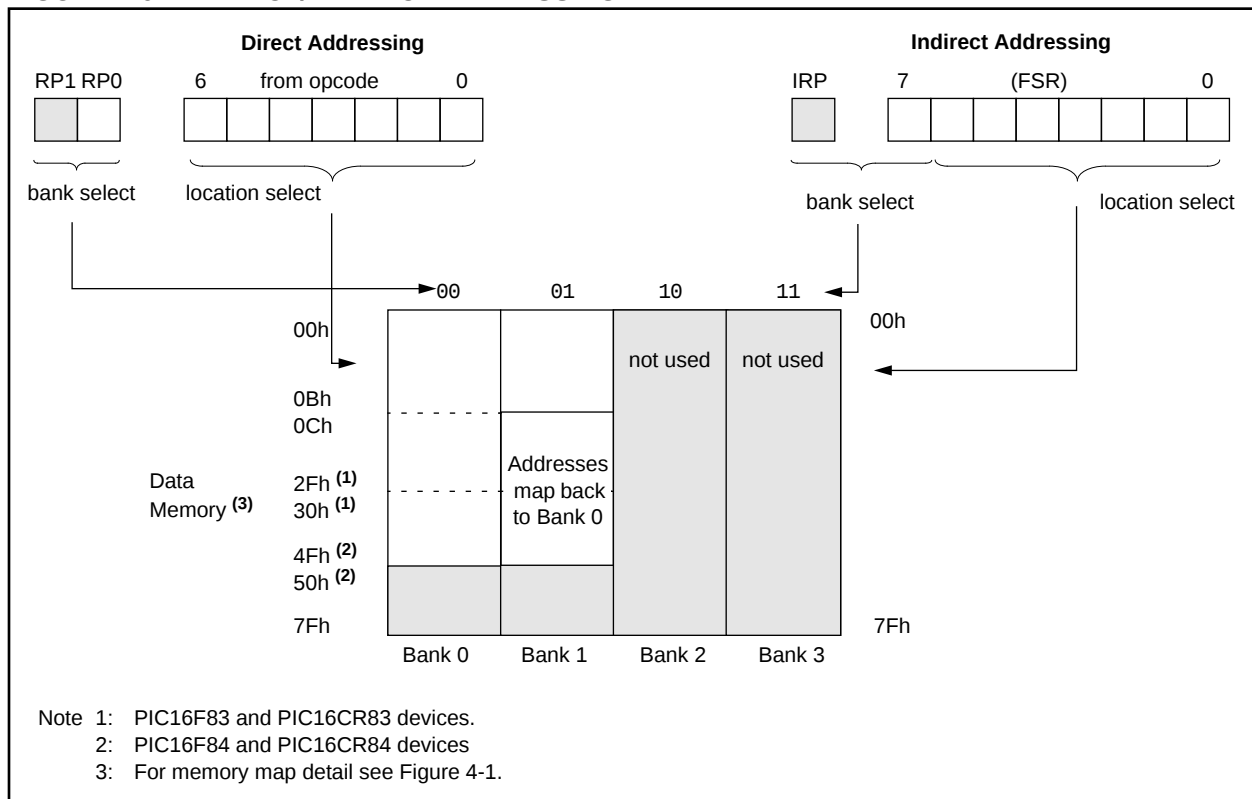
```

movlw 0x20 ;initialize pointer
movwf FSR ; to RAM
NEXT   clrf INDF ;clear INDF register
       incf FSR ;inc pointer
       btfss FSR,4 ;all done?
       goto NEXT ;NO, clear next

CONTINUE
       : ;YES, continue
    
```

An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-9. However, IRP is not used in the PIC16F8X.

FIGURE 4-9: DIRECT/INDIRECT ADDRESSING



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NOTES:

5.0 I/O PORTS

The PIC16F8X has two ports, PORTA and PORTB. Some port pins are multiplexed with an alternate function for other features on the device.

5.1 PORTA and TRISA Registers

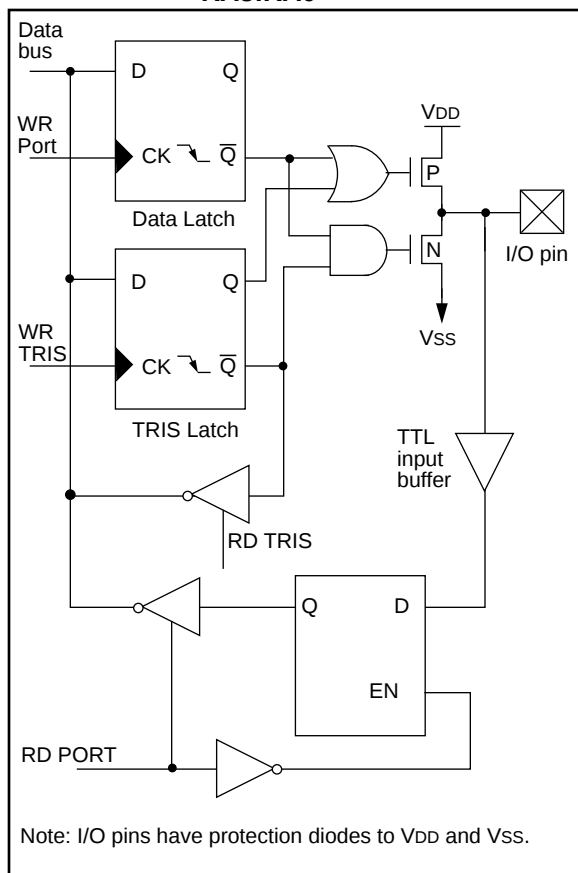
PORTA is a 5-bit wide latch. RA4 is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers. All pins have data direction bits (TRIS registers) which can configure these pins as output or input.

Setting a TRISA bit (=1) will make the corresponding PORTA pin an input, i.e., put the corresponding output driver in a hi-impedence mode. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output, i.e., put the contents of the output latch on the selected pin.

Reading the PORTA register reads the status of the pins whereas writing to it will write to the port latch. All write operations are read-modify-write operations. So a write to a port implies that the port pins are first read, then this value is modified and written to the port data latch.

The RA4 pin is multiplexed with the TMR0 clock input.

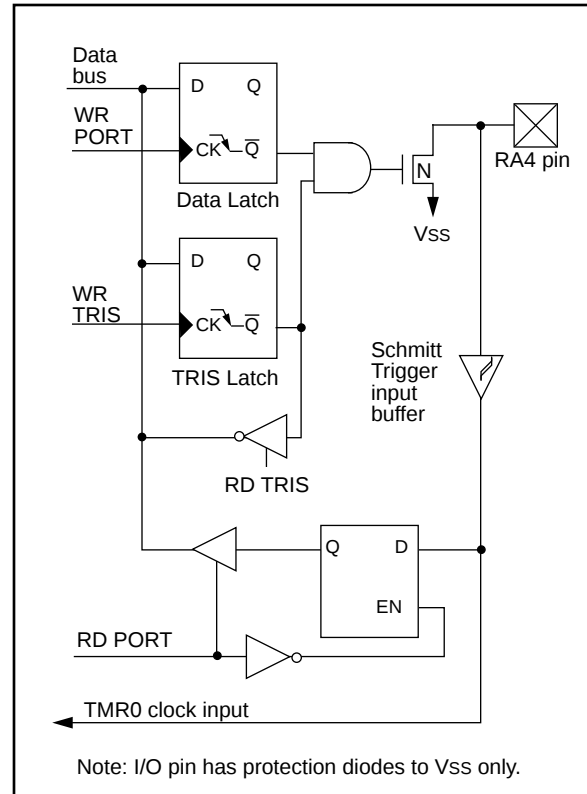
FIGURE 5-1: BLOCK DIAGRAM OF PINS RA3:RA0



EXAMPLE 5-1: INITIALIZING PORTA

```
CLRF    PORTA      ; Initialize PORTA by
                   ; setting output
                   ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0x0F       ; Value used to
                   ; initialize data
                   ; direction
MOVWF   TRISA       ; Set RA<3:0> as inputs
                   ; RA4 as outputs
                   ; TRISA<7:5> are always
                   ; read as '0'.
```

FIGURE 5-2: BLOCK DIAGRAM OF PIN RA4



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TABLE 5-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
05h	PORTA	—	—	—	RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are unimplemented, read as '0'

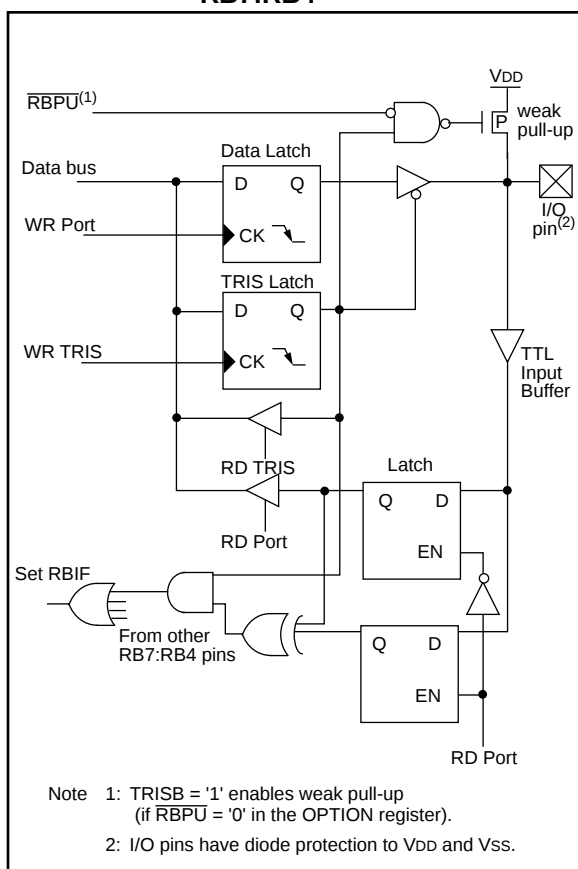
5.2 PORTB and TRISB Registers

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. A '1' on any bit in the TRISB register puts the corresponding output driver in a hi-impedance mode. A '0' on any bit in the TRISB register puts the contents of the output latch on the selected pin(s).

Each of the PORTB pins have a weak internal pull-up. A single control bit can turn on all the pull-ups. This is done by clearing the $\overline{\text{RBP}}\text{U}$ (OPTION<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The pins value in input mode are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of the pins are OR'ed together to generate the RB port change interrupt.

FIGURE 5-3: BLOCK DIAGRAM OF PINS RB7:RB4



This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- Read (or write) PORTB. This will end the mismatch condition.
- Clear flag bit RBIF.

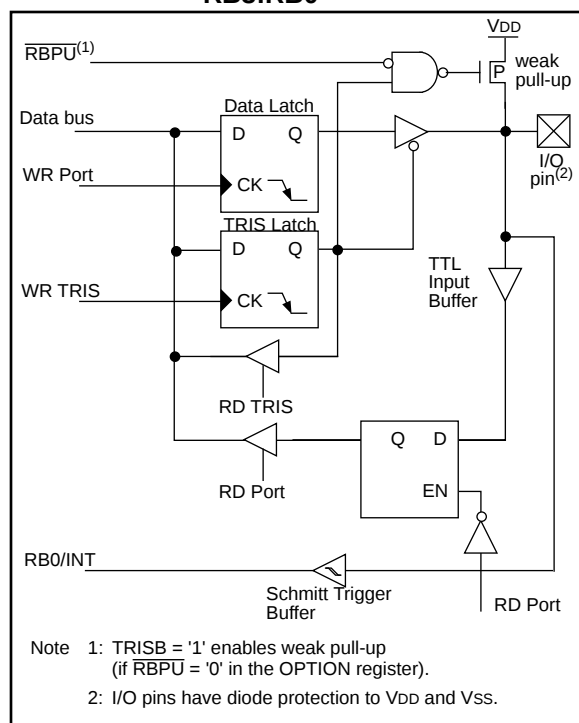
A mismatch condition will continue to set the RBIF bit. Reading PORTB will end the mismatch condition, and allow the RBIF bit to be cleared.

This interrupt on mismatch feature, together with software configurable pull-ups on these four pins allow easy interface to a key pad and make it possible for wake-up on key-depression (see AN552 in the Embedded Control Handbook).

Note 1: For a change on the I/O pin to be recognized, the pulse width must be at least T_{CY} wide.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

FIGURE 5-4: BLOCK DIAGRAM OF PINS RB3:RB0



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EXAMPLE 5-2: INITIALIZING PORTB

```
CLRF    PORTB      ; Initialize PORTB by
                   ; setting output
                   ; data latches
BSF     STATUS, RP0 ; Select Bank 1
MOVLW   0xCF        ; Value used to
                   ; initialize data
                   ; direction
MOVWF   TRISB       ; Set RB<3:0> as inputs
                   ; RB<5:4> as outputs
                   ; RB<7:6> as inputs
```

TABLE 5-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in serial programming mode.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION	RBP _U	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (i.e., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch is unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (i.e., BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output current may damage the chip.

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

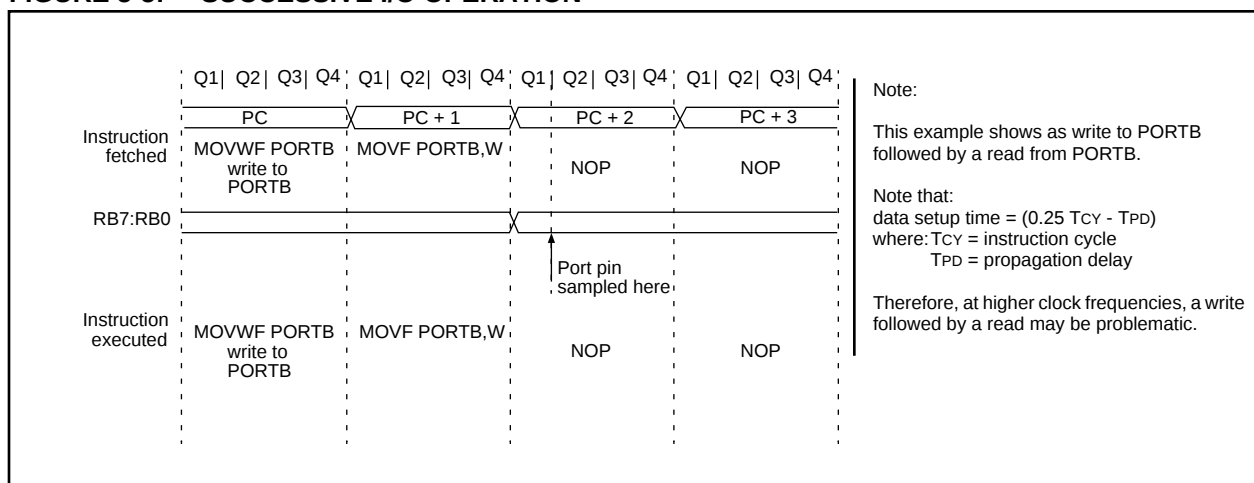
The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such that the pin voltage stabilizes (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

Example 5-3 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

EXAMPLE 5-3: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT settings: PORTB<7:4> Inputs
;                        PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                        PORT latch  PORT pins
;                        -----
;
BCF PORTB, 7    ; 01pp ppp   11pp ppp
BCF PORTB, 6    ; 10pp ppp   11pp ppp
BSF STATUS, RP0 ;
BCF TRISB, 7    ; 10pp ppp   11pp ppp
BCF TRISB, 6    ; 10pp ppp   10pp ppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

FIGURE 5-5: SUCCESSIVE I/O OPERATION



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NOTES:

6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module (Figure 6-1) will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-2 and Figure 6-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode TMR0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the T0 source

edge select bit, T0SE (OPTION<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.2.

The prescaler is shared between the Timer0 Module and the Watchdog Timer. The prescaler assignment is controlled, in software, by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 Module. The prescaler is not readable or writable. When the prescaler (Section 6.3) is assigned to the Timer0 Module, the prescale value (1:2, 1:4, ..., 1:256) is software selectable.

6.1 TMR0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets the TOIF bit (INTCON<2>). The interrupt can be masked by clearing enable bit T0IE (INTCON<5>). The TOIF bit must be cleared in software by the Timer0 Module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt (Figure 6-4) cannot wake the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 6-1: TMR0 BLOCK DIAGRAM

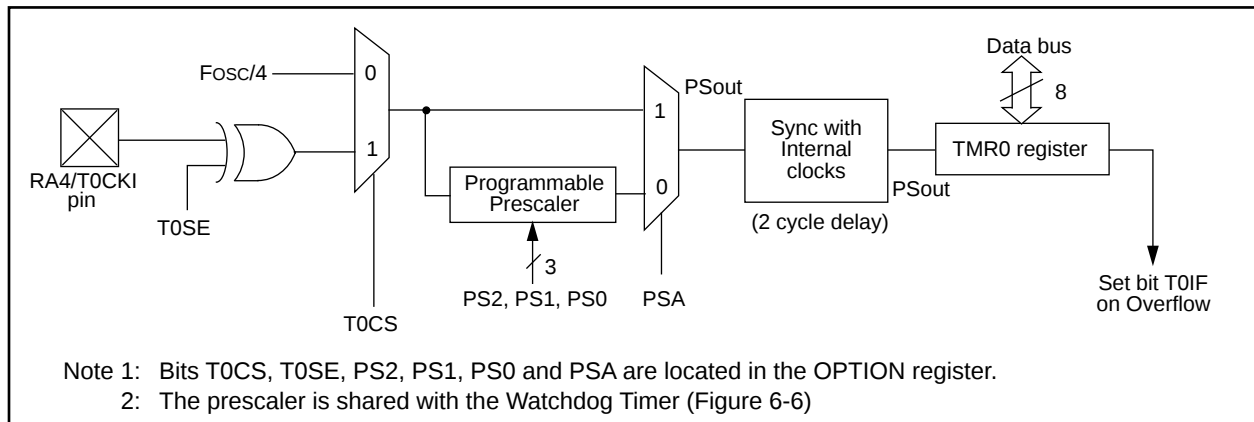
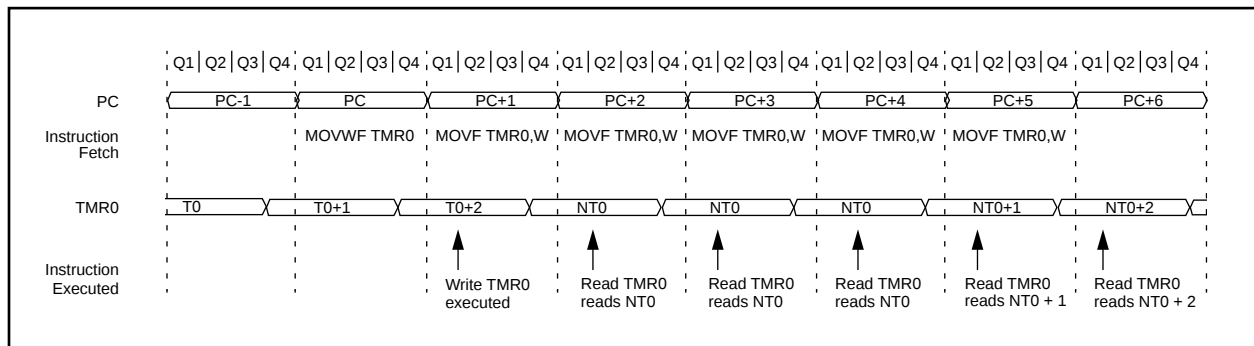


FIGURE 6-2: TMR0 TIMING: INTERNAL CLOCK/NO PRESCALER



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FIGURE 6-3: TMR0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

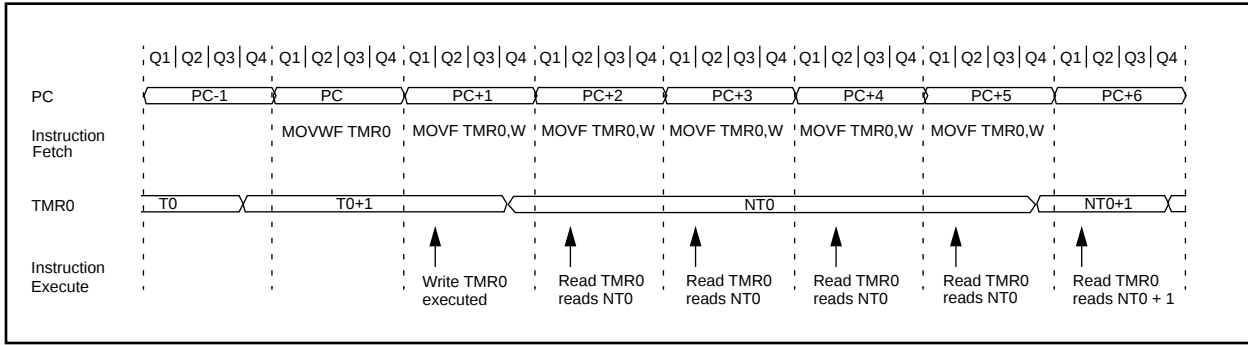
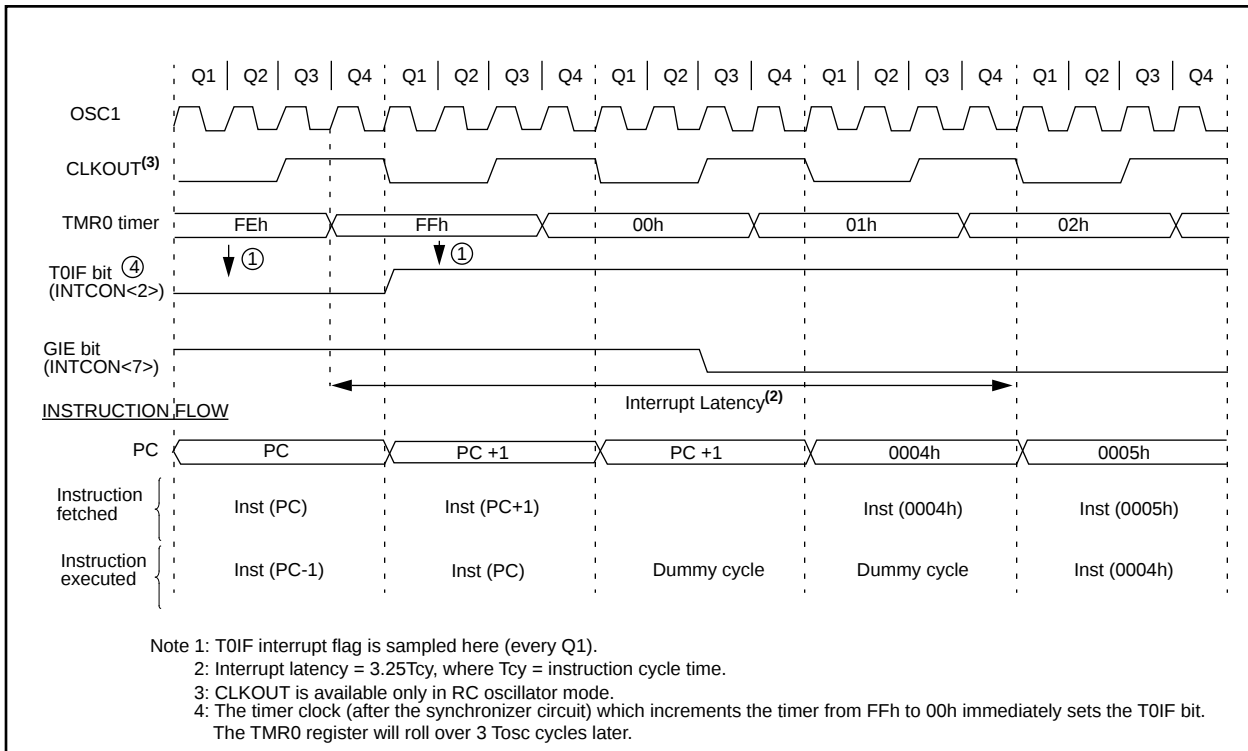


FIGURE 6-4: TMR0 INTERRUPT TIMING



6.2 Using TMR0 with External Clock

When an external clock input is used for TMR0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of the TMR0 register after synchronization.

6.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of pin RA4/T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (plus a small RC delay) and low for at least 2Tosc (plus a small RC delay). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by an asynchronous ripple counter type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (plus a small RC delay) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the AC Electrical Specifications of the desired device.

6.2.2 TMR0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 Module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

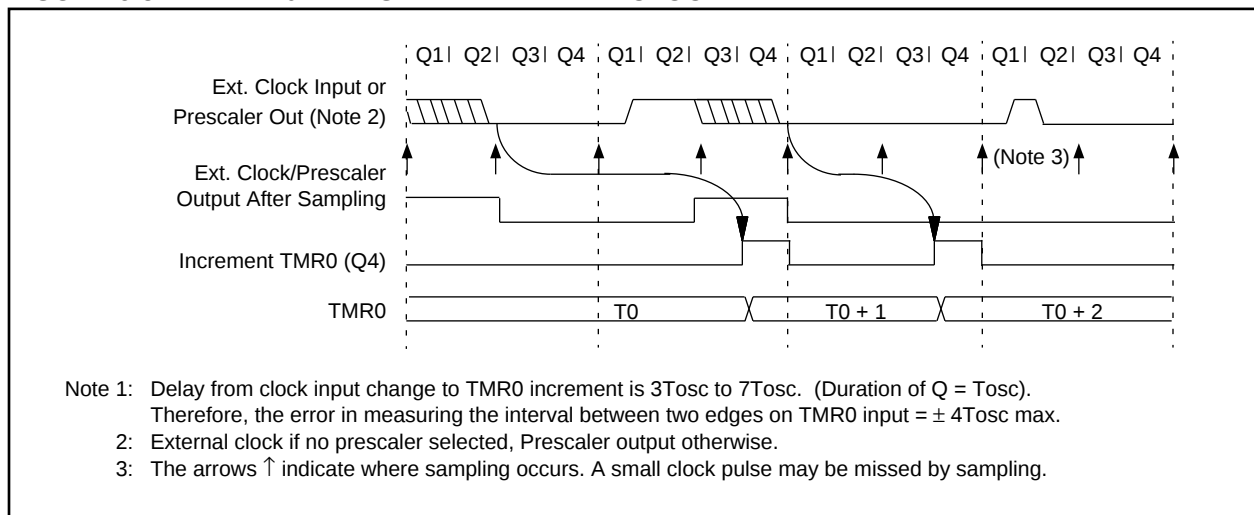
6.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 Module, or as a postscaler for the Watchdog Timer (Figure 6-6). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusive between the Timer0 Module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 Module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

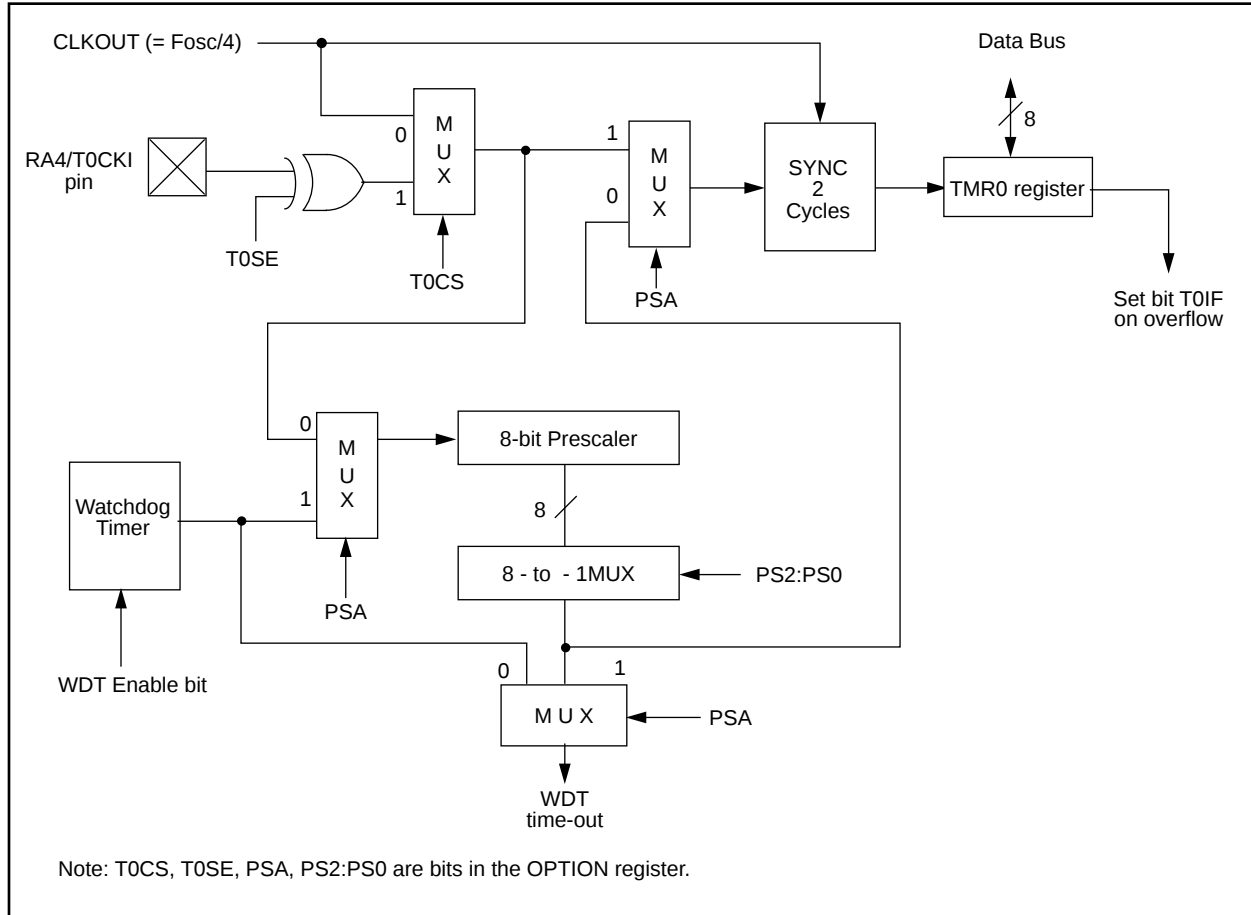
When assigned to the Timer0 Module, all instructions writing to the Timer0 Module (e.g., CLRF 1, MOVWF 1, BSF 1, x ...etc.) will clear the prescaler. When assigned to WDT, a CLRWD instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



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FIGURE 6-6: BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER



6.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution).

Note: To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be taken even if the WDT is disabled. To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 6-2.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF    STATUS, RP0    ;Bank 0
CLRF   TMR0           ;Clear TMR0
                        ; and Prescaler
BSF    STATUS, RP0    ;Bank 1
CLRWDT           ;Clears WDT
MOVLW  b'xxxx1xxx'    ;Select new
MOVWF  OPTION        ; prescale value
BCF    STATUS, RP0    ;Bank 0
```

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT           ;Clear WDT and
                  ; prescaler
BSF    STATUS, RP0    ;Bank 1
MOVLW  b'xxxx0xxx'    ;Select TMR0, new
                        ; prescale value
                        ; and clock source
MOVWF  OPTION        ;
BCF    STATUS, RP0    ;Bank 0
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh	INTCON	GIE	EEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 0000
81h	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged. - = unimplemented read as '0'. Shaded cells are not associated with Timer0.

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NOTES:

7.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F8X devices have 64 bytes of data EEPROM with an address range from 0h to 3Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

7.1 EEADR

The EEADR register can address up to a maximum of 256 bytes of data EEPROM. Only the first 64 bytes of data EEPROM are implemented.

The upper two bits are address decoded. This means that these two bits must always be '0' to ensure that the address is in the 64 byte memory space.

FIGURE 7-1: EECON1 REGISTER (ADDRESS 88h)

U	U	U	R/W-0	R/W-x	R/W-0	R/S-0	R/S-x
—	—	—	EEIF	WRERR	WREN	WR	RD
bit7							bit0

R = Readable bit
W = Writable bit
S = Settable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7:5 **Unimplemented:** Read as '0'

bit 4 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 **WRERR:** EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any MCLR reset or any WDT reset during normal operation)
0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
1 = initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
1 = Initiates an EEPROM read (read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software).
0 = Does not initiate an EEPROM read

7.2 EECON1 and EECN2 Registers

EECON1 is the control register with five low order bits physically implemented. The upper-three bits are non-existent and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR reset or a WDT time-out reset during normal operation. In these situations, following reset, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDATA and EEADR registers.

Interrupt flag bit EEIF is set when write is complete. It must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the Data EEPROM write sequence.

7.3 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>). The data is available, in the very next cycle, in the EEDATA register; therefore it can be read in the next instruction. EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 7-1: DATA EEPROM READ

```
BCF    STATUS, RP0    ; Bank 0
MOVLW  CONFIG_ADDR    ;
MOVWF  EEADR          ; Address to read
BSF    STATUS, RP0    ; Bank 1
BSF    EECN1, RD      ; EE Read
BCF    STATUS, RP0    ; Bank 0
MOVF   EEDATA, W      ; W = EEDATA
```

7.4 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte.

EXAMPLE 7-2: DATA EEPROM WRITE

	BSF	STATUS, RP0	; Bank 1
	BCF	INTCON, GIE	; Disable INTs.
	BSF	EECON1, WREN	; Enable Write
Required Sequence	MOVLW	55h	;
	MOVWF	EECON2	; Write 55h
	MOVLW	AAh	;
	MOVWF	EECON2	; Write AAh
	BSF	EECON1, WR	; Set WR bit
			; begin write
	BSF	INTCON, GIE	; Enable INTs.

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

7.5 Write Verify

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (Example 7-3) to the desired value to be written. This should be used in applications where an EEPROM bit will be stressed near the specification limit. The Total Endurance disk will help determine your comfort level.

Generally the EEPROM write failure will be a bit which was written as a '1', but reads back as a '0' (due to leakage off the bit).

EXAMPLE 7-3: WRITE VERIFY

```

BCF  STATUS, RP0 ; Bank 0
:      ; Any code can go here
:      ;
MOVF  EEDATA, W   ; Must be in Bank 0
BSF  STATUS, RP0 ; Bank 1
READ
BSF  EECON1, RD   ; YES, Read the
:      ; value written
BCF  STATUS, RP0 ; Bank 0
;
; Is the value written (in W reg) and
; read (in EEDATA) the same?
;
SUBWF EEDATA, W   ;
BTFSZ STATUS, Z   ; Is difference 0?
GOTO  WRITE_ERR   ; NO, Write error
:      ; YES, Good write
:      ; Continue program

```

7.6 Protection Against Spurious Writes

There are conditions when the device may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch, or software malfunction.

7.7 Data EEPROM Operation during Code Protect

When the device is code protected, the CPU is able to read and write unscrambled data to the Data EEPROM.

For ROM devices, there are two code protection bits (Section 8.1). One for the ROM program memory and one for the Data EEPROM memory.

TABLE 7-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
08h	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
09h	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
88h	EECON1	—	—	—	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
89h	EECON2	EEPROM control register 2								---- ----	---- ----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by Data EEPROM.

PIC16F8X

NOTES:

8.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real time applications. The PIC16F8X has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- OSC Selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC16F8X has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. This design keeps the device in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode offers a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer time-out or through an interrupt. Several oscillator options are provided to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select the various options.

8.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

Address 2007h is beyond the user program memory space and it belongs to the special test/configuration memory space (2000h - 3FFFh). This space can only be accessed during programming.

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FIGURE 8-1: CONFIGURATION WORD - PIC16CR83 AND PIC16CR84

R-u	R-u	R-u	R-u	R-u	R-u	R/P-u	R-u	R-u	R-u	R-u	R-u	R-u	R-u
CP	CP	CP	CP	CP	CP	DP	CP	CP	CP	PWRTÉ	WDTE	FOSC1	FOSC0
bit13											bit0		

R = Readable bit
P = Programmable bit
- n = Value at POR reset
u = unchanged

bit 13:8 **CP**: Program Memory Code Protection bit
1 = Code protection off
0 = Program memory is code protected

bit 7 **DP**: Data Memory Code Protection bit
1 = Code protection off
0 = Data memory is code protected

bit 6:4 **CP**: Program Memory Code Protection bit
1 = Code protection off
0 = Program memory is code protected

bit 3 **PWRTÉ**: Power-up Timer Enable bit
1 = Power-up timer is disabled
0 = Power-up timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1:0 **FOSC1:FOSC0**: Oscillator Selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

FIGURE 8-2: CONFIGURATION WORD - PIC16F83 AND PIC16F84

R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u	R/P-u
CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	CP	PWRTÉ	WDTE	FOSC1	FOSC0
bit13											bit0			

R = Readable bit
P = Programmable bit
- n = Value at POR reset
u = unchanged

bit 13:4 **CP**: Code Protection bit

1 = Code protection off

0 = All memory is code protected

bit 3 **PWRTÉ**: Power-up Timer Enable bit

1 = Power-up timer is disabled

0 = Power-up timer is enabled

bit 2 **WDTE**: Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 1:0 **FOSC1:FOSC0**: Oscillator Selection bits

11 = RC oscillator

10 = HS oscillator

01 = XT oscillator

00 = LP oscillator

8.2 Oscillator Configurations

8.2.1 OSCILLATOR TYPES

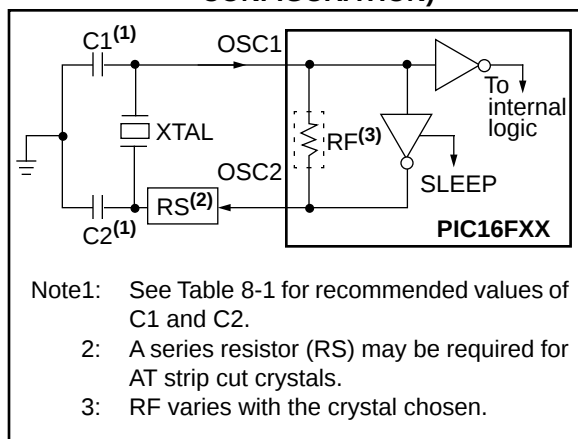
The PIC16F8X can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

8.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 8-3).

FIGURE 8-3: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



The PIC16F8X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 8-4).

FIGURE 8-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

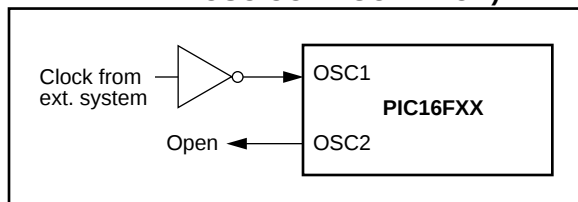


TABLE 8-1: PIC16F83/CR83/F84/CR84 CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Tested:			
Mode	Freq	OSC1/C1	OSC2/C2
XT	455 kHz	47 - 100 pF	47 - 100 pF
	2.0 MHz	15 - 33 pF	15 - 33 pF
	4.0 MHz	15 - 33 pF	15 - 33 pF
HS	8.0 MHz	15 - 33 pF	15 - 33 pF
	10.0 MHz	15 - 33 pF	15 - 33 pF
Note: Recommended values of C1 and C2 are identical to the ranges tested table. Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for the appropriate values of external components.			
Resonators Tested:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
10.0 MHz	Murata Erie CSA10.00MTZ	± 0.5%	
None of the resonators had built-in capacitors.			

TABLE 8-2: PIC16F83/CR83/F84/CR84 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1/C1	OSC2/C2
LP	32 kHz	68 - 100 pF	68 - 100 pF
	200 kHz	15 - 33 pF	15 - 33 pF
XT	100 kHz	100 - 150 pF	100 - 150 pF
	2 MHz	15 - 33 pF	15 - 33 pF
	4 MHz	15 - 33 pF	15 - 33 pF
HS	4 MHz	15 - 33 pF	15 - 33 pF
	10 MHz	15 - 33 pF	15 - 33 pF

Note: Higher capacitance increases the stability of oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

Crystals Tested:

32.768 kHz	Epson C-001R32.768K-A	± 20 PPM
100 kHz	Epson C-2 100.00 KC-P	± 20 PPM
200 kHz	STD XTL 200.000 KHz	± 20 PPM
1.0 MHz	ECS ECS-10-13-2	± 50 PPM
2.0 MHz	ECS ECS-20-S-2	± 50 PPM
4.0 MHz	ECS ECS-40-S-4	± 50 PPM
10.0 MHz	ECS ECS-100-S-4	± 50 PPM

8.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator can be used or a simple oscillator circuit with TTL gates can be built. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits are available; one with series resonance, and one with parallel resonance.

Figure 8-5 shows a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides negative feedback for stability. The 10 kΩ potentiometer biases the 74AS04 in the linear region. This could be used for external oscillator designs.

FIGURE 8-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

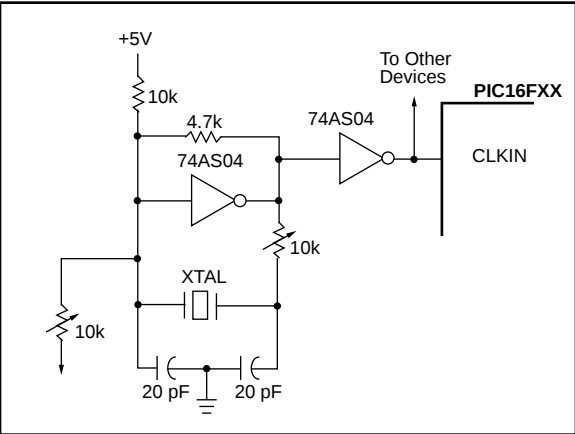
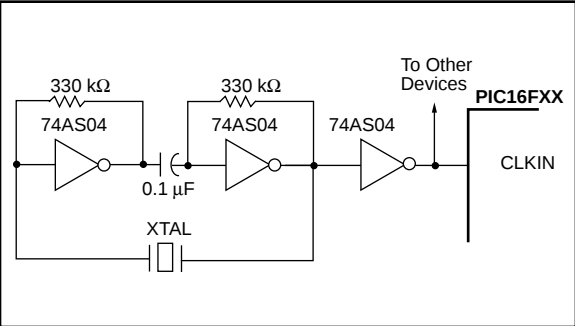


Figure 8-6 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 8-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



8.2.4 RC OSCILLATOR

For timing insensitive applications the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{ext}) values, capacitor (C_{ext}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types also affects the oscillation frequency, especially for low C_{ext} values. The user needs to take into account variation due to tolerance of the external R and C components. Figure 8-7 shows how an R/C combination is connected to the PIC16F8X. For R_{ext} values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high R_{ext} values (e.g., 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping R_{ext} between 5 k Ω and 100 k Ω .

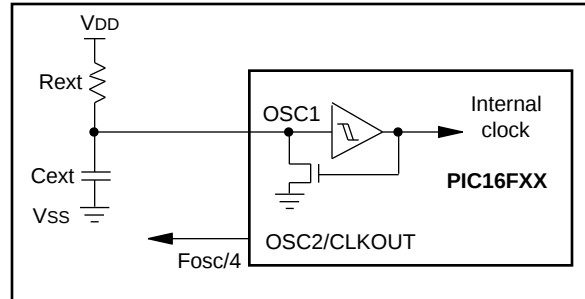
Although the oscillator will operate with no external capacitor ($C_{ext} = 0$ pF), we recommend using values above 20 pF for noise and stability reasons. With little or no external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See the electrical specification section for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance has a greater effect on RC frequency).

See the electrical specification section for variation of oscillator frequency due to V_{DD} for given R_{ext}/C_{ext} values as well as frequency variation due to operating temperature.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic (see Figure 3-2 for waveform).

FIGURE 8-7: RC OSCILLATOR MODE



Note: When the device oscillator is in RC mode, do not drive the OSC1 pin with an external clock or you may damage the device.

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8.3 Reset

The PIC16F8X differentiates between various kinds of reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ reset during normal operation
- $\overline{\text{MCLR}}$ reset during SLEEP
- WDT Reset (during normal operation)
- WDT Wake-up (during SLEEP)

Figure 8-8 shows a simplified block diagram of the on-chip reset circuit. The $\overline{\text{MCLR}}$ reset path has a noise filter to ignore small pulses. The electrical specifications state the pulse width requirements for the $\overline{\text{MCLR}}$ pin.

Some registers are not affected in any reset condition; their status is unknown on a POR reset and unchanged in any other reset. Most other registers are reset to a

“reset state” on POR, $\overline{\text{MCLR}}$ or WDT reset during normal operation and on $\overline{\text{MCLR}}$ reset during SLEEP. They are not affected by a WDT reset during SLEEP, since this reset is viewed as the resumption of normal operation.

Table 8-3 gives a description of reset conditions for the program counter (PC) and the STATUS register. Table 8-4 gives a full description of reset states for all registers.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different reset situations (Section 8.7). These bits are used in software to determine the nature of the reset.

FIGURE 8-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

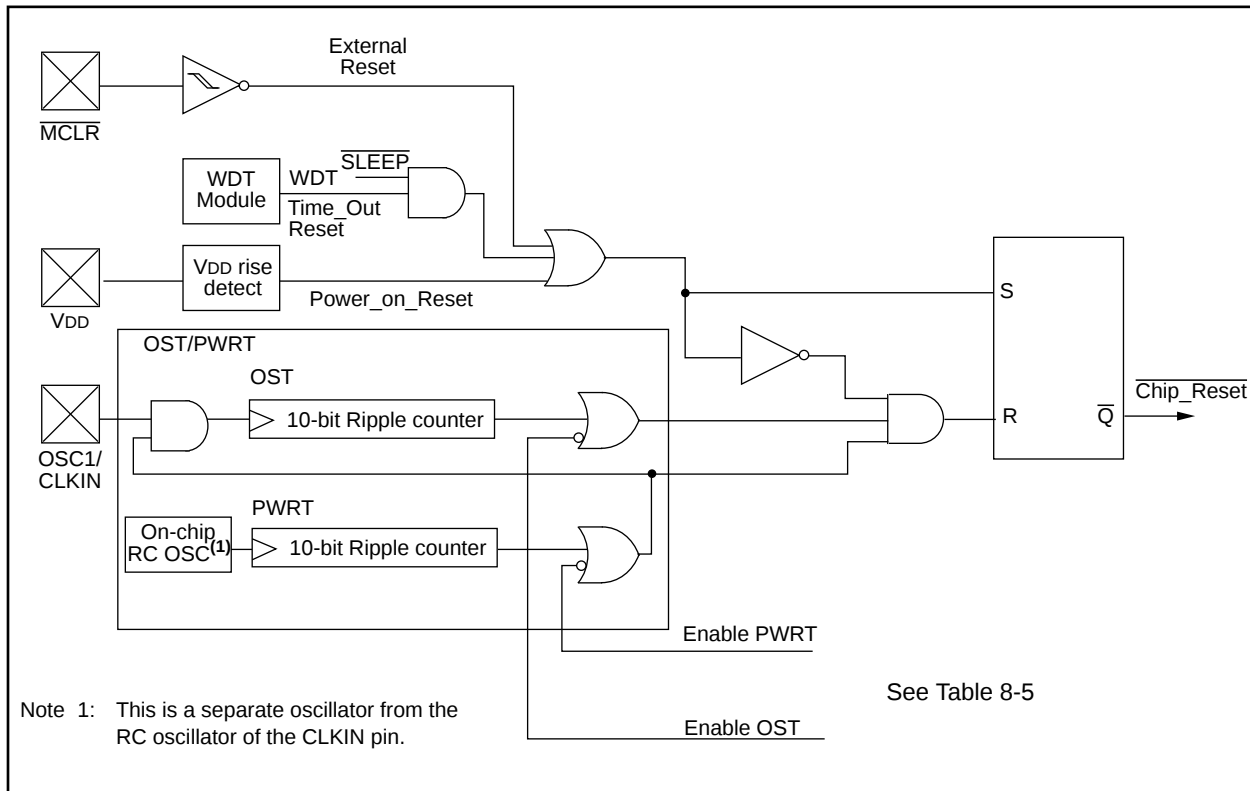


TABLE 8-3: RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	0001 1xxx
MCLR Reset during normal operation	000h	000u uuuu
MCLR Reset during SLEEP	000h	0001 0uuu
WDT Reset (during normal operation)	000h	0000 1uuu
WDT Wake-up	PC + 1	uuu0 0uuu
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu

Legend: u = unchanged, x = unknown.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 8-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	MCLR Reset during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h	---- ----	---- ----	---- ----
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1 ⁽²⁾
STATUS	03h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	---x xxxx	---u uuuu	---u uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATA	08h	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	0Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
INDF	80h	---- ----	---- ----	---- ----
OPTION	81h	1111 1111	1111 1111	uuuu uuuu
PCL	82h	0000h	0000h	PC + 1
STATUS	83h	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TRISA	85h	---1 1111	---1 1111	---u uuuu
TRISB	86h	1111 1111	1111 1111	uuuu uuuu
EECON1	88h	---0 x000	---0 q000	---0 uuuu
EECON2	89h	---- ----	---- ----	---- ----
PCLATH	8Ah	---0 0000	---0 0000	---u uuuu
INTCON	8Bh	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0',
q = value depends on condition.

Note 1: One or more bits in INTCON will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: Table 8-3 lists the reset value for each specific condition.

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8.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the $\overline{MCLR}$ pin directly (or through a resistor) to V_{DD} . This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for V_{DD} must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

The POR circuit does not produce an internal reset when V_{DD} declines.

8.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out ($TPWRT$) from POR (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13). The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level (Possible exception shown in Figure 8-13).

A configuration bit, $PWRT\overline{E}$, can enable/disable the PWRT. See either Figure 8-1 or Figure 8-2 for the operation of the $PWRT\overline{E}$ bit for a particular device.

The power-up time delay $TPWRT$ will vary from chip to chip due to V_{DD} , temperature, and process variation. See DC parameters for details.

8.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out ($TOST$) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When V_{DD} rises very slowly, it is possible that the $TPWRT$ time-out and $TOST$ time-out will expire before V_{DD} has reached its final value. In this case (Figure 8-13), an external power-on reset circuit may be necessary (Figure 8-9).

FIGURE 8-9: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V_{DD} POWER-UP)

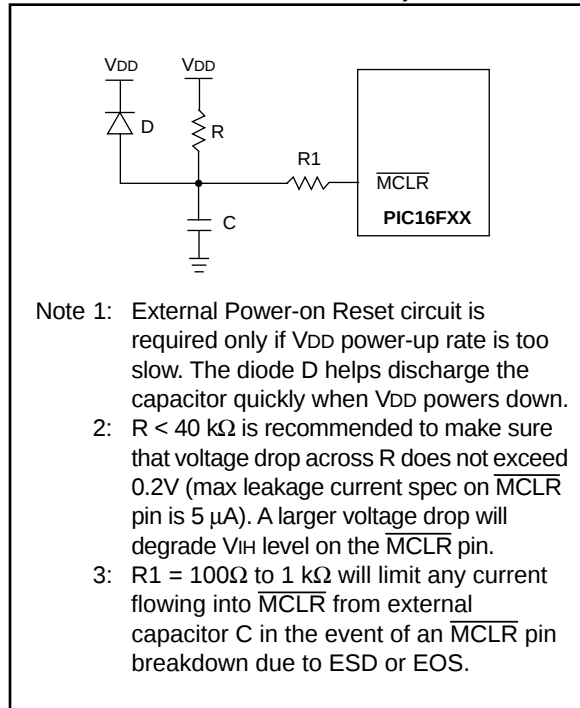


FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

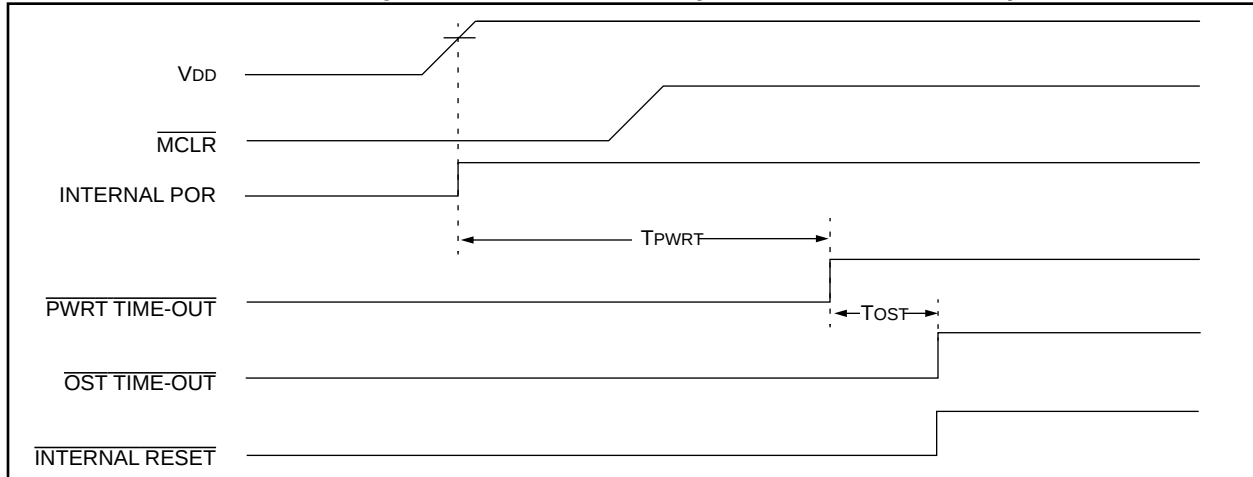
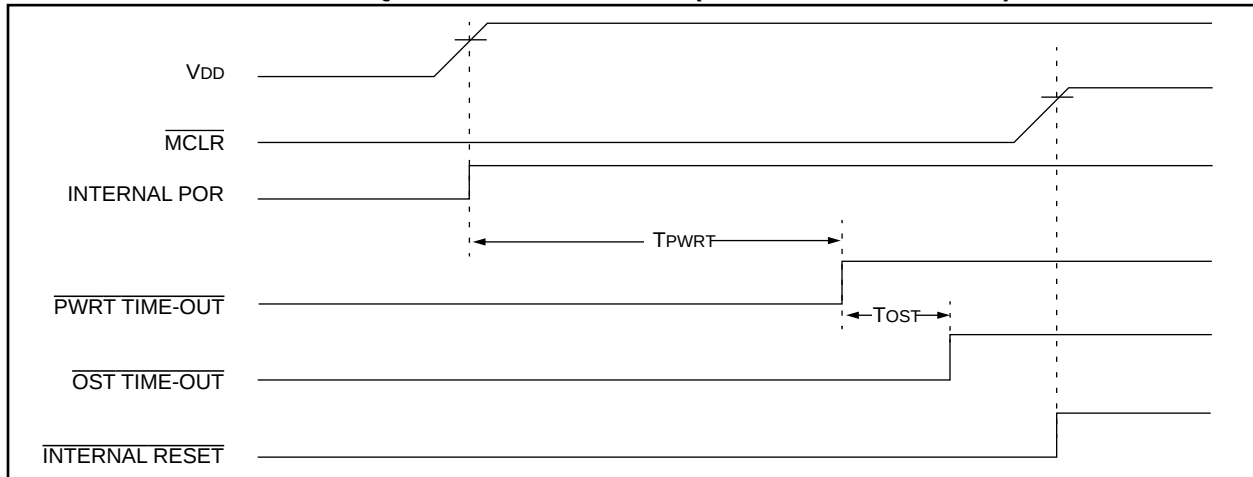


FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2



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FIGURE 8-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME

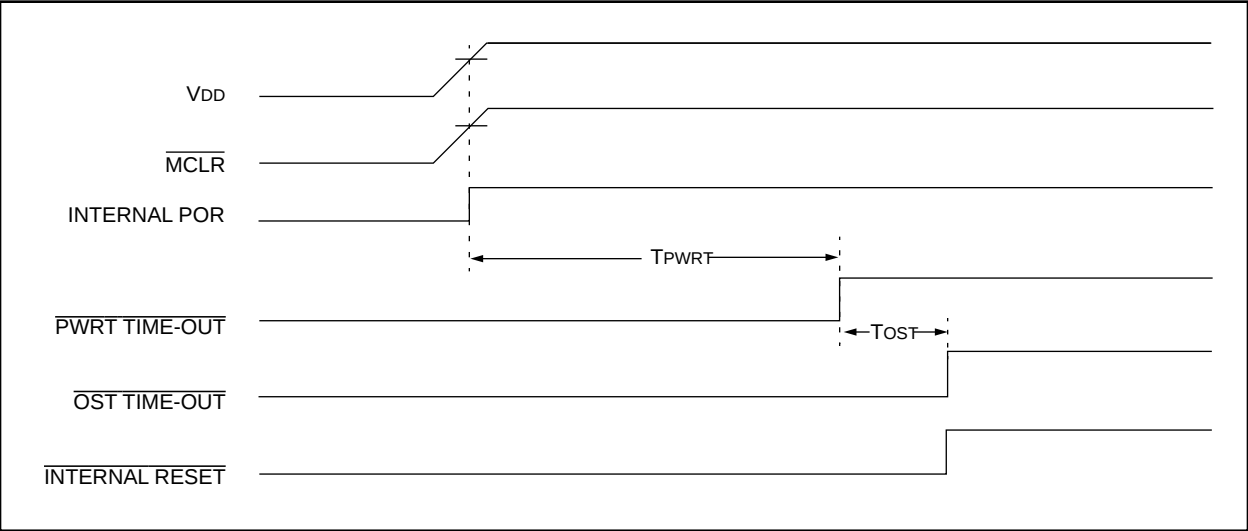
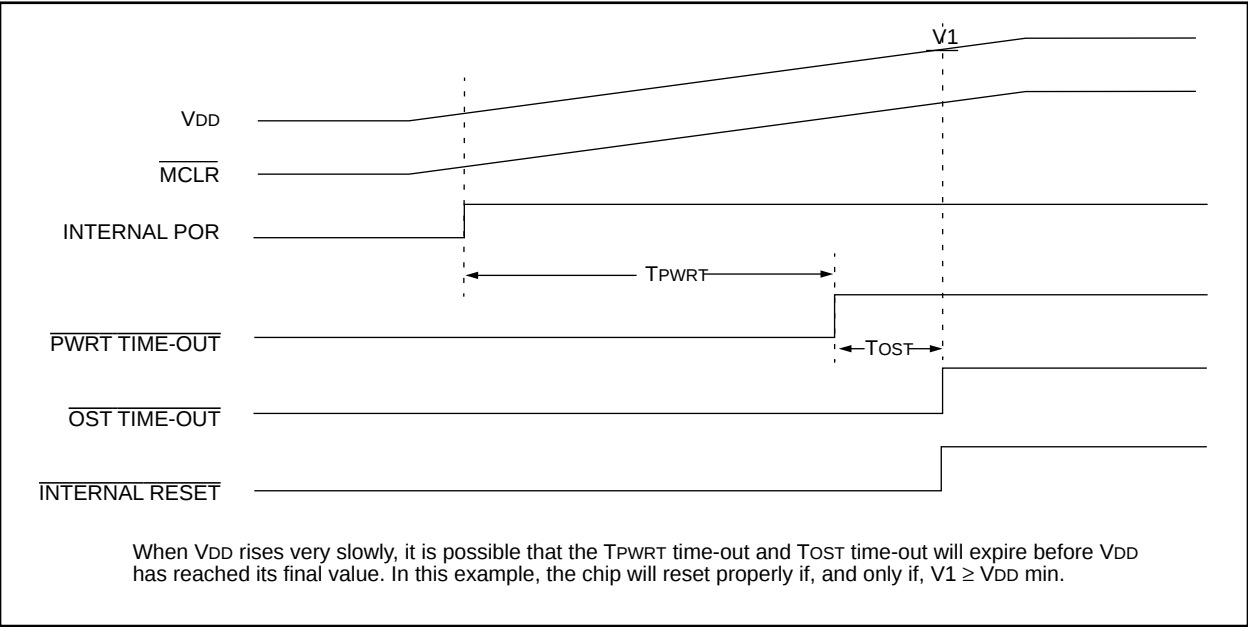


FIGURE 8-13: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



8.7 Time-out Sequence and Power-down Status Bits (TO/PD)

On power-up (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13) the time-out sequence is as follows: First PWRT time-out is invoked after a POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and PWRT configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

TABLE 8-5: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	PWRT Disabled	
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	1024Tosc
RC	72 ms	—	—

Since the time-outs occur from the POR reset pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high, execution will begin immediately (Figure 8-10). This is useful for testing purposes or to synchronize more than one PIC16F8X device when operating in parallel.

Table 8-6 shows the significance of the TO and PD bits. Table 8-3 lists the reset conditions for some special registers, while Table 8-4 lists the reset conditions for all the registers.

TABLE 8-6: STATUS BITS AND THEIR SIGNIFICANCE

TO	PD	Condition
1	1	Power-on Reset
0	x	Illegal, TO is set on POR
x	0	Illegal, PD is set on POR
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	MCLR Reset during normal operation
1	0	MCLR Reset during SLEEP or interrupt wake-up from SLEEP

8.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset a PIC16F8X device when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-14 and Figure 8-15.

FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 1

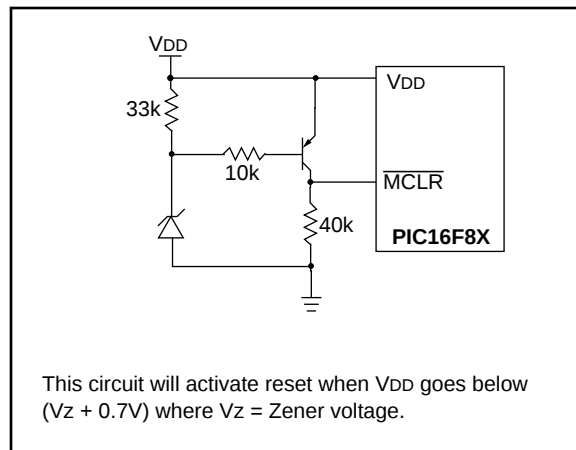
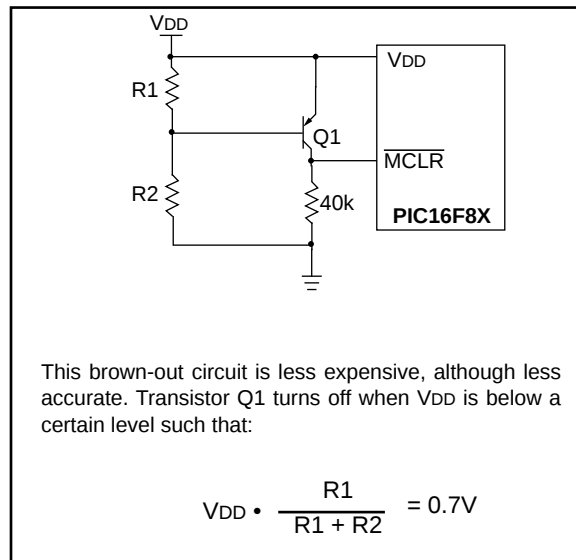


FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 2



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8.9 Interrupts

The PIC16F8X has 4 sources of interrupt:

- External interrupt RB0/INT pin
- TMR0 overflow interrupt
- PORTB change interrupts (pins RB7:RB4)
- Data EEPROM write complete interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also contains the individual and global interrupt enable bits.

The global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register. Bit GIE is cleared on reset.

The “return from interrupt” instruction, RETFIE, exits interrupt routine as well as sets the GIE bit, which re-enable interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

When an interrupt is responded to; the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. For external interrupt events, such as the RB0/INT pin or PORTB change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 8-17). The latency is the same for both one and two cycle instructions. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

Note 1: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

FIGURE 8-16: INTERRUPT LOGIC

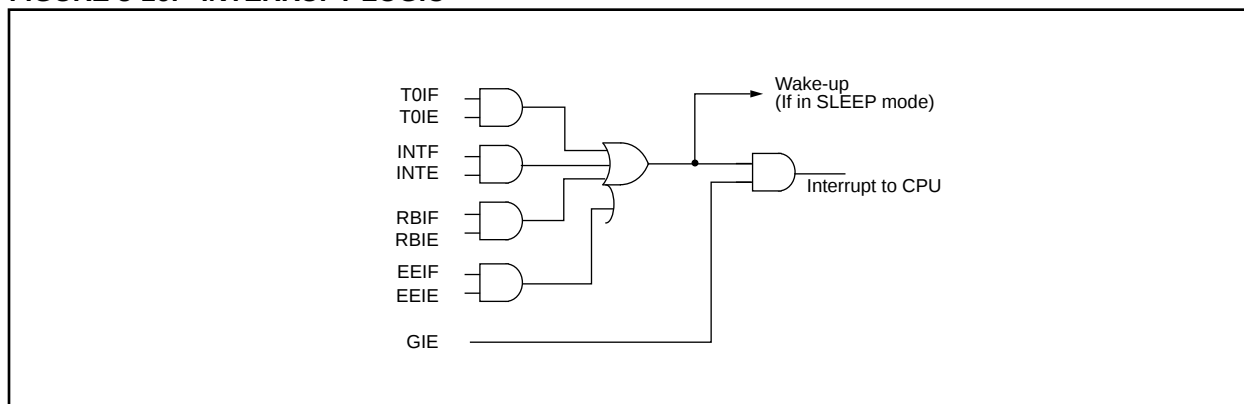
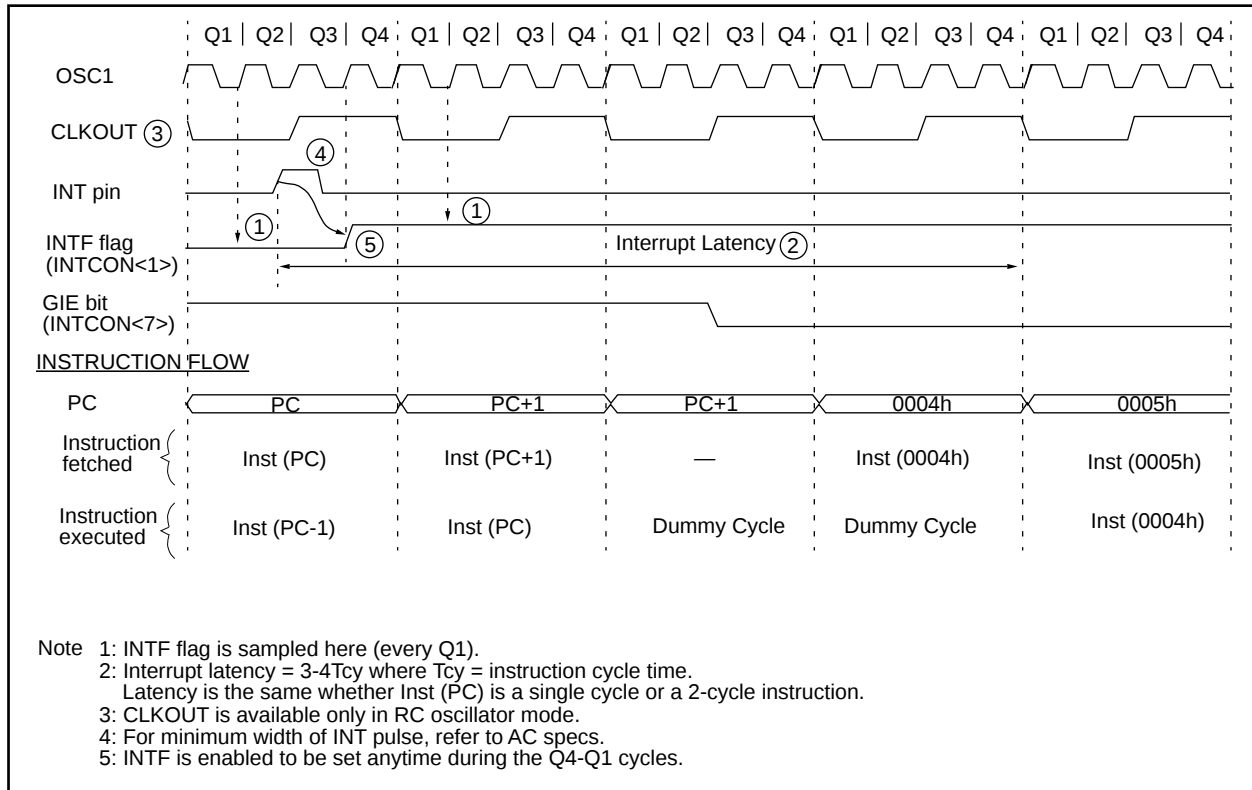


FIGURE 8-17: INT PIN INTERRUPT TIMING



8.9.1 INT INTERRUPT

External interrupt on RB0/INT pin is edge triggered: either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing control bit INTE (INTCON<4>). Flag bit INTF must be cleared in software via the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake the processor from SLEEP (Section 8.12) only if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether the processor branches to the interrupt vector following wake-up.

8.9.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in TMR0 will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>) (Section 6.0).

8.9.3 PORT RB INTERRUPT

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<3>) (Section 5.2).

Note 1: For a change on the I/O pin to be recognized, the pulse width must be at least Tcy wide.

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8.10 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users wish to save key register values during an interrupt (e.g., W register and STATUS register). This is implemented in software.

Example 8-1 stores and restores the STATUS and W register's values. The User defined registers, W_TEMP and STATUS_TEMP are the temporary storage locations for the W and STATUS registers values.

Example 8-1 does the following:

- a) Stores the W register.
- b) Stores the STATUS register in STATUS_TEMP.
- c) Executes the Interrupt Service Routine code.
- d) Restores the STATUS (and bank select bit) register.
- e) Restores the W register.

EXAMPLE 8-1: SAVING STATUS AND W REGISTERS IN RAM

```
PUSH    MOVWF    W_TEMP        ; Copy W to TEMP register,
        SWAPF    STATUS, W      ; Swap status to be saved into W
        MOVWF    STATUS_TEMP    ; Save status to STATUS_TEMP register
ISR      :
        :                      ;
        :                      ; Interrupt Service Routine
        :                      ; should configure Bank as required
        :                      ;
POP      SWAPF    STATUS_TEMP, W ; Swap nibbles in STATUS_TEMP register
        :                      ; and place result into W
        MOVWF    STATUS        ; Move W into STATUS register
        :                      ; (sets bank to original state)
        SWAPF    W_TEMP, F      ; Swap nibbles in W_TEMP and place result in W_TEMP
        SWAPF    W_TEMP, W      ; Swap nibbles in W_TEMP and place result into W
```

8.11 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a SLEEP instruction. During normal operation a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT Wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit WDTE as a '0' (Section 8.1).

8.11.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, V_{DD} and process variations from part to

part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a WDT time-out.

8.11.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 8-18: WATCHDOG TIMER BLOCK DIAGRAM

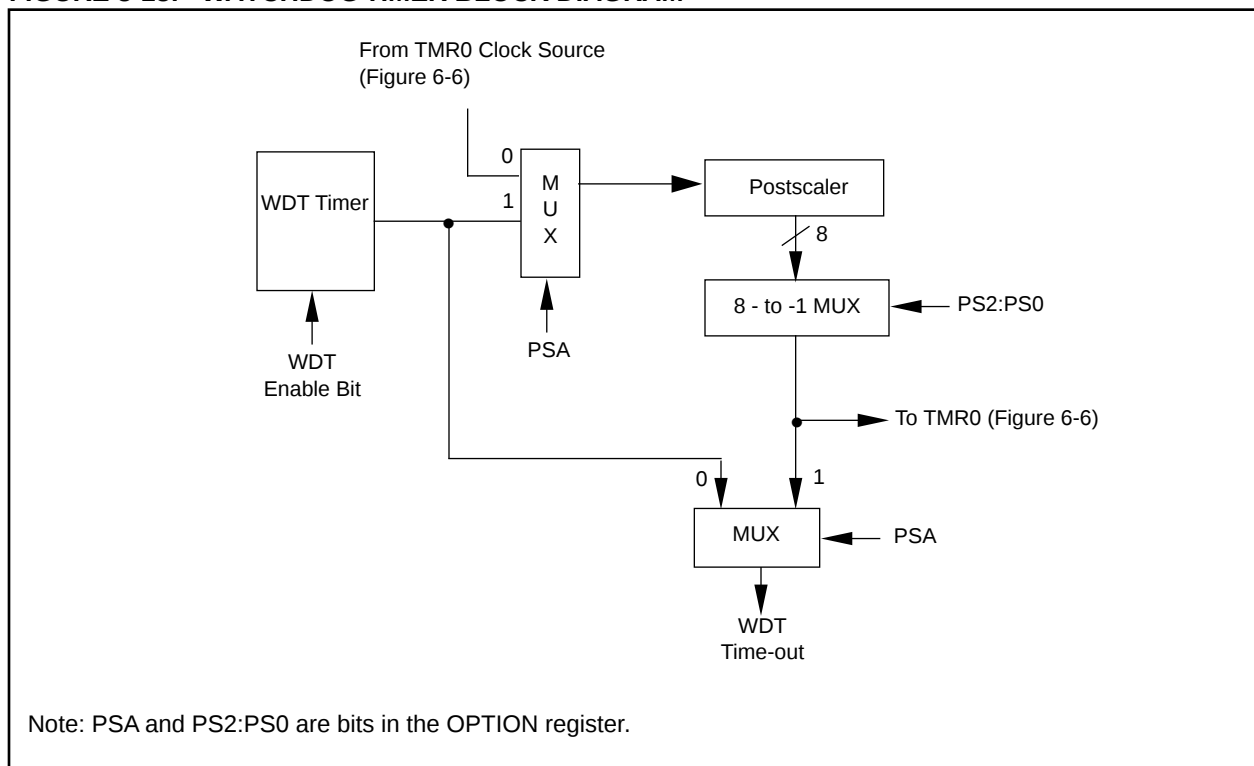


TABLE 8-7: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
2007h	Config. bits	(2)	(2)	(2)	(2)	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0	(2)	
81h	OPTION	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.

Note 1: See Figure 8-1 and Figure 8-2 for operation of the PWRTE bit.

2: See Figure 8-1, Figure 8-2 and Section 8.13 for operation of the Code and Data protection bits.

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8.12 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

8.12.1 SLEEP

The Power-down mode is entered by executing the SLEEP instruction.

If enabled, the Watchdog Timer is cleared (but keeps running), the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ bit (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For the lowest current consumption in SLEEP mode, place all I/O pins at either at VDD or VSS, with no external circuitry drawing current from the I/O pins, and disable external clocks. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (V_{IHMC}).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

8.12.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

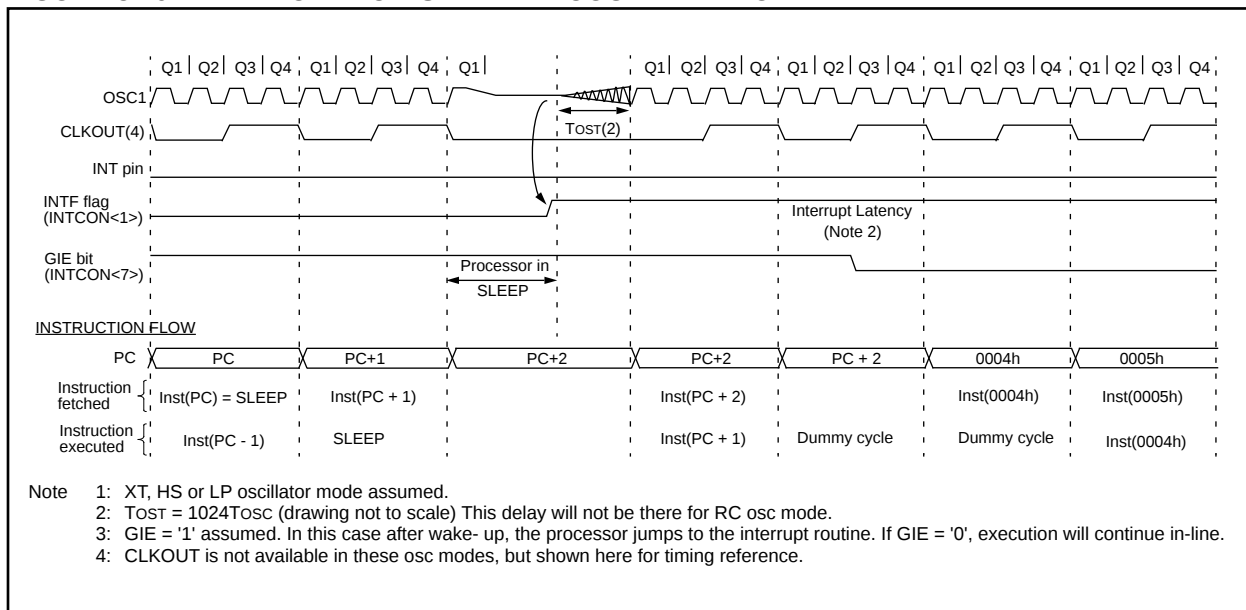
1. External reset input on $\overline{MCLR}$ pin.
2. WDT Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or data EEPROM write complete.

Peripherals cannot generate interrupts during SLEEP, since no on-chip Q clocks are present.

The first event ($\overline{MCLR}$ reset) will cause a device reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of a device reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

While the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.

FIGURE 8-19: WAKE-UP FROM SLEEP THROUGH INTERRUPT



8.12.3 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

8.13 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting widowed devices.

8.14 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations to store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable only during program/verify. Only the 4 least significant bits of ID location are usable.

For ROM devices, these values are submitted along with the ROM code.

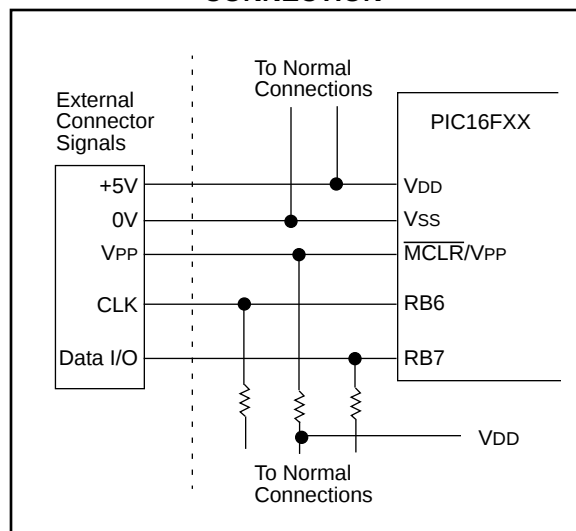
8.15 In-Circuit Serial Programming

PIC16F8X microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. Customers can manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product, allowing the most recent firmware or custom firmware to be programmed.

The device is placed into a program/verify mode by holding the RB6 and RB7 pins low, while raising the MCLR pin from V_{IL} to V_{IH} (see programming specification). RB6 becomes the programming clock and RB7 becomes the programming data. Both RB6 and RB7 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) points to location 00h. A 6-bit command is then supplied to the device, 14-bits of program data is then supplied to or from the device, using load or read-type instructions. For complete details of serial programming, please refer to the PIC16CXX Programming Specifications (Literature #DS30189).

FIGURE 8-20: TYPICAL IN-SYSTEM SERIAL PROGRAMMING CONNECTION



For ROM devices, both the program memory and Data EEPROM memory may be read, but only the Data EEPROM memory may be programmed.

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NOTES:

9.0 INSTRUCTION SET SUMMARY

Each PIC16FXX instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16FXX instruction set summary in Table 9-2 lists byte-oriented, bit-oriented, and literal and control operations. Table 9-1 shows the opcode field descriptions.

Byte-oriented instructions: 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in the file register specified by the instruction.

Bit-oriented instructions: 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

Literal and control operations: 'k' represents an eight or eleven bit constant or literal value.

TABLE 9-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
TO	Time-out bit
PD	Power-down bit
dest	Destination (Either the W register or the specified register file location)
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- Byte-oriented
- Bit-oriented
- Literal and control

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. The execution takes two instruction cycles with the second cycle executed as a NOP. Each cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. The instruction execution time is 2 μ s for program branches.

Table 9-2 lists the instructions recognized by Microchip's assembler (MPASM).

Figure 9-1 shows the three general formats of instructions.

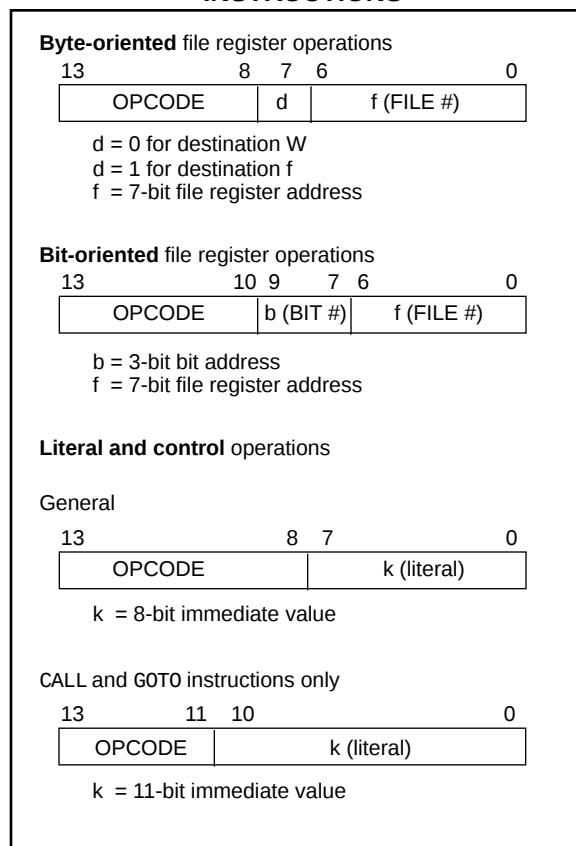
Note: To maintain upward compatibility with future PIC16FXX products, do not use the OPTION and TRIS instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 9-1: GENERAL FORMAT FOR INSTRUCTIONS



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TABLE 9-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb		LSb			
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0000	0011	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECf	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff	None	1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff	None	1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff	None	
NOP	-	No Operation	1	00	0000	0xx0	0000	None	
RLF	f, d	Rotate left f through carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate right f through carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff	None	1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff	None	1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff	None	1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff	None	3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff	None	3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWD $\overline{T}$	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}, \overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk	None	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk	None	
RETFIE	-	Return from interrupt	2	00	0000	0000	1001	None	
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk	None	
RETURN	-	Return from subroutine	2	00	0000	0000	1000	None	
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}, \overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (i.e., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the TMR0.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

9.1 Instruction Descriptions

ADDLW Add Literal and W

Syntax:	[<i>label</i>] ADDLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	$(W) + k \rightarrow (W)$				
Status Affected:	C, DC, Z				
Encoding:	<table border="1"><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>	11	111x	kkkk	kkkk
11	111x	kkkk	kkkk		
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed back in the W register.				
Words:	1				
Cycles:	1				
Example	ADDLW 0x15 Before Instruction W = 0x10 After Instruction W = 0x25				

ANDLW AND Literal with W

Syntax:	[<i>label</i>] ANDLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	(W) .AND. (k) $\rightarrow$ (W)				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>	11	1001	kkkk	kkkk
11	1001	kkkk	kkkk		
Description:	The contents of W register is AND'ed with the eight bit literal 'k'. The result is placed back in the W register.				
Words:	1				
Cycles:	1				
Example	ANDLW 0x5F Before Instruction W = 0xA3 After Instruction W = 0x03				

ADDWF Add W and f

Syntax:	[<i>label</i>] ADDWF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(W) + (f) \rightarrow (dest)$				
Status Affected:	C, DC, Z				
Encoding:	<table><tr><td>00</td><td>0111</td><td>dfff</td><td>ffff</td></tr></table>	00	0111	dfff	ffff
00	0111	dfff	ffff		
Description:	Add the contents of the W register to register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	ADDWF FSR, 0 Before Instruction W = 0x17 FSR = 0xC2 After Instruction W = 0xD9 FSR = 0xC2				

ANDWF AND W with f

Syntax:	[<i>label</i>] ANDWF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(W) .AND. (f) $\rightarrow$ (dest)			
Status Affected:	Z			
Encoding:	00	0101	dfff	ffff
Description:	AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example	ANDWF FSR, 1			
	Before Instruction			
	W	=	0x17	
	FSR	=	0xC2	
	After Instruction			
	W	=	0x17	
	FSR	=	0x02	

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BCF		Bit Clear f							
Syntax:	[<i>label</i>] BCF f,b								
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$								
Operation:	$0 \rightarrow (f)$								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>01</td><td>00bb</td><td>bfff</td><td>ffff</td></tr></table>				01	00bb	bfff	ffff	
01	00bb	bfff	ffff						
Description:	Bit 'b' in register 'f' is cleared.								
Words:	1								
Cycles:	1								
Example	BCF FLAG_REG, 7								
	Before Instruction								
	FLAG_REG = 0xC7								
	After Instruction								
	FLAG_REG = 0x47								

BSF		Bit Set f			
Syntax:	[<i>label</i>] BSF f,b				
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$				
Operation:	$1 \rightarrow (f)$				
Status Affected:	None				
Encoding:	01	01bb	bfff	ffff	
Description:	Bit 'b' in register 'f' is set.				
Words:	1				
Cycles:	1				
Example	BSF FLAG_REG, 7				
	Before Instruction				
	FLAG_REG= 0x0A				
	After Instruction				
	FLAG_REG= 0x8A				

BTFSC		Bit Test f, Skip if Clear						
Syntax:	[<i>label</i>] BTFSC f,b							
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$							
Operation:	skip if (f) = 0							
Status Affected:	None							
Encoding:	<table border="1"><tr><td>01</td><td>10bb</td><td>bfff</td><td>ffff</td></tr></table>				01	10bb	bfff	ffff
01	10bb	bfff	ffff					
Description:	If bit 'b' in register 'f' is 0 then the next instruction is skipped. If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2 cycle instruction.							
Words:	1							
Cycles:	1(2)							
Example	HERE FALSE TRUE	BTFSC GOTO • • •	FLAG, 1 PROCESS_CODE					
	Before Instruction PC = address HERE After Instruction if FLAG<1>=0, PC=address TRUE if FLAG<1>=1, PC=address FALSE							

BTFSS		Bit Test f, skip if Set							
Syntax:	[<i>label</i>] BTFSS f,b								
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7								
Operation:	skip if (f) = 1								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>01</td><td>11bb</td><td>bfff</td><td>ffff</td></tr></table>				01	11bb	bfff	ffff	
01	11bb	bfff	ffff						
Description:	If bit 'b' in register 'f' is 1 then the next instruction is skipped. If bit 'b' is 1, then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2 cycle instruction.								
Words:	1								
Cycles:	1(2)								
Example	HERE FALSE TRUE	BTFSC GOTO • • •	FLAG, 1 PROCESS_CODE						
Before Instruction									
PC = address HERE									
After Instruction									
if FLAG<1>=0,									
PC=address FALSE									
if FLAG<1>=1,									
PC=address TRUE									

CALL		Subroutine Call																		
Syntax:	[<i>label</i>] CALL k																			
Operands:	0 ≤ k ≤ 2047																			
Operation:	(PC)+ 1 → TOS, k → (PC<10:0>), (PCLATH<4:3>) → (PC<12:11>)																			
Status Affected:	None																			
Encoding:	<table><tr><td>10</td><td>0kkk</td><td>kkkk</td><td>kkkk</td></tr></table>					10	0kkk	kkkk	kkkk											
10	0kkk	kkkk	kkkk																	
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two cycle instruction.																			
Words:	1																			
Cycles:	2																			
Example	<table><tr><td>HERE</td><td>CALL</td><td>THERE</td></tr></table> <table><tr><td>Before Instruction</td><td>PC =</td><td>Address</td><td>HERE</td></tr><tr><td>After Instruction</td><td>PC =</td><td>Address</td><td>THERE</td></tr><tr><td></td><td>TOS =</td><td>Address</td><td>HERE</td></tr></table>					HERE	CALL	THERE	Before Instruction	PC =	Address	HERE	After Instruction	PC =	Address	THERE		TOS =	Address	HERE
HERE	CALL	THERE																		
Before Instruction	PC =	Address	HERE																	
After Instruction	PC =	Address	THERE																	
	TOS =	Address	HERE																	

CLRF		Clear f							
Syntax:	[<i>label</i>] CLRF f								
Operands:	$0 \leq f \leq 127$								
Operation:	00h → (f) 1 → Z								
Status Affected:	Z								
Encoding:	<table><tr><td>00</td><td>0001</td><td>1fff</td><td>ffff</td></tr></table>					00	0001	1fff	ffff
00	0001	1fff	ffff						
Description:	The contents of register 'f' are cleared and the Z bit is set.								
Words:	1								
Cycles:	1								
Example	CLRF FLAG_REG								
	Before Instruction								
	FLAG_REG = 0x5A								
	After Instruction								
	FLAG_REG = 0x00								
	Z = 1								

CLR W Register					
Syntax:	[<i>label</i>] CLRW				
Operands:	None				
Operation:	00h → (W) 1 → Z				
Status Affected:	Z				
Encoding:	<table><tr><td>00</td><td>0001</td><td>0000</td><td>0011</td></tr></table>	00	0001	0000	0011
00	0001	0000	0011		
Description:	W register is cleared. Zero bit (Z) is set.				
Words:	1				
Cycles:	1				
Example	<pre>CLRW</pre> Before Instruction W = 0x5A After Instruction W = 0x00 Z = 1				

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CLRWDT Clear Watchdog Timer

Syntax:	[<i>label</i>] CLRWDT			
Operands:	None			
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$			
Status Affected:	$\overline{TO}$, $\overline{PD}$			
Encoding:	00	0000	0110	0100
Description:	The CLRWDT instruction resets the watchdog timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.			
Words:	1			
Cycles:	1			
Example	CLRWDT			

Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
 $\overline{TO}$ = 1
 $\overline{PD}$ = 1

COMF Complement f

Syntax:	[<i>label</i>] COMF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	$(\bar{f}) \rightarrow (\text{dest})$			
Status Affected:	Z			
Encoding:	00	1001	dfff	ffff
Description:	The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.			
Words:	1			
Cycles:	1			
Example	COMF REG1, 0			

Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

DECF Decrement f

Syntax:	[<i>label</i>] DECF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(f) - 1 \rightarrow (\text{dest})$				
Status Affected:	Z				
Encoding:	<table><tr><td>00</td><td>0011</td><td>dfff</td><td>ffff</td></tr></table>	00	0011	dfff	ffff
00	0011	dfff	ffff		
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	DECF CNT, 1				

Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

DECFSZ Decrement f, Skip if 0

Syntax:	[<i>label</i>] DECFSZ f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(f) - 1 \rightarrow (\text{dest})$; skip if result = 0				
Status Affected:	None				
Encoding:	<table border="1"><tr><td>00</td><td>1011</td><td>dfff</td><td>ffff</td></tr></table>	00	1011	dfff	ffff
00	1011	dfff	ffff		
Description:	The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.				
Words:	1				
Cycles:	1(2)				
Example	<pre>HERE DECFSZ CNT, 1 GOTO LOOP</pre>				

Before Instruction
PC = addressHERE
After Instruction
CNT = CNT - 1
if CNT = 0,
PC = address CONTINUE
if CNT ≠ 0,
PC = address HERE+1

GOTO		Go to address							
Syntax:	[<i>label</i>] GOTO k								
Operands:	$0 \leq k \leq 2047$								
Operation:	$k \rightarrow (PC<10:0>)$ $(PCLATH<4:3>) \rightarrow (PC<12:11>)$								
Status Affected:	None								
Encoding:	<table><tr><td>10</td><td>1kkk</td><td>kkkk</td><td>kkkk</td></tr></table>					10	1kkk	kkkk	kkkk
10	1kkk	kkkk	kkkk						
Description:	GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.								
Words:	1								
Cycles:	2								
Example	GOTO THERE								
	After Instruction								
	PC = Address THERE								

INCFSZ		Increment f, Skip if 0						
Syntax:	[<i>label</i>] INCFSZ f,d							
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$							
Operation:	$(f) + 1 \rightarrow (\text{dest}), \text{ skip if result} = 0$							
Status Affected:	None							
Encoding:	00		1111		dfff		ffff	
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.							
Words:	1							
Cycles:	1(2)							
Example	HERE 1		INCFSZ		CNT,			
			GOTO		LOOP			
	CONTINUE		•					
			•					
			•					

Before Instruction
 PC = addressHERE
 After Instruction
 CNT = CNT + 1
 if CNT = 0,
 PC = addressCONTINUE
 if CNT ≠ 0,
 PC = addressHERE +1

INCF		Increment f								
Syntax:	[<i>label</i>] INCF f,d									
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]									
Operation:	(f) + 1 → (dest)									
Status Affected:	Z									
Encoding:	<table><tr><td>00</td><td>1010</td><td>dfff</td><td>ffff</td></tr></table>						00	1010	dfff	ffff
00	1010	dfff	ffff							
Description:	The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.									
Words:	1									
Cycles:	1									
Example	INCF CNT, 1									
	Before Instruction									
	CNT	=	0xFF							
	Z	=	0							
	After Instruction									
	CNT	=	0x00							
	Z	=	1							

IORLW		Inclusive OR Literal with W						
Syntax:	[<i>label</i>] IORLW k							
Operands:	$0 \leq k \leq 255$							
Operation:	$(W) .OR. (k) \rightarrow (W)$							
Status Affected:	Z							
Encoding:	<table border="1"><tr><td>11</td><td>1000</td><td>kkkk</td><td>kkkk</td></tr></table>				11	1000	kkkk	kkkk
11	1000	kkkk	kkkk					
Description:	The contents of the W register are OR'ed to the eight bit literal 'k'. The result is placed in the W register.							
Words:	1							
Cycles:	1							
Example	IORLW 0x35							
	Before Instruction							
	W = 0x9A							
	After Instruction							
	W = 0xBF							

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IORWF Inclusive OR W with f

Syntax:	[<i>label</i>] IORWF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	(W) .OR. (f) $\rightarrow$ (W)				
Status Affected:	$\bar{Z}$				
Encoding:	<table><tr><td>00</td><td>0100</td><td>dfff</td><td>ffff</td></tr></table>	00	0100	dfff	ffff
00	0100	dfff	ffff		
Description:	Inclusive OR the W register to register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.				
Words:	1				
Cycles:	1				
Example	IORWF RESULT, 0 Before Instruction RESULT = 0x13 W = 0x91 After Instruction RESULT = 0x13 W = 0x93				

MOVLW Move literal to W

Syntax:	[<i>label</i>] MOVLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	$k \rightarrow (W)$				
Status Affected:	None				
Encoding:	<table><tr><td>11</td><td>00XX</td><td>kkkk</td><td>kkkk</td></tr></table>	11	00XX	kkkk	kkkk
11	00XX	kkkk	kkkk		
Description:	The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.				
Words:	1				
Cycles:	1				
Example	<pre>MOVLW 0x5A</pre> After Instruction W = 0x5A				

MOVF Move f

Syntax:	[<i>label</i>] MOVF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(f) $\rightarrow$ (dest)			
Status Affected:	Z			
Encoding:	00	1000	dfff	ffff
Description:	The contents of register f is moved to destination d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.			
Words:	1			
Cycles:	1			
Example	MOVF FSR, 0			
	After Instruction			
	W =value in FSR register			

MOVWF Move W to f

Syntax:	[<i>label</i>] MOVWF f												
Operands:	$0 \leq f \leq 127$												
Operation:	(W) $\rightarrow$ (f)												
Status Affected:	None												
Encoding:	<table><tr><td>00</td><td>0000</td><td>1fff</td><td>ffff</td></tr></table>	00	0000	1fff	ffff								
00	0000	1fff	ffff										
Description:	Move data from W register to register 'f'.												
Words:	1												
Cycles:	1												
Example	<pre>MOVWF OPTION</pre> Before Instruction <table><tr><td>OPTION</td><td>=</td><td>0xFF</td></tr><tr><td>W</td><td>=</td><td>0x4F</td></tr></table> After Instruction <table><tr><td>OPTION</td><td>=</td><td>0x4F</td></tr><tr><td>W</td><td>=</td><td>0x4F</td></tr></table>	OPTION	=	0xFF	W	=	0x4F	OPTION	=	0x4F	W	=	0x4F
OPTION	=	0xFF											
W	=	0x4F											
OPTION	=	0x4F											
W	=	0x4F											

NOP No Operation

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

00	0000	0xx0	0000
----	------	------	------

Description: No operation.

Words: 1

Cycles: 1

Example NOP

RETFIE Return from Interrupt

Syntax: [*label*] RETFIE

Operands: None

Operation: TOS → (PC),
1 → GIE

Status Affected: None

Encoding:

00	0000	0000	1001
----	------	------	------

Description: The Stack is popped and Top of Stack (TOS) is loaded into the PC. Interrupts are enabled by setting the Global Interrupt Enable bit. This is a two cycle instruction.

Words: 1

Cycles: 2

Example RETFIE

After Interrupt

PC = TOS

GIE = 1

OPTION Load Option Register

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

00	0000	0110	0010
----	------	------	------

Description: The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.

Words: 1

Cycles: 1

Example

Note: To maintain upward compatibility with future PIC16FXX products, do not use this instruction.

RETLW Return Literal to W

Syntax: [*label*] RETLW k

Operands: $0 \leq k \leq 255$

Operation: k → (W),
TOS → (PC)

Status Affected: None

Encoding:

11	01xx	kkkk	kkkk
----	------	------	------

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

Words: 1

Cycles: 2

Example

```
CALL TABLE ;W contains table
              ;offset value
      .      ;W now has table value
      .
      .
TABLE ADDWF PC ;W = offset
      RETLW k1 ;Begin table
      RETLW k2 ;
      .
      .
      .
      RETLW kn ;End of table
```

Before Instruction

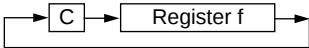
W = 0x07

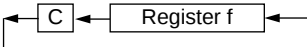
After Instruction

W = value of k7

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RETURN	Return from Subroutine				
Syntax:	[<i>label</i>] RETURN				
Operands:	None				
Operation:	TOS → (PC)				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0000</td><td>1000</td></tr></table>	00	0000	0000	1000
00	0000	0000	1000		
Description:	Return from subroutine. The stack is popped and the Top of Stack (TOS) is loaded into the program counter. This is a two cycle instruction.				
Words:	1				
Cycles:	2				
Example	RETURN After Interrupt PC = TOS				

RRF		Rotate Right f through Carry							
Syntax:	[<i>label</i>] RRF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	See description below								
Status Affected:	C								
Encoding:	<table><tr><td>00</td><td>1100</td><td>dfff</td><td>ffff</td></tr></table>					00	1100	dfff	ffff
00	1100	dfff	ffff						
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. 								
Words:	1								
Cycles:	1								
Example	RRF REG1,0								

RLF	Rotate Left f through Carry				
Syntax:	[<i>label</i>] RLF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	See description below				
Status Affected:	C				
Encoding:	<table><tr><td>00</td><td>1101</td><td>dfff</td><td>ffff</td></tr></table>	00	1101	dfff	ffff
00	1101	dfff	ffff		
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'. 				
Words:	1				
Cycles:	1				
Example	RLF REG1,0				
	Before Instruction				
	REG1 = 1110 0110				
	C = 0				
	After Instruction				
	REG1 = 1110 0110				
	W = 1100 1100				
	C = 1				

SLEEP	Go into Standby Mode				
Syntax:	[<i>label</i>] SLEEP				
Operands:	None				
Operation:	00h → WDT, 0 → WDT prescaler 1 → $\overline{\text{TO}}$, 0 → $\overline{\text{PD}}$				
Status Affected:	$\overline{\text{TO}}$, $\overline{\text{PD}}$				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0011</td></tr></table>	00	0000	0110	0011
00	0000	0110	0011		
Description:	The power down status bit ($\overline{\text{PD}}$) is cleared. Time-out status bit ($\overline{\text{TO}}$) is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.				
Words:	1				
Cycles:	1				
Example:	SLEEP				

SUBLW Subtract W from Literal

Syntax:	[<i>label</i>] SUBLW k				
Operands:	0 ≤ k ≤ 255				
Operation:	k − (W) → (W)				
Status Affected:	C, DC, Z				
Encoding:	<table><tr><td>11</td><td>110x</td><td>kkkk</td><td>kkkk</td></tr></table>	11	110x	kkkk	kkkk
11	110x	kkkk	kkkk		

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example 1: SUBLW 0x02

Before Instruction

W = 1
C = ?

After Instruction

W = 1
C = 1; result is positive

Example 2: Before Instruction

W = 2
C = ?

After Instruction

W = 0
C = 1; result is zero

Example 3: Before Instruction

W = 3
C = ?

After Instruction

W = FF
C = 0; result is negative

SUBWF Subtract W from f

Syntax:	[<i>label</i>] SUBWF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(f) - (W) \rightarrow (\text{dest})$				
Status Affected:	C, DC, Z				
Encoding:	<table><tr><td>00</td><td>0010</td><td>dfff</td><td>ffff</td></tr></table>	00	0010	dfff	ffff
00	0010	dfff	ffff		

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: SUBWF REG1,1

Before Instruction

REG1 = 3
W = 2
C = ?

After Instruction

REG1 = 1
W = 2
C = 1; result is positive

Example 2: Before Instruction

REG1 = 2
W = 2
C = ?

After Instruction

REG1 = 0
W = 2
C = 1; result is zero

Example 3: Before Instruction

REG1 = 1
W = 2
C = ?

After Instruction

REG1 = FF
W = 2
C = 0; result is negative

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SWAPF	Swap f
Syntax:	[<i>label</i> SWAPF f,d

TRIS	Load TRIS Register				
Syntax:	[<i>label</i>] TRIS f				
Operands:	$5 \leq f \leq 7$				
Operation:	(W) → TRIS register (f)				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0fff</td></tr></table>	00	0000	0110	0fff
00	0000	0110	0fff		
Description:	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.				
Words:	1				
Cycles:	1				
Example					
Note:	To maintain upward compatibility with future PIC16FXX products, do not use this instruction.				

XORLW		Exclusive OR Literal with W							
Syntax:	[<i>label</i>] XORLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	(W) .XOR. k $\rightarrow$ (W)								
Status Affected:	Z								
Encoding:	<table border="1"><tr><td>11</td><td>1010</td><td>kkkk</td><td>kkkk</td></tr></table>					11	1010	kkkk	kkkk
11	1010	kkkk	kkkk						
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.								
Words:	1								
Cycles:	1								
Example:	XORLW 0xAF								
	Before Instruction								
	W = 0xB5								
	After Instruction								
	W = 0x1A								

XORWF	Exclusive OR W with f				
Syntax:	[<i>label</i>] XORWF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	(W) .XOR. (f) $\rightarrow$ (dest)				
Status Affected:	Z				
Encoding:	<table><tr><td>00</td><td>0110</td><td>dfff</td><td>ffff</td></tr></table>	00	0110	dfff	ffff
00	0110	dfff	ffff		
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	XORWF REG 1 Before Instruction REG = 0xAF W = 0xB5 After Instruction REG = 0x1A W = 0xB5				

10.0 DEVELOPMENT SUPPORT

10.1 Development Tools

The PIC16/17 microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB-SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy logic development system (fuzzyTECH®-MP)

10.2 PICMASTER: High Performance Universal In-Circuit Emulator with MPLAB IDE

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX and PIC17CXX families. PICMASTER is supplied with the MPLAB™ Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

10.3 ICEPIC: Low-cost PIC16CXXX In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT® through Pentium™ based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

10.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC16C5X, PIC16CXXX, PIC17CXX and PIC14000 devices. It can also set configuration and code-protect bits in this mode.

10.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

10.6 PICDEM-1 Low-Cost PIC16/17 Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-16B programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

10.7 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-16C, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

10.8 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features

include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals. PICDEM-3 will be available in the 3rd quarter of 1996.

10.9 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC16/17 tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

10.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allow full symbolic debugging from the Microchip Universal Emulator System (PICMASTER).

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PIC16/17. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

10.11 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16/17 series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

10.12 C Compiler (MPLAB-C)

The MPLAB-C Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC16/17 family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display (PICMASTER emulator software versions 1.13 and later).

10.13 Fuzzy Logic Development System (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzyTECH-MP*, edition for implementing more complex systems.

Both versions include Microchip's *fuzzyLAB™* demonstration board for hands-on experience with fuzzy logic systems implementation.

10.14 MP-DriveWay™ – Application Code Generator

MP-DriveWay is an easy-to-use Windows-based Application Code Generator. With MP-DriveWay you can visually configure all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language. The output is fully compatible with Microchip's MPLAB-C C compiler. The code produced is highly modular and allows easy integration of your own code. MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

10.15 SEEVAL® Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

10.16 TrueGauge® Intelligent Battery Management

The TrueGauge development tool supports system development with the MTA11200B TrueGauge Intelligent Battery Management IC. System design verification can be accomplished before hardware prototypes are built. User interface is graphically-oriented and measured data can be saved in a file for exporting to Microsoft Excel.

10.17 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

TABLE 10-1: DEVELOPMENT TOOLS FROM MICROCHIP

Product	** MPLAB™ Integrated Development Environment	MPLAB™ C Compiler	MP-DriveWay Applications Code Generator	fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	*** PICMASTER®/PICMASTER-CE In-Circuit Emulator	ICEPIC Low-Cost In-Circuit Emulator	****PRO MATE™ II Universal Microchip Programmer	PICSTART® Lite Ultra Low-Cost Dev. Kit	PICSTART® Plus Low-Cost Universal Dev. Kit
PIC12C508, 509	SW007002	SW006005	—	—	EM167015/ EM167101	—	DV007003	—	DV003001
PIC14000	SW007002	SW006005	—	—	EM147001/ EM147101	—	DV007003	—	DV003001
PIC16C52, 54, 54A, 55, 56, 57, 58A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167015/ EM167101	EM167201	DV007003	DV162003	DV003001
PIC16C554, 556, 558	SW007002	SW006005	—	DV005001/ DV005002	EM167033/ EM167113	—	DV007003	—	DV003001
PIC16C61	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167021/ N/A	EM167205	DV007003	DV162003	DV003001
PIC16C62, 62A, 64, 64A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167025/ EM167103	EM167203	DV007003	DV162002	DV003001
PIC16C620, 621, 622	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167023/ EM167109	EM167202	DV007003	DV162003	DV003001
PIC16C63, 65, 65A, 73, 73A, 74, 74A	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167025/ EM167103	EM167204	DV007003	DV162002	DV003001
PIC16C642, 662*	SW007002	SW006005	—	—	EM167035/ EM167105	—	DV007003	DV162002	DV003001
PIC16C71	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167027/ EM167105	EM167205	DV007003	DV162003	DV003001
PIC16C710, 711	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167027/ EM167105	—	DV007003	DV162003	DV003001
PIC16C72	SW007002	SW006005	SW006006	—	EM167025/ EM167103	—	DV007003	DV162002	DV003001
PIC16F83	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	—	DV007003	DV162003	DV003001
PIC16C84	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	EM167206	DV007003	DV162003	DV003001
PIC16F84	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167029/ EM167107	—	DV007003	DV162003	DV003001
PIC16C923, 924*	SW007002	SW006005	SW006006	DV005001/ DV005002	EM167031/ EM167111	—	DV007003	—	DV003001
PIC17C42, 42A, 43, 44	SW007002	SW006005	SW006006	DV005001/ DV005002	EM177007/ EM177107	—	DV007003	—	DV003001

*Contact Microchip Technology for availability date

**MPLAB Integrated Development Environment includes MPLAB-SIM Simulator and MPASM Assembler

***All PICMASTER and PICMASTER-CE ordering part numbers above include PRO MATE II programmer

****PRO MATE socket modules are ordered separately. See development systems ordering guide for specific ordering part numbers

Product	TRUEGAUGE® Development Kit	SEEVAL® Designers Kit	Hopping Code Security Programmer Kit	Hopping Code Security Eval/Demo Kit
All 2 wire and 3 wire Serial EEPROM's	N/A	DV243001	N/A	N/A
MTA11200B	DV114001	N/A	N/A	N/A
HCS200, 300, 301 *	N/A	N/A	PG306001	DM303001

11.0 ELECTRICAL CHARACTERISTICS FOR PIC16F83 AND PIC16F84

Absolute Maximum Ratings †

Ambient temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS ⁽²⁾	-0.3 to +14V
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$)	-0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of VSS pin	150 mA
Maximum current into VDD pin	100 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	20 mA
Maximum current sunk by PORTA	80 mA
Maximum current sourced by PORTA	50 mA
Maximum current sunk by PORTB	150 mA
Maximum current sourced by PORTB	100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below VSS at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16F8X

Applicable Devices F83 CR83 F84 CR84

TABLE 11-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16F84-04 PIC16F83-04	PIC16F84-10 PIC16F83-10	PIC16LF84-04 PIC16LF83-04
RC	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 μ A max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μ A typ. at 5.5V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 7.0 μ A max. at 2V WDT dis Freq: 2.0 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 μ A max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μ A typ. at 5.5V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 7.0 μ A max. at 2V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 4.5 mA typ. at 5.5V IPD: 1.0 μ A typ. at 4.5V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V typ. IPD: 1.0 μ A typ. at 4.5V WDT dis Freq: 10 MHz max.	Do not use in HS mode
LP	VDD: 4.0V to 6.0V IDD: 35 μ A typ. at 32 kHz, 3.0V IPD: 0.6 μ A typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	VDD: 2.0V to 6.0V IDD: 32 μ A max. at 32 kHz, 3.0V IPD: 7 μ A max. at 2.0V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

11.1 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A	VDD	Supply Voltage	4.0 4.5	— —	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D010 D010A D013	IDD	Supply Current ⁽²⁾	— — —	1.8 7.3 5	4.5 10 10	mA mA mA	RC and XT osc configuration ⁽⁴⁾ FOSC = 4.0 MHz, VDD = 5.5V FOSC ≥ 4.0 MHz, VDD = 5.5V (During Flash programming) HS OSC CONFIGURATION (PIC16F84-10) FOSC = 10 MHz, VDD = 5.5V
D020 D021 D021A	IPD	Power-down Current ⁽³⁾	— — —	7.0 1.0 1.0	28 14 16	μA μA μA	VDD = 4.0V, WDT enabled, industrial VDD = 4.0V, WDT disabled, commercial VDD = 4.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

PIC16F8X

Applicable Devices F83 CR83 F84 CR84

11.2 DC CHARACTERISTICS: PIC16LF84, PIC16LF83 (Commercial, Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.0	—	6.0	V	XT, RC, and LP osc configuration
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D010 D010A D014	IDD	Supply Current ⁽²⁾	— — —	1 7.3 15	4 10 32	mA mA μA	RC and XT osc configuration ⁽⁴⁾ Fosc = 2.0 MHz, VDD = 5.5V Fosc = 2.0 MHz, VDD = 5.5V (During Flash programming) LP osc configuration Fosc = 32 kHz, VDD = 2.0V, WDT disabled
D020 D021 D021A	IPD	Power-down Current ⁽³⁾	— — —	3.0 0.4 0.4	16 7.0 9.0	μA μA μA	VDD = 2.0V, WDT enabled, industrial VDD = 2.0V, WDT disabled, commercial VDD = 2.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

11.3 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial) PIC16LF84, PIC16LF83 (Commercial, Industrial)

DC Characteristics		Standard Operating Conditions (unless otherwise stated)					
All Pins Except		Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)					
Power Supply Pins		Operating voltage V_{DD} range as described in DC spec Section 11.1 and Section 11.2.					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D034	V_{IL}	Input Low Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR, RA4/T0CKI OSC1 (XT, HS and LP modes) ⁽¹⁾ OSC1 (RC mode)	V_{SS} V_{SS} V_{SS} V_{SS} V_{SS} V_{SS}	— — — — — —	0.8 0.16 V_{DD} 0.2 V_{DD} 0.2 V_{DD} 0.3 V_{DD} 0.1 V_{DD}	V V V V V V	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ entire range ⁽⁴⁾ entire range
D040 D040A D041 D042 D043	V_{IH}	Input High Voltage I/O ports with TTL buffer with Schmitt Trigger buffer MCLR, RA4/T0CKI, OSC1 (RC mode) OSC1 (XT, HS and LP modes) ⁽¹⁾	2.4 0.48 V_{DD} 0.45 V_{DD} 0.85 V_{DD} 0.7 V_{DD}	— — — — —	V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}	V V V V V	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ entire range ⁽⁴⁾ entire range
D050	V_{HYS}	Hysteresis of Schmitt Trigger inputs	TBD	—	—	V	
D070	I_{PURB}	PORTB weak pull-up current	50*	250*	400*	μA	$V_{DD} = 5.0\text{V}$, $V_{PIN} = V_{SS}$
D060 D061 D063	I_{IL}	Input Leakage Current ^(2,3) I/O ports MCLR, RA4/T0CKI OSC1	— — —	— — —	± 1 ± 5 ± 5	μA μA μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance $V_{SS} \leq V_{PIN} \leq V_{DD}$ $V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration
D080 D083	V_{OL}	Output Low Voltage I/O ports OSC2/CLKOUT	— —	— —	0.6 0.6	V V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5\text{V}$ $I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5\text{V}$
D090 D092	V_{OH}	Output High Voltage I/O ports ⁽³⁾ OSC2/CLKOUT	$V_{DD}-0.7$ $V_{DD}-0.7$	— —	— —	V V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5\text{V}$ $I_{OH} = -1.3\text{ mA}$, $V_{DD} = 4.5\text{V}$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16F8X with an external clock while the device is in RC mode, otherwise chip damage may result.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may use better of the two specs.

PIC16F8X

Applicable Devices F83 CR83 F84 CR84

11.4 DC CHARACTERISTICS: PIC16F84, PIC16F83 (Commercial, Industrial) PIC16LF84, PIC16F83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) Operating voltage V_{DD} range as described in DC spec Section 11.1 and Section 11.2.					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100	Cosc2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	Cio	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
D120	ED	Data EEPROM Memory Endurance	1M	10M	—	E/W	25°C at 5V V_{MIN} = Minimum operating voltage
D121	VDRW	V_{DD} for read/write	V_{MIN}	—	6.0	V	
D122	TDEW	Erase/Write cycle time	—	—	10	ms	
D130	EP	Program Flash Memory Endurance	100	1000	—	E/W	V_{MIN} = Minimum operating voltage
D131	VPR	V_{DD} for read	V_{MIN}	—	6.0	V	
D132	VPEW	V_{DD} for erase/write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	10	—	ms	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 11-2: TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T		T	
F	Frequency	T	Time
Lowercase symbols (pp) and their meanings:			
pp		os,osc	OSC1
2	to	ost	oscillator start-up timer
ck	CLKOUT	pwrt	power-up timer
cy	cycle time	rbt	RBx pins
io	I/O port	t0	T0CKI
inp	INT pin	wdt	watchdog timer
mc	MCLR		
Uppercase symbols and their meanings:			
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	High Impedance
L	Low		

FIGURE 11-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.

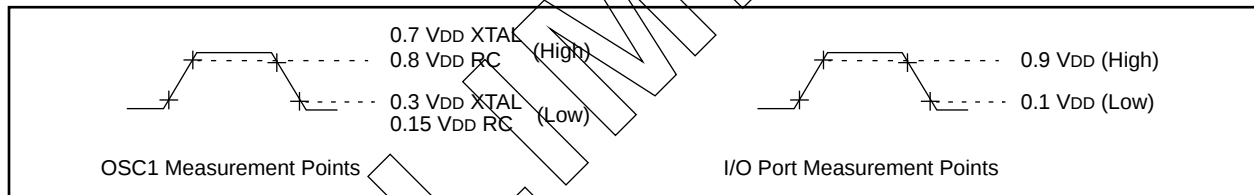
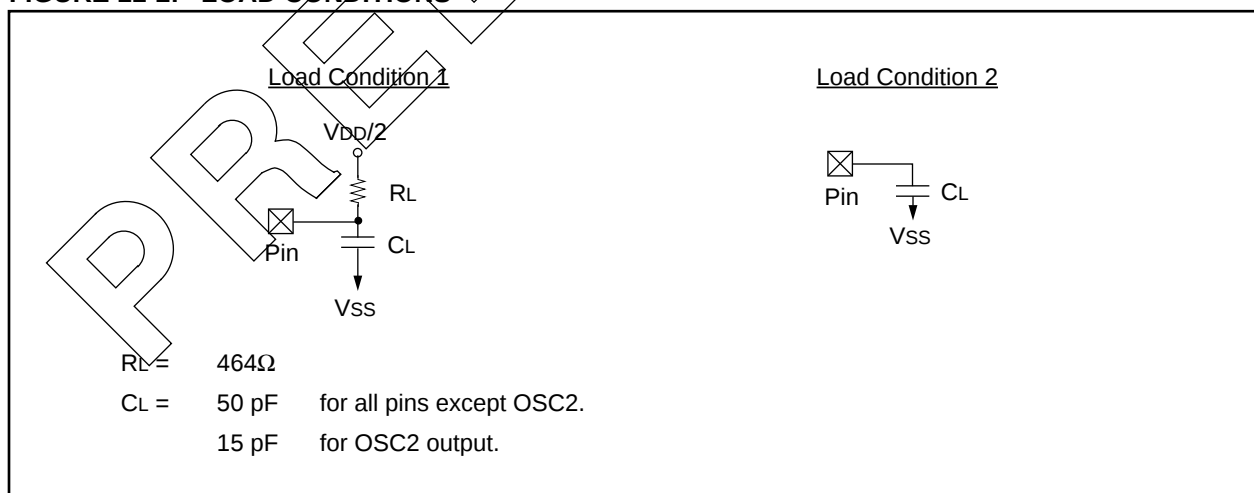


FIGURE 11-2: LOAD CONDITIONS



PIC16F8X

Applicable Devices F83 CR83 F84 CR84

11.5 Timing Diagrams and Specifications

FIGURE 11-3: EXTERNAL CLOCK TIMING

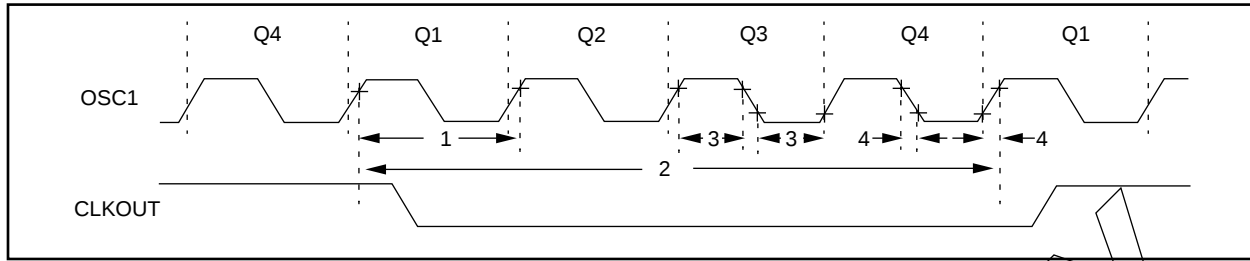


TABLE 11-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency⁽¹⁾	DC	—	2	MHz	XT, RC osc PIC16LF8X-04
			DC	—	4	MHz	XT, RC osc PIC16F8X-04
			DC	—	10	MHz	HS osc PIC16F8X-10
			DC	—	200	kHz	LP osc PIC16LF8X-04
		Oscillator Frequency⁽¹⁾	DC	—	2	MHz	RC osc PIC16LF8X-04
			DC	—	4	MHz	RC osc PIC16F8X-04
			0.1	—	2	MHz	XT osc PIC16LF8X-04
			0.1	—	4	MHz	XT osc PIC16F8X-04
			1.0	—	10	MHz	HS osc PIC16F8X-10
			DC	—	200	kHz	LP osc PIC16LF8X-04
1	Tosc	External CLKIN Period⁽¹⁾	500	—	—	ns	XT, RC osc PIC16LF8X-04
			250	—	—	ns	XT, RC osc PIC16F8X-04
			100	—	—	ns	HS osc PIC16F8X-10
			5.0	—	—	μs	LP osc PIC16LF8X-04
		Oscillator Period⁽¹⁾	500	—	—	ns	RC osc PIC16LF8X-04
			250	—	—	ns	RC osc PIC16F8X-04
			500	—	10,000	ns	XT osc PIC16LF8X-04
			250	—	10,000	ns	XT osc PIC16F8X-04
			100	—	1,000	ns	HS osc PIC16F8X-10
			5.0	—	—	μs	LP osc PIC16LF8X-04
2	Tcy	Instruction Cycle Time⁽¹⁾	0.4	4/Fosc	DC	μs	
3	TosL, TosH	Clock in (OSC1) High or Low Time	60 *	—	—	ns	XT osc PIC16LF8X-04
			50 *	—	—	ns	XT osc PIC16F8X-04
			2.0 *	—	—	μs	LP osc PIC16LF8X-04
			35 *	—	—	ns	HS osc PIC16F8X-10
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	25 *	—	—	ns	XT osc PIC16F8X-04
			50 *	—	—	ns	LP osc PIC16LF8X-04
			15 *	—	—	ns	HS osc PIC16F8X-10

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.

When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 11-4: CLKOUT AND I/O TIMING

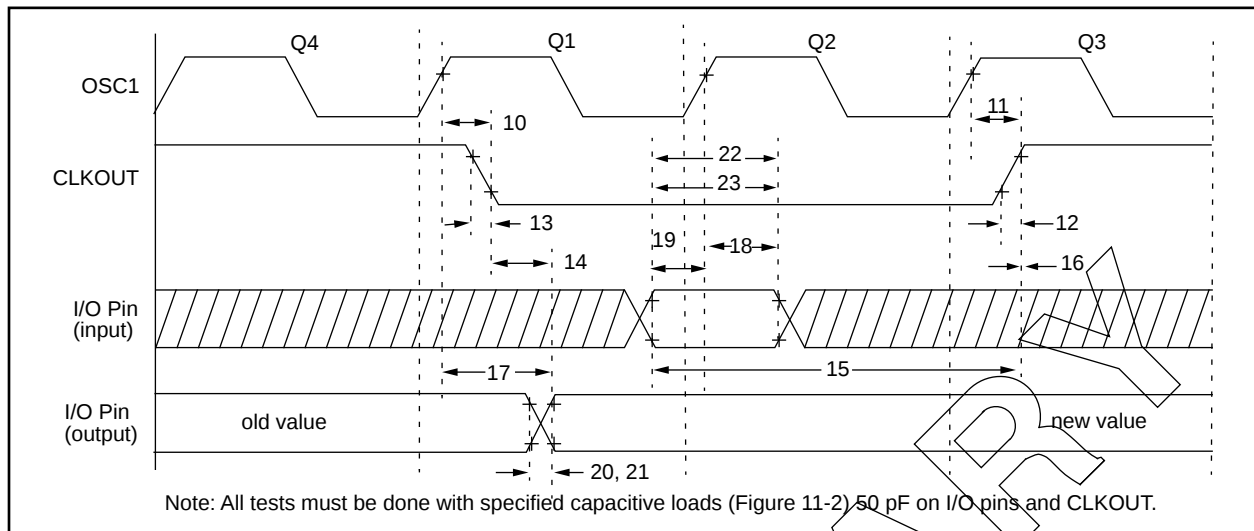


TABLE 11-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓		15	30 *	ns	Note 1
10A				15	120 *	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑		15	30 *	ns	Note 1
11A				15	120 *	ns	Note 1
12	TckR	CLKOUT rise time		15	30 *	ns	Note 1
12A				15	100 *	ns	Note 1
13	TckF	CLKOUT fall time		15	30 *	ns	Note 1
13A				15	100 *	ns	Note 1
14	TckL2ioV	CLKOUT ↓ to Port out valid			0.5Tcy + 20 *	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT ↑	PIC16F8X 0.30Tcy + 30 *			ns	Note 1
			PIC16LF8X 0.30Tcy + 80 *			ns	Note 1
16	TckH2iol	Port in hold after CLKOUT ↑	0 *			ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid			125 *	ns	
					250 *	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD			ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD			ns	
20	TioR	Port output rise time	PIC16F8X —	10	25 *	ns	
20A			PIC16LF8X —	10	60 *	ns	
21	TioF	Port output fall time	PIC16F8X —	10	25 *	ns	
21A			PIC16LF8X —	10	60 *	ns	
22	Tinp	INT pin high	PIC16F8X 20 *			ns	
22A		or low time	PIC16LF8X 55 *			ns	
23	Trbp	RB7:RB4 change INT	PIC16F8X Tosc §			ns	
23A		high or low time	PIC16LF8X Tosc §			ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

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Applicable Devices F83 CR83 F84 CR84

FIGURE 11-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

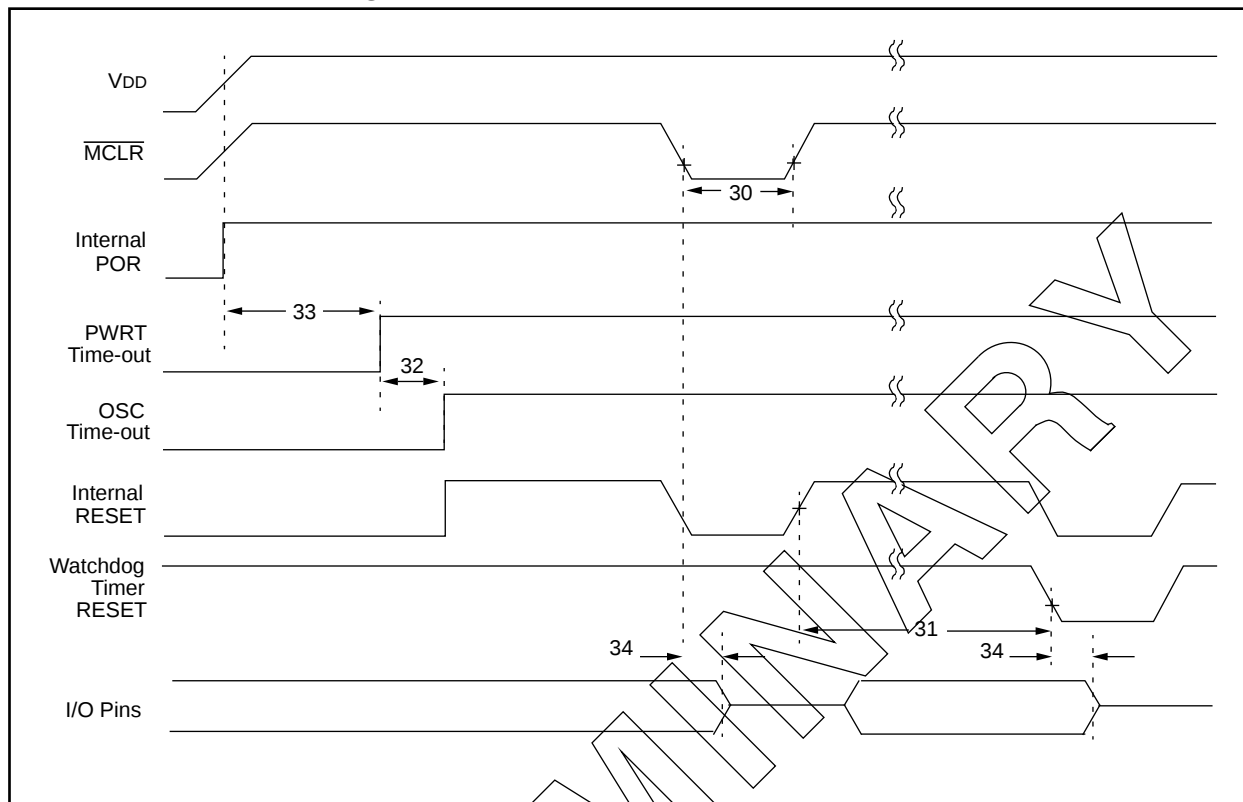


TABLE 11-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	1000 *	—	—	ns	2.0V ≤ VDD ≤ 6.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5.0V
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—	ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V
34	Tioz	I/O Hi-impedance from MCLR Low or reset	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-6: TIMER0 CLOCK TIMINGS

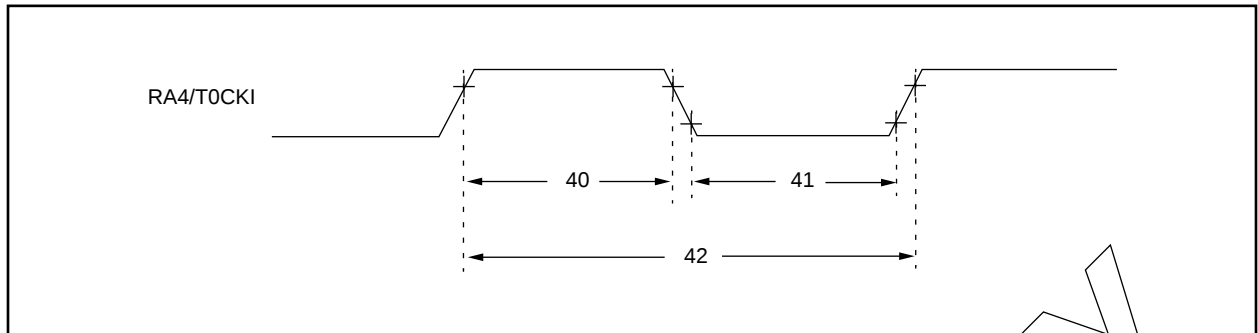


TABLE 11-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	TtOH	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	$2.0V \leq V_{DD} \leq 3.0V$ $3.0V \leq V_{DD} \leq 6.0V$
			With Prescaler	50^* 30^*	—	—	ns ns	
41	TtOL	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	$2.0V \leq V_{DD} \leq 3.0V$ $3.0V \leq V_{DD} \leq 6.0V$
			With Prescaler	50^* 20^*	—	—	ns ns	
42	TtOP	T0CKI Period		$T_{CY} + 40^*$ N	—	—	ns	N = prescale value (2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16F8X

Applicable Devices	F83	CR83	F84	CR84
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NOTES:

Applicable Devices	F83	CR83	F84	CR84
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12.0 DC & AC CHARACTERISTICS GRAPHS/TABLES FOR PIC16F83 AND PIC16F84

NOT AVAILABLE AT THIS TIME.

PIC16F8X

Applicable Devices	F83	CR83	F84	CR84
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NOTES:

13.0 ELECTRICAL CHARACTERISTICS FOR PIC16CR83 AND PIC16CR84

Absolute Maximum Ratings †

Ambient temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	-0.3 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS ⁽²⁾	-0.3 to +14V
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$)	-0.6V to (VDD + 0.6V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of VSS pin	150 mA
Maximum current into VDD pin	100 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	20 mA
Maximum current sunk by PORTA	80 mA
Maximum current sourced by PORTA	50 mA
Maximum current sunk by PORTB	150 mA
Maximum current sourced by PORTB	100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below VSS at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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Applicable Devices F83 CR83 F84 CR84

TABLE 13-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR84-04 PIC16CR83-04	PIC16CR84-10 PIC16CR83-10	PIC16LCR84-04 PIC16LCR83-04
RC	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 μ A max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μ A typ. at 5.5V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 6.0 μ A max. at 2V WDT dis Freq: 2.0 MHz max.
XT	VDD: 4.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 14 μ A max. at 4V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 1.8 mA typ. at 5.5V IPD: 1.0 μ A typ. at 5.5V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 6.0V IDD: 4.5 mA max. at 5.5V IPD: 6.0 μ A max. at 2V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 4.5 mA typ. at 5.5V IPD: 1.0 μ A typ. at 4.5V WDT dis Freq: 4.0 MHz max.	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V typ. IPD: 1.0 μ A typ. at 4.5V WDT dis Freq: 10 MHz max.	Do not use in HS mode
LP	VDD: 4.0V to 6.0V IDD: 35 μ A typ. at 32 kHz, 3.0V IPD: 0.6 μ A typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	VDD: 2.0V to 6.0V IDD: 32 μ A max. at 32 kHz, 3.0V IPD: 6.0 μ A max. at 2V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

13.1 DC CHARACTERISTICS: PIC16CR84, PIC16CR83 (Commercial, Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A	VDD	Supply Voltage	4.0 4.5	— —	6.0 5.5	V V	XT, RC and LP osc configuration HS osc configuration
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D010 D010A D013	IDD	Supply Current ⁽²⁾	— — —	1.8 7.3 5	4.5 10 10	mA mA mA	RC and XT osc configuration ⁽⁴⁾ FOSC = 4.0 MHz, VDD = 5.5V FOSC ≥ 4.0 MHz, VDD = 5.5V (During EEPROM programming) HS OSC CONFIGURATION (PIC16CR84-10) FOSC = 10 MHz, VDD = 5.5V
D020 D021 D021A	IPD	Power-down Current ⁽³⁾	— — —	7.0 1.0 1.0	28 14 16	μA μA μA	VDD = 4.0V, WDT enabled, industrial VDD = 4.0V, WDT disabled, commercial VDD = 4.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

PIC16F8X

Applicable Devices F83 CR83 F84 CR84

13.2 DC CHARACTERISTICS: PIC16LCR84, PIC16LCR83 (Commercial, Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.0	—	6.0	V	XT, RC, and LP osc configuration
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	1.5 *	—	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure internal Power-on Reset signal	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D010 D010A D014	IDD	Supply Current ⁽²⁾	— — —	1 7.3 15	4 10 32	mA mA μA	RC and XT osc configuration ⁽⁴⁾ FOSC = 2.0 MHz, VDD = 5.5V FOSC = 2.0 MHz, VDD = 5.5V (During EEPROM programming) LP osc configuration FOSC = 32 kHz, VDD = 2.0V, WDT disabled
D020 D021 D021A	IPD	Power-down Current ⁽³⁾	— — —	3.0 0.4 0.4	16 5.0 6.0	μA μA μA	VDD = 2.0V, WDT enabled, industrial VDD = 2.0V, WDT disabled, commercial VDD = 2.0V, WDT disabled, industrial

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to VDD, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_R = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

13.3 DC CHARACTERISTICS: PIC16CR84A, PIC16CR83 (Commercial, Industrial) PIC16LCR84, PIC16LCR83 (Commercial, Industrial)

DC Characteristics		Standard Operating Conditions (unless otherwise stated)					
All Pins Except		Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)					
Power Supply Pins		Operating voltage V_{DD} range as described in DC spec Section 13.1 and Section 13.2.					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D034	V _{IL}	Input Low Voltage					
		I/O ports					
		with TTL buffer	V _{SS}	—	0.8	V	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
			V _{SS}	—	0.16V _{DD}	V	entire range ⁽⁴⁾
		with Schmitt Trigger buffer	V _{SS}	—	0.2V _{DD}	V	entire range
		MCLR, RA4/T0CKI	V _{SS}	—	0.2V _{DD}	V	
D040 D040A D041 D042 D043	V _{IH}	Input High Voltage					
		I/O ports					
		with TTL buffer	2.4	—	V _{DD}	V	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
			0.48V _{DD}	—	V _{DD}	V	entire range ⁽⁴⁾
		with Schmitt Trigger buffer	0.45V _{DD}	—	V _{DD}	V	entire range
		MCLR, RA4/T0CKI, OSC1 (RC mode)	0.85 V _{DD}	—	V _{DD}	V	
D043 D050		OSC1 (XT, HS and LP modes) ⁽¹⁾	0.7 V _{DD}	—	V _{DD}	V	
D050	V _{HYS}	Hysteresis of Schmitt Trigger inputs	TBD	—	—	V	
D070	I _{PURB}	PORTB weak pull-up current	50*	250*	400*	μA	V _{DD} = 5.0V, V _{PIN} = V _{SS}
D060 D061 D063	I _{IL}	Input Leakage Current^(2,3)					
		I/O ports	—	—	±1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at hi-impedance
		MCLR, RA4/T0CKI	—	—	±5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
		OSC1	—	—	±5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT, HS and LP osc configuration
D080 D083	V _{OL}	Output Low Voltage					
		I/O ports	—	—	0.6	V	I _{OL} = 8.5 mA, V _{DD} = 4.5V
D090 D092	V _{OH}	Output High Voltage					
		I/O ports ⁽³⁾	V _{DD} -0.7	—	—	V	I _{OH} = -3.0 mA, V _{DD} = 4.5V
D090 D092		OSC2/CLKOUT	V _{DD} -0.7	—	—	V	I _{OH} = -1.3 mA, V _{DD} = 4.5V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1 pin is a Schmitt Trigger input. Do not drive the PIC16CR8X with an external clock while the device is in RC mode, otherwise chip damage may result.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: The user may use better of the two specs.

PIC16F8X

Applicable Devices F83 CR83 F84 CR84

13.4 DC CHARACTERISTICS: PIC16CR84A, PIC16CR83 (Commercial, Industrial) PIC16LCR84A, PIC16LCR83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) Operating voltage V_{DD} range as described in DC spec Section 13.1 and Section 13.2.					
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100	Cosc2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
D120	ED	Data EEPROM Memory Endurance	1M	10M	—	EW	25°C at 5V V_{MIN} = Minimum operating voltage
D121	VDRW	V_{DD} for read/write	V_{MIN}	—	6.0	V	
D122	TDEW	Erase/Write cycle time	—	—	10	ms	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 13-2: TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T		T	
F	Frequency	T	Time
Lowercase symbols (pp) and their meanings:			
pp		os,osc	OSC1
2	to	ost	oscillator start-up timer
ck	CLKOUT	pwrt	power-up timer
cy	cycle time	rbt	RBx pins
io	I/O port	t0	T0CKI
inp	INT pin	wdt	watchdog timer
mc	MCLR		
Uppercase symbols and their meanings:			
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	High Impedance
L	Low		

FIGURE 13-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.

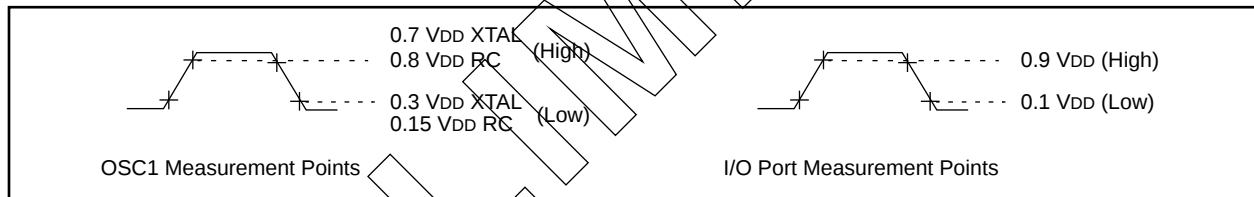
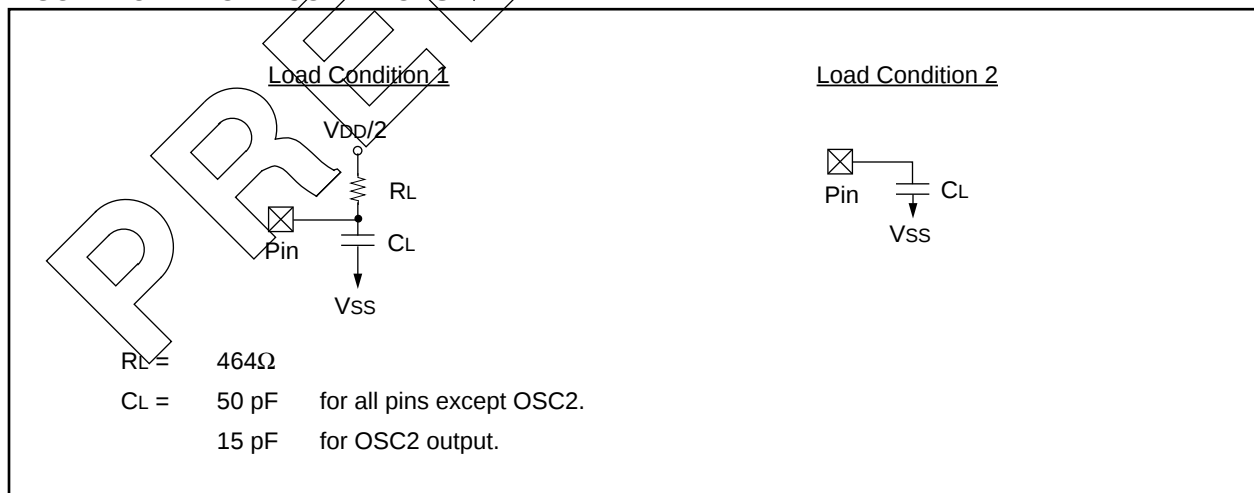


FIGURE 13-2: LOAD CONDITIONS



PIC16F8X

Applicable Devices F83 CR83 F84 CR84

13.5 Timing Diagrams and Specifications

FIGURE 13-3: EXTERNAL CLOCK TIMING

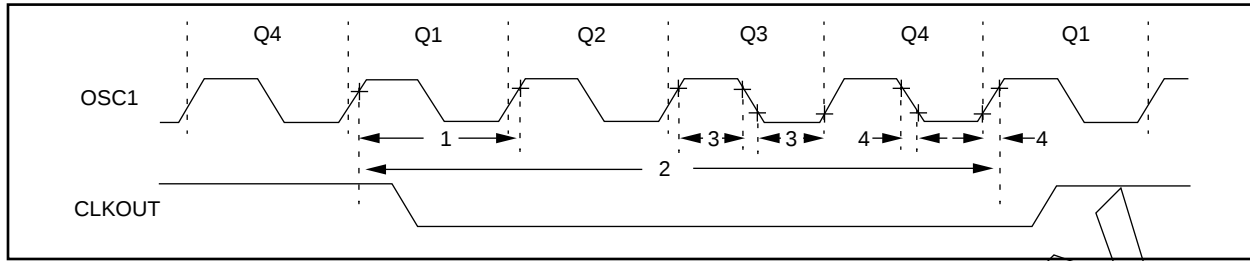


TABLE 13-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency ⁽¹⁾	DC	—	2	MHz	XT, RC osc PIC16LCR8X-04
			DC	—	4	MHz	XT, RC osc PIC16CR8X-04
			DC	—	10	MHz	HS osc PIC16CR8X-10
			DC	—	200	kHz	LP osc PIC16LCR8X-04
		Oscillator Frequency ⁽¹⁾	DC	—	2	MHz	RC osc PIC16LCR8X-04
			DC	—	4	MHz	RC osc PIC16CR8X-04
			0.1	—	2	MHz	XT osc PIC16LCR8X-04
			0.1	—	4	MHz	XT osc PIC16CR8X-04
			1.0	—	10	MHz	HS osc PIC16CR8X-10
			DC	—	200	kHz	LP osc PIC16LCR8X-04
1	Tosc	External CLKIN Period ⁽¹⁾	500	—	—	ns	XT, RC osc PIC16LCR8X-04
			250	—	—	ns	XT, RC osc PIC16CR8X-04
			100	—	—	ns	HS osc PIC16CR8X-10
			5.0	—	—	μs	LP osc PIC16LCR8X-04
		Oscillator Period ⁽¹⁾	500	—	—	ns	RC osc PIC16LCR8X-04
			250	—	—	ns	RC osc PIC16CR8X-04
			500	—	10,000	ns	XT osc PIC16LCR8X-04
			250	—	10,000	ns	XT osc PIC16CR8X-04
			100	—	1,000	ns	HS osc PIC16CR8X-10
			5.0	—	—	μs	LP osc PIC16LCR8X-04
2	Tcy	Instruction Cycle Time ⁽¹⁾	0.4	4/Fosc	DC	μs	
3	TosL, TosH	Clock in (OSC1) High or Low Time	60 *	—	—	ns	XT osc PIC16LCR8X-04
			50 *	—	—	ns	XT osc PIC16CR8X-04
			2.0 *	—	—	μs	LP osc PIC16LCR8X-04
			35 *	—	—	ns	HS osc PIC16CR8X-10
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	25 *	—	—	ns	XT osc PIC16CR8X-04
			50 *	—	—	ns	LP osc PIC16LCR8X-04
			15 *	—	—	ns	HS osc PIC16CR8X-10

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1 pin.

When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 13-4: CLKOUT AND I/O TIMING

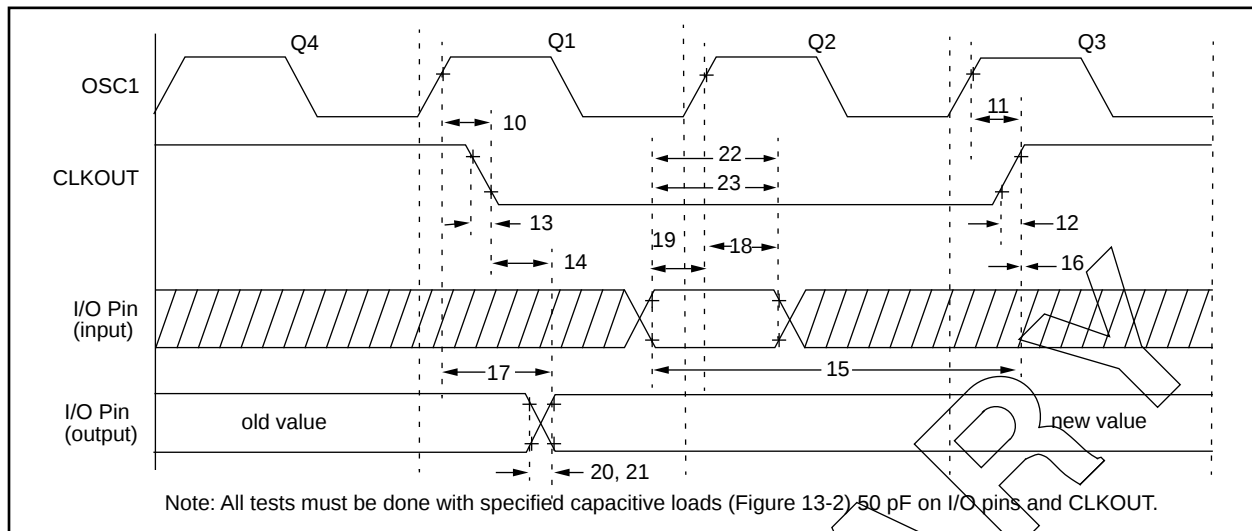


TABLE 13-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓		15	30 *	ns	Note 1
10A				15	120 *	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑		15	30 *	ns	Note 1
11A				15	120 *	ns	Note 1
12	TckR	CLKOUT rise time		15	30 *	ns	Note 1
12A				15	100 *	ns	Note 1
13	TckF	CLKOUT fall time		15	30 *	ns	Note 1
13A				15	100 *	ns	Note 1
14	TckL2ioV	CLKOUT↓ to Port out valid			0.5Tcy + 20 *	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT↑	PIC16CR8X 0.30Tcy + 30 *			ns	Note 1
			PIC16LCR8X 0.30Tcy + 80 *			ns	Note 1
16	TckH2iol	Port in hold after CLKOUT↑	0 *			ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid			125 *	ns	
					250 *	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD			ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD			ns	
20	TioR	Port output rise time	PIC16CR8X —	10	25 *	ns	
20A			PIC16LCR8X —	10	60 *	ns	
21	TioF	Port output fall time	PIC16CR8X —	10	25 *	ns	
21A			PIC16LCR8X —	10	60 *	ns	
22	Tinp	INT pin high or low time	PIC16CR8X 20 *			ns	
22A			PIC16LCR8X 55 *			ns	
23	Trbp	RB7:RB4 change INT high or low time	PIC16CR8X Tosc §			ns	
23A			PIC16LCR8X Tosc §			ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

PIC16F8X

Applicable Devices F83 CR83 F84 CR84

FIGURE 13-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

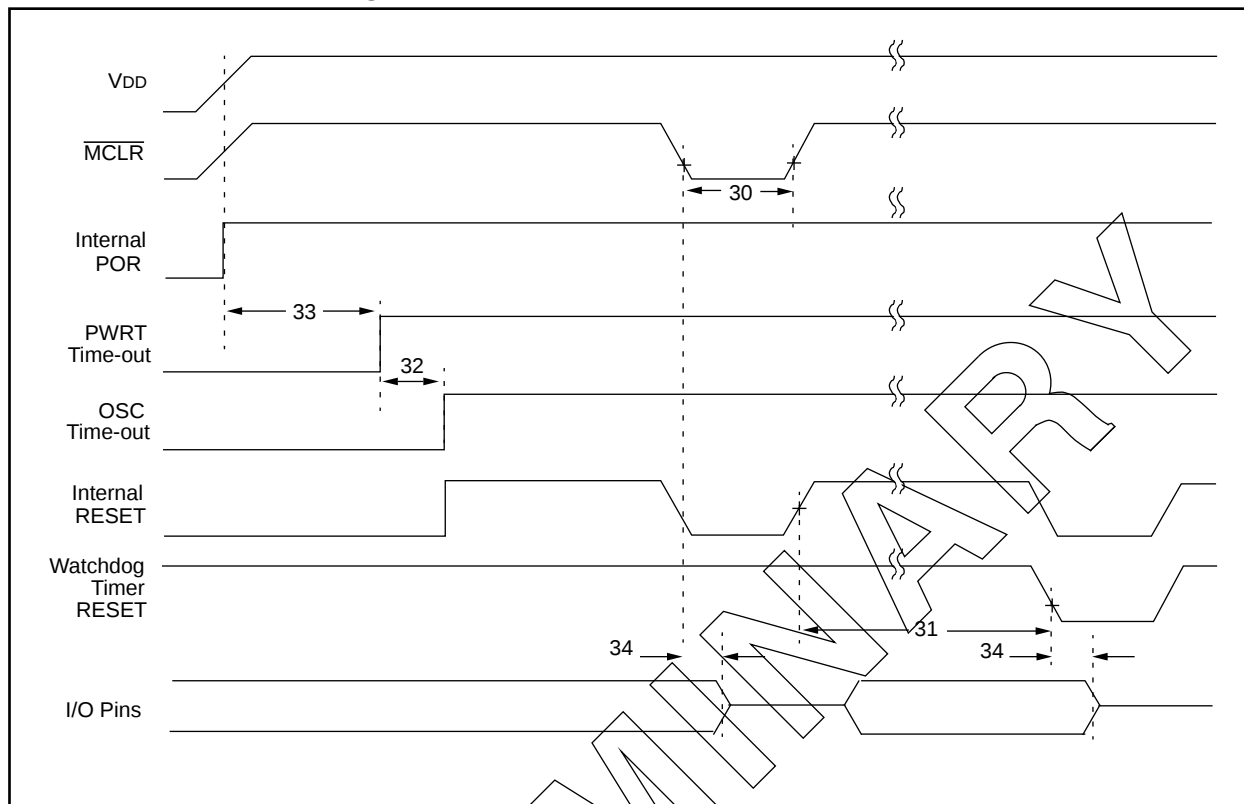


TABLE 13-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	1000 *	—	—	ns	2.0V ≤ VDD ≤ 6.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5.0V
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—	ms	Tosc = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V
34	Tioz	I/O Hi-impedance from MCLR Low or reset	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-6: TIMER0 CLOCK TIMINGS

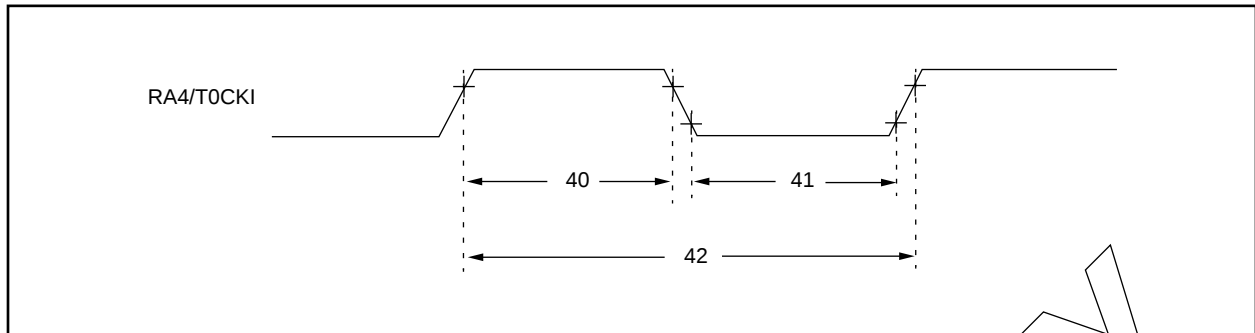


TABLE 13-6: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	TtOH	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	$2.0V \leq V_{DD} \leq 3.0V$ $3.0V \leq V_{DD} \leq 6.0V$
			With Prescaler	50^* 30^*	—	—	ns	
41	TtOL	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	$2.0V \leq V_{DD} \leq 3.0V$ $3.0V \leq V_{DD} \leq 6.0V$
			With Prescaler	50^* 20^*	—	—	ns	
42	TtOP	T0CKI Period		$T_{CY} + 40^*$ N	—	—	ns	N = prescale value (2, 4, ..., 256)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16F8X

Applicable Devices	F83	CR83	F84	CR84
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NOTES:

14.0 DC & AC CHARACTERISTICS GRAPHS/TABLES FOR PIC16CR83 AND PIC16CR84

NOT AVAILABLE AT THIS TIME.

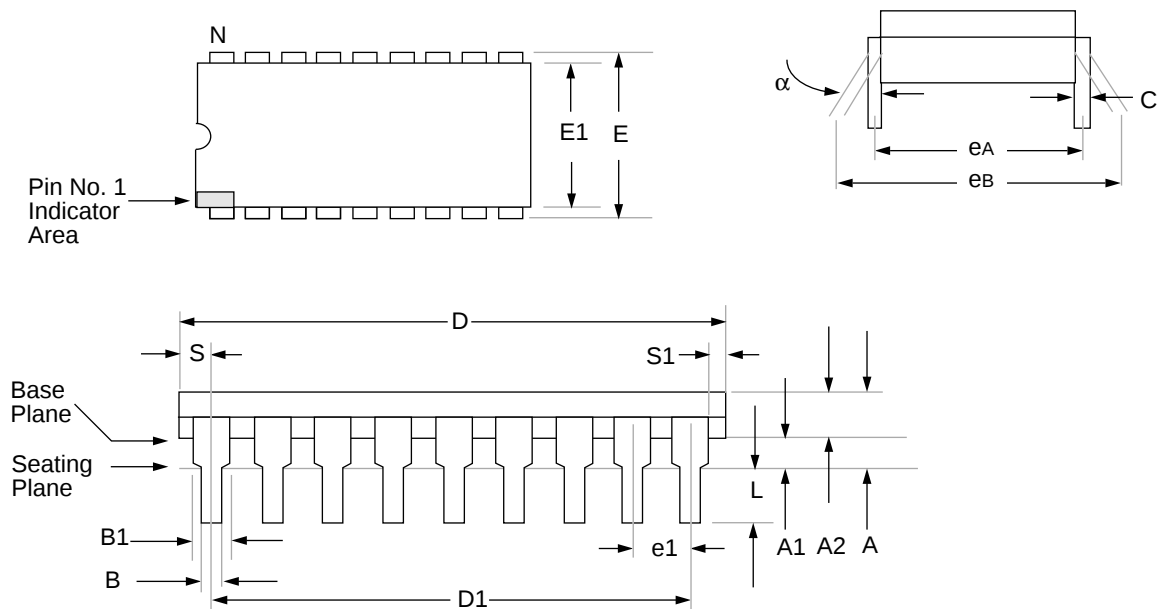
PIC16F8X

Applicable Devices	F83	CR83	F84	CR84
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NOTES:

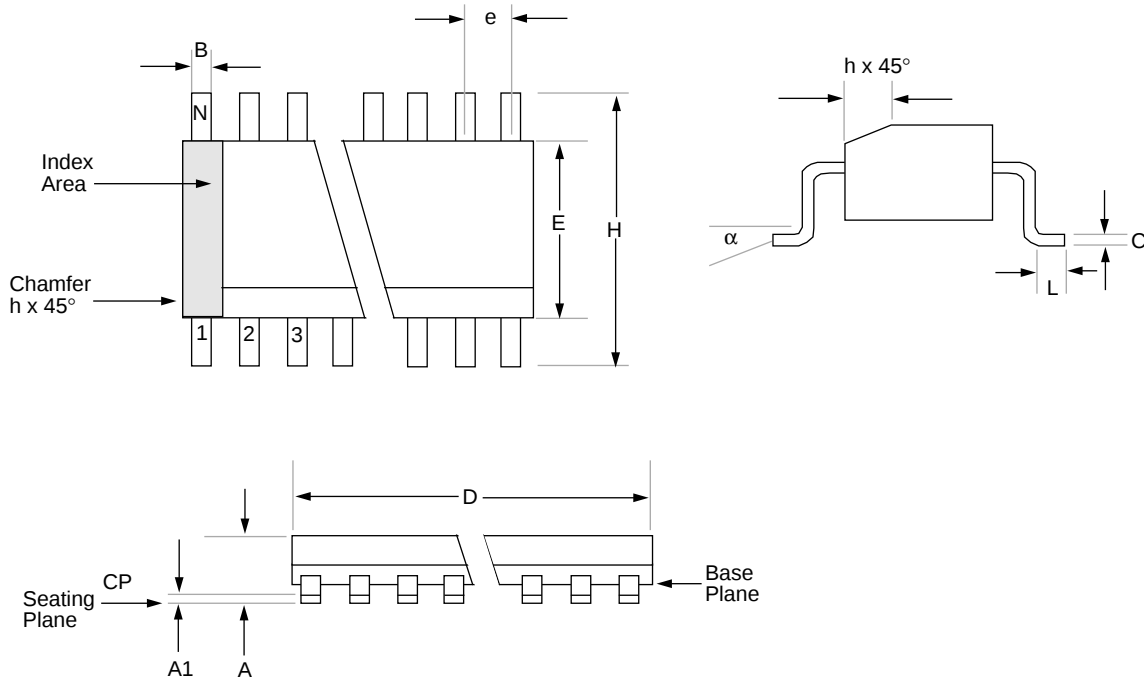
PIC16F8X

15.2 18-Lead Plastic Dual In-line (PDIP) - 300 mil



Package Group: Plastic Dual In-Line (PLA)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	10°		0°	10°	
A	—	4.064		—	0.160	
A1	0.381	—		0.015	—	
A2	3.048	3.810		0.120	0.150	
B	0.355	0.559		0.014	0.022	
B1	1.524	1.524	Reference	0.060	0.060	Reference
C	0.203	0.381	Typical	0.008	0.015	Typical
D	22.479	23.495		0.885	0.925	
D1	20.320	20.320	Reference	0.800	0.800	Reference
E	7.620	8.255		0.300	0.325	
E1	6.096	7.112		0.240	0.280	
e1	2.489	2.591	Typical	0.098	0.102	Typical
eA	7.620	7.620	Reference	0.300	0.300	Reference
eB	7.874	9.906		0.310	0.390	
L	3.048	3.556		0.120	0.140	
N	18	18		18	18	
S	0.889	—		0.035	—	
S1	0.127	—		0.005	—	

15.3 18-Lead Plastic Surface Mount (SOIC) - 300 mil



Package Group: Plastic SOIC (SO)						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
α	0°	8°		0°	8°	
A	2.362	2.642		0.093	0.104	
A1	0.101	0.300		0.004	0.012	
B	0.355	0.483		0.014	0.019	
C	0.241	0.318		0.009	0.013	
D	11.353	11.735		0.447	0.462	
E	7.416	7.595		0.292	0.299	
e	1.270	1.270	Reference	0.050	0.050	Reference
H	10.007	10.643		0.394	0.419	
h	0.381	0.762		0.015	0.030	
L	0.406	1.143		0.016	0.045	
N	18	18		18	18	
CP	—	0.102		—	0.004	

PIC16F8X

NOTES:

APPENDIX A: FEATURE IMPROVEMENTS

The following is the list of feature improvements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and the register file (128 bytes now versus 32 bytes before).
2. A PC latch register (PCLATH) is added to handle program memory paging. PA2, PA1 and PA0 bits are removed from the status register and placed in the option register.
3. Data memory paging is redefined slightly. The STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions, TRIS and OPTION, are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, the Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change features.
13. T0CKI pin is also a port pin (RA4/T0CKI).
14. FSR is a full 8-bit register.
15. "In system programming" is made possible. The user can program PIC16FXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).

APPENDIX B: COMPATIBILITY

To convert code written for PIC16C5X to PIC16F8X, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables for reallocation.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

APPENDIX C: WHAT'S NEW

Not applicable - new document.

APPENDIX D: WHAT'S CHANGES

Not applicable - new document.

APPENDIX E: PIC16C84 TO PIC16F83/CR83 AND PIC16F84/CR84 CONVERSION CONSIDERATIONS

This appendix discusses some of the issues that you may encounter as you convert your design from a PIC16C84 to a PIC16F83 or PIC16F84 device. These new devices are:

- PIC16F83
- PIC16CR83
- PIC16F84
- PIC16CR84

Some of the issues that may be encountered are:

1. The polarity of the PWRTE configuration bit has been reversed. Ensure that the programmer has this bit correctly set before programming.
2. The PIC16F84 and PIC16CR84 have larger RAM sizes. Ensure that this does not cause an issue with your program.
3. The $\overline{\text{MCLR}}$ pin now has an on-chip filter. The input signal on the $\overline{\text{MCLR}}$ pin will require a longer low pulse to generate an interrupt.
4. Many electrical specifications have been improved. Compare the electrical specifications of the two devices to ensure that this will not cause a compatibility issue.

APPENDIX F: PIC16/17 MICROCONTROLLERS

F.1 PIC14000 Devices

PIC14000	Memory				Peripherals				Features			
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (K14 words)	Data Memory (bytes)	Timer Module(s)	Serial Ports (SPI/I ² C, USART)	Slope A/D Converter (high-res) Channels	Interrupt Sources	I/O Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Additional On-chip Features	Packages
PIC14000	20	4K	192	TMR0 ADTMR	I ² C/ SMBus	14	11	22	2.7-6.0	Yes	Internal Oscillator, Bandgap Reference, Temperature Sensor, Calibration Factors, Low Voltage Detector, SLEEP, HIBERNATE, Comparators with Programmable References (2)	28-pin DIP, SOIC, SSOP (.300 mil)

PIC16F8X

F.2 PIC16C5X Family of Devices

	Clock			Memory		Peripherals		Features	
	Maximum Frequency of Operation (MHz)			Program Memory (x12 words)		Timer Module(s)		Number of Instructions	
		EPROM	ROM	RAM Data Memory (bytes)		I/O Pins		Voltage Range (Volts)	
									Packages
PIC16C52	4	384	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC
PIC16C54	20	512	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C54A	20	512	—	25	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR54A	20	—	512	25	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C55	20	512	—	24	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C56	20	1K	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16C57	20	2K	—	72	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16CR57B	20	—	2K	72	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C58A	20	2K	—	73	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR58A	20	—	2K	73	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

F.3 PIC16CXXX Family of Devices

	Clock			Memory			Peripherals			Features		
	Maximum Frequency of Operation (MHz)	EPROM	Data Memory (bytes)	Program Memory (K14 words)	Timer Modules	Comparators	Internal Reference Voltage	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Brown-out Reset	Packages
PIC16C554	20	512	80	TMR0	—	—	3	13	2.5-6.0	—	—	18-pin DIP, SOIC; 20-pin SSOP
PIC16C556	20	1K	80	TMR0	—	—	3	13	2.5-6.0	—	—	18-pin DIP, SOIC; 20-pin SSOP
PIC16C558	20	2K	128	TMR0	—	—	3	13	2.5-6.0	—	—	18-pin DIP, SOIC; 20-pin SSOP
PIC16C620	20	512	80	TMR0	2	Yes	4	13	2.5-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C621	20	1K	80	TMR0	2	Yes	4	13	2.5-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP
PIC16C622	20	2K	128	TMR0	2	Yes	4	13	2.5-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16C6XXX Family devices use serial programming with clock pin RB6 and data pin RB7.

PIC16F8X

F.4 PIC16C6X Family of Devices

	Clock		Memory			Peripherals				Features																	
	Maximum Frequency of Operation (MHz)		Program Memory (Kx14 words)			Timer Modules(s)				Serial Ports (SPI/I ² C, USART)		Capture/Compare/PWM Modules(s)		Parallel Slave Port		Interrupt Sources		I/O Pins		Voltage Range (Volts)		In-Circuit Serial Programming		Brown-out Reset		Packages	
	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I ² C	—	7	22	3.0-6.0	Yes	—	28-pin SDIP, SOIC, SSOP													
PIC16C62																											
PIC16C62A ⁽¹⁾	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I ² C	—	7	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP													
PIC16CR62 ⁽¹⁾	20	—	2K	128	TMR0, TMR1, TMR2	1	SPI/I ² C	—	7	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC, SSOP													
PIC16C63	20	4K	—	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	—	10	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC													
PIC16CR63 ⁽¹⁾	20	—	4K	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	—	10	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC													
PIC16C64	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I ² C	Yes	8	33	3.0-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP													
PIC16C64A ⁽¹⁾	20	2K	—	128	TMR0, TMR1, TMR2	1	SPI/I ² C	Yes	8	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP													
PIC16CR64 ⁽¹⁾	20	—	2K	128	TMR0, TMR1, TMR2	1	SPI/I ² C	Yes	8	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP													
PIC16C65	20	4K	—	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	Yes	11	33	3.0-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP													
PIC16C65A ⁽¹⁾	20	4K	—	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	Yes	11	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP													
PIC16CR65 ⁽¹⁾	20	—	4K	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	Yes	11	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP													

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16C6X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

F.5 PIC16C7X Family of Devices

	Clock		Memory		Peripherals					Features				
	Maximum Frequency of Operation (MHz)	EPROM Program Memory (Kx4 words)	Data Memory (bytes)	Timer Modules(s)	Capture/Compare/PWM Modules(s)	Serial Ports (SPI/I ² C, USART)	A/D Converter (8-bit) Channels	Interrupt Sources	I/O Pins	Voltage Range (Volts)	In-Circuit Serial Programming	Brown-out Reset	Packages	
PIC16C710	20	512	36	TMR0	—	—	4	4	13	2.5-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP	
PIC16C71	20	1K	36	TMR0	—	—	4	4	13	2.5-6.0	Yes	—	18-pin DIP, SOIC	
PIC16C711	20	1K	68	TMR0	—	—	4	4	13	2.5-6.0	Yes	Yes	18-pin DIP, SOIC; 20-pin SSOP	
PIC16C72	20	2K	128	TMR0, TMR1, TMR2	1	SPI/I ² C	—	5	8	22	2.5-6.0	Yes	28-pin SDIP, SOIC, SSOP	
PIC16C73	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	—	5	11	22	2.5-6.0	Yes	—	28-pin SDIP, SOIC
PIC16C73A ⁽¹⁾	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	—	5	11	22	2.5-6.0	Yes	Yes	28-pin SDIP, SOIC
PIC16C74	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	Yes	8	12	33	2.5-6.0	Yes	—	40-pin DIP; 44-pin PLCC, MQFP
PIC16C74A ⁽¹⁾	20	4K	192	TMR0, TMR1, TMR2	2	SPI/I ² C, USART	Yes	8	12	33	2.5-6.0	Yes	Yes	40-pin DIP; 44-pin PLCC, MQFP, TQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16C7X Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

PIC16F8X

F.6 PIC16C8X Family of Devices

	Clock			Memory			Peripherals		Features												
	Maximum Frequency of Operation (MHz)			Program Memory			Data EEPROM (bytes)			Data Memory (bytes)		Timer Modules		Interrupt Sources		I/O Pins		Voltage Range (Volts)		Packages	
PIC16C84	10	—	1K	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC										
PIC16F84 ⁽¹⁾	10	1K	—	—	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC										
PIC16CR84 ⁽¹⁾	10	—	—	1K	68	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC										
PIC16F83 ⁽¹⁾	10	512	—	—	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC										
PIC16CR83 ⁽¹⁾	10	—	—	512	36	64	TMR0	4	13	2.0-6.0	18-pin DIP, SOIC										

All PIC16/17 family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect, and high I/O current capability.

All PIC16C8X family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local sales office for availability of these devices.

F.7 PIC16C9XX Family Of Devices

	Clock		Memory		Peripherals						Features			
	8	4K	176	TMR0, TMR1, TMR2	1 SPI/I ² C	—	—	4 Com 32 Seg	8	25	27	3.0-6.0	Yes	—
PIC16C923														64-pin SDIP ⁽¹⁾ , TQFP, 68-pin PLCC, DIE
PIC16C924	8	4K	176	TMR0, TMR1, TMR2	1 SPI/I ² C	—	5	4 Com 32 Seg	9	25	27	3.0-6.0	Yes	—
														64-pin SDIP ⁽¹⁾ , TQFP, 68-pin PLCC, DIE

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC16CXX Family devices use serial programming with clock pin RB6 and data pin RB7.

Note 1: Please contact your local Microchip representative for availability of this package.

PIC16F8X

F.8 PIC17CXX Family of Devices

	Clock			Memory			Peripherals				Features		
	Maximum Frequency of Operation (MHz)	Program Memory (Words)	RAM Data Memory (bytes)	Timer Module(s)	Captures/PWMs	Serial Port(s) (USART)	Hardware Multiplex	External Interrupts	Interrupt Sources	I/O Pins	Voltage Range (Volts)	Number of Instructions	Packages
PIC17C42	25	2K	—	232	2	2	Yes	—	Yes	11	33	4.5-5.5	55 40-pin DIP; 44-pin PLCC, MQFP
PIC17C42A	25	2K	—	232	2	2	Yes	Yes	Yes	11	33	2.5-6.0	58 40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17CR42	25	—	2K	232	2	2	Yes	Yes	Yes	11	33	2.5-6.0	58 40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17C43	25	4K	—	454	2	2	Yes	Yes	Yes	11	33	2.5-6.0	58 40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17CR43	25	—	4K	454	2	2	Yes	Yes	Yes	11	33	2.5-6.0	58 40-pin DIP; 44-pin PLCC, TQFP, MQFP
PIC17C44	25	8K	—	454	2	2	Yes	Yes	Yes	11	33	2.5-6.0	58 40-pin DIP; 44-pin PLCC, TQFP, MQFP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

PIN COMPATIBILITY

Devices that have the same package type and VDD, VSS and MCLR pin locations are said to be pin compatible. This allows these different devices to operate in the same socket. Compatible devices may only require minor software modification to allow proper operation in the application socket (ex., PIC16C56 and PIC16C61 devices). Not all devices in the same package size are pin compatible; for example, the PIC16C62 is compatible with the PIC16C63, but not the PIC16C55.

Pin compatibility does not mean that the devices offer the same features. As an example, the PIC16C54 is pin compatible with the PIC16C71, but does not have an A/D converter, weak pull-ups on PORTB, or interrupts.

TABLE F-1: PIN COMPATIBLE DEVICES

Pin Compatible Devices	Package
PIC12C508, PIC12C509	8-pin
PIC16C54, PIC16C54A, PIC16CR54A, PIC16C56, PIC16C58A, PIC16CR58A, PIC16C61, PIC16C554, PIC16C556, PIC16C558 PIC16C620, PIC16C621, PIC16C622, PIC16C710, PIC16C71, PIC16C711, PIC16F83, PIC16CR83, PIC16C84, PIC16F84A, PIC16CR84	18-pin 20-pin
PIC16C55, PIC16C57, PIC16CR57B	28-pin
PIC16C62, PIC16CR62, PIC16C62A, PIC16C63, PIC16C72, PIC16C73, PIC16C73A	28-pin
PIC16C64, PIC16CR64, PIC16C64A, PIC16C65, PIC16C65A, PIC16C74, PIC16C74A	40-pin
PIC17C42, PIC17CR42, PIC17C42A, PIC17C43, PIC17CR43, PIC17C44	40-pin
PIC16C923, PIC16C924	64/68-pin

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1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe access number.
3. Depress the <Enter> key and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type +, depress the <Enter> key and "Host Name:" will appear.
5. Type MCHIPBBS, depress the <Enter> key and you will be connected to the Microchip BBS.

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PIC16F8X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-XX</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Frequency Range	Temperature Range	Package	Pattern
Device	PIC16F8X ⁽²⁾ , PIC16F8XT ⁽³⁾ PIC16LF8X ⁽²⁾ , PIC16LF8XT ⁽³⁾ PIC16CR8X ⁽²⁾ , PIC16CR8XT ⁽³⁾ PIC16LCR8X ⁽²⁾ , PIC16LCR8XT ⁽³⁾			
Frequency Range	04 = 4 MHz 10 = 10 MHz			
Temperature Range	b ⁽¹⁾ = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)			
Package	P = PDIP SO = SOIC (Gull Wing, 300 mil body)			
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)			

Examples:

a) PIC16F84 -04/P 301 = Commercial temp., PDIP package, 4 MHz, normal V_{DD} limits, QTP pattern #301.

b) PIC16LF84 - 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended V_{DD} limits.

c) PIC16CR84 - 10I/P = ROM program memory, Industrial temp., PDIP package, 10MHz, normal V_{DD} limits.

Note 1: b = blank
 2: F = Standard V_{DD} range
 LF = Extended V_{DD} range
 CR = ROM Version, Standard V_{DD} range
 LCR = ROM Version, Extended V_{DD} range
 3: T = in tape and reel - SOIC, SSOP packages only.

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Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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