Foto 1 : Bagian Atas dari Alat

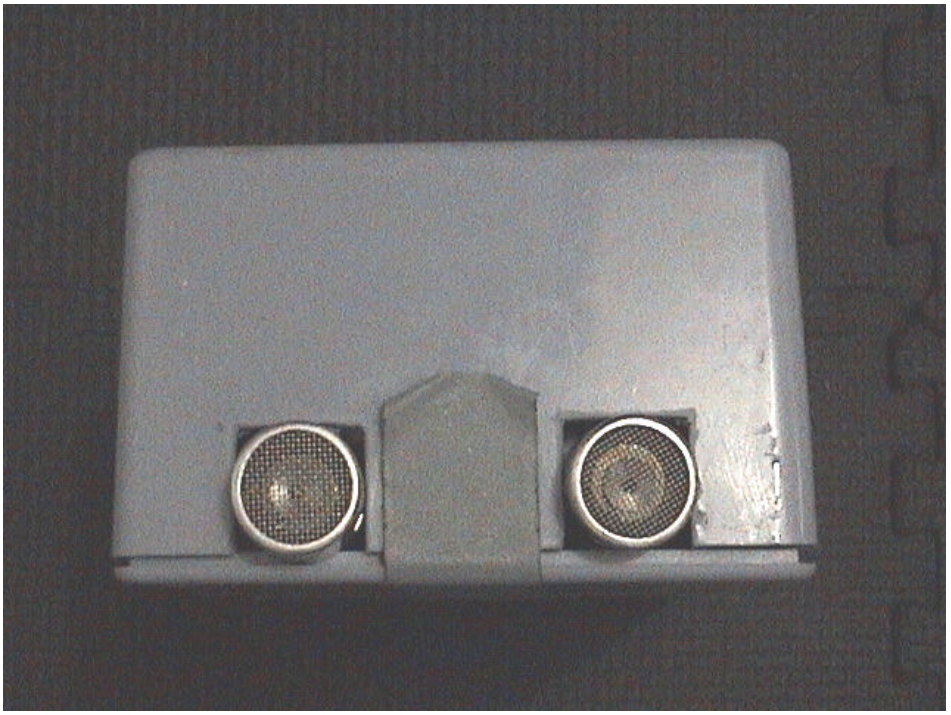


Foto 2 : Bagian Depan dari Alat

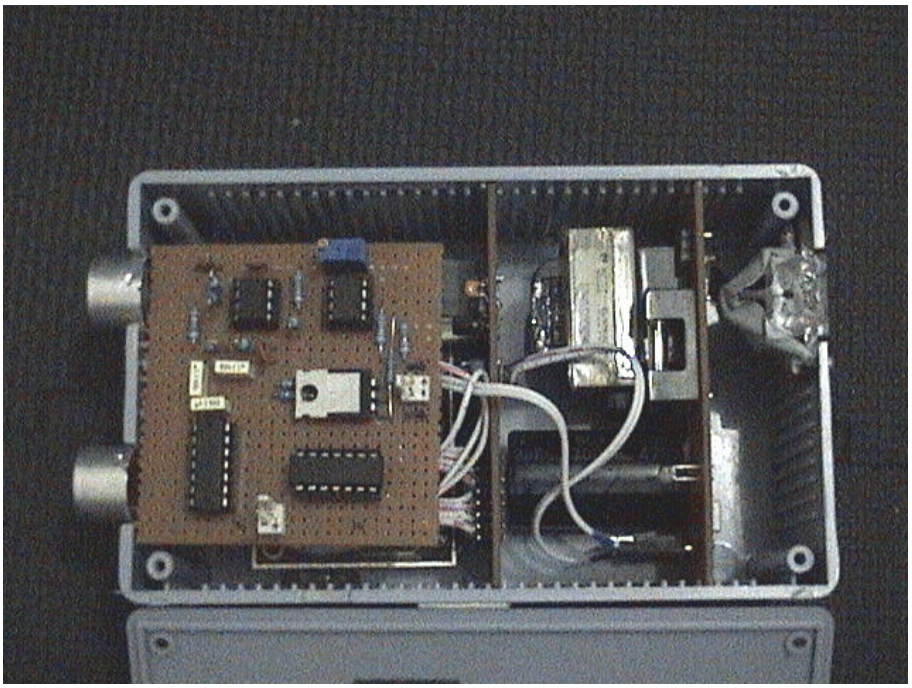
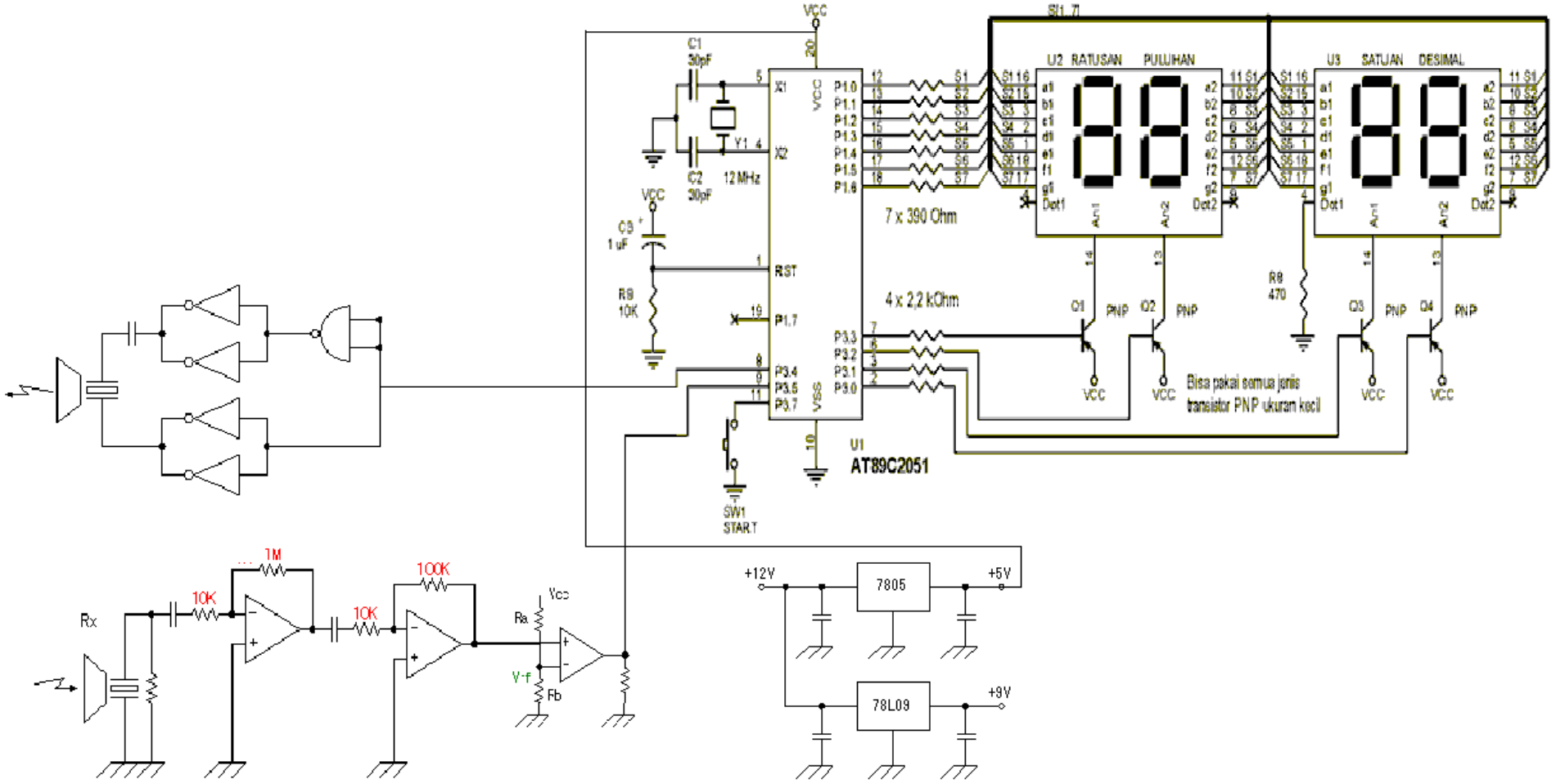


Foto 3 : Bagian Dalam dari Alat


VCC
C1
30pF
X1
X2
Y1
12 MHz
C2
30pF
C3
1 uF
RST
R8
10K
P1.7
P3.4
P3.5
P3.7
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P3.3
P3.2
P3.1
P3.0
VSS
U1
AT89C2051
SW1
START
7 x 390 Ohm
4 x 2,2 kOhm
U2 RATUSAN PULUHAN
U3 SATUAN DESIMAL
Dot1
Dot2
R9
470
Q1
Q2
Q3
Q4
PNP
Bisa pakai semua jenis
transistor PNP ukuran kecil
1M
10K
100K
Rx
Ra
Vcc
V-f
Fb
+12V
7805
+5V
78L09
+9V

```
;-- Display Port & RAMs --;
    DisDat  EQU P1
    PS1     BIT P3.0
    PS2     BIT P3.1
    PS3     BIT P3.2
    PS4     BIT P3.3
    dg1     EQU 08h
    dg2     EQU 09h
    dg3     EQU 0Ah
    dg4     EQU 0Bh

    APar2   EQU 0Ch
    APar1   EQU 0Dh
    SPar2   EQU 0Eh
    SPar1   EQU 0Fh
    MPar2   EQU 10h
    MPar1   EQU 11h
    DPar2   EQU 12h
    DPar1   EQU 13h

    RBak2   EQU 14h
    RBak1   EQU 15h

    J1_2    EQU 16h
    J1_1    EQU 17h
    J2_2    EQU 18h
    J2_1    EQU 19h

    p50ms   EQU 20h
    FLAG    EQU 21h
      Sdh5    BIT FLAG.0
;-- Others Port & RAMs --;
    SOut    BIT P3.4
    SIn     BIT P3.5
    Button  BIT P3.7

;--------------------------------------------------------------------------------
org 00h
        jmp mulai
org 0Bh
        jmp T0_Vect

;--------------------------------------------------------------------------------
mulai:
        ;-- Inisialisasi Var& Port
        mov SP, #22h
        mov DisDat, #0FFh
        setb PS1
        setb PS2
        setb PS3
        setb PS4
        setb SOut
        setb SIn
        mov dg4, #10h
        mov dg3, #10h
        mov dg2, #10h
        mov dg1, #10h
        ;-- Inisialisasi Timer
        mov TMOD, #51h
        clr TR1
        clr TR0
        clr ET1
        clr ET0
    ulang:
```

```
        ;--- Tembakan Pertama
        mov TH0, #00h
        mov TL0, #00h
        mov TH1, #00h
        mov TL1, #00h
        clr TF0
        setb TR1
        setb TR0
        mov b, #40
    ambil_frek:
        cpl SOut
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        djnz b, ambil_frek
        ;---
    tunggu:
        mov a, TL1
        jnz dapat
        jnb TF0, tunggu
        clr TR1
        clr TR0
        jmp ulang
    dapat:
        clr TR0
        clr TR1
        ;--- Simpan Jarak-1
        mov J1_2, TH0
        mov J1_1, TL0

        ;--- Tunggu 500 ms
        clr Sdh5
        mov TH0, #03Ch
        mov TL0, #0B0h
        mov p50ms, #10
        setb TR0
        setb ET0
        setb EA
    dly500ms:
        call show7s
        jnb Sdh5, dly500ms
;        mov R0, #10         ; 1   ( R0 = x )
;    dly500ms_1:
;        mov R1, #100        ; x   ( R1 = y )
;    dly500ms_2:
;        mov R2, #245        ; y*x ( R2 = z )
;        djnz R2, $          ; 2*z*y*x
;        djnz R1, dly500ms_2 ; 2*y*x
;        djnz R0, dly500ms_1 ; 2*x

        ;--- Tembakan Kedua
        mov TH0, #00h
        mov TL0, #00h
        mov TH1, #00h
        mov TL1, #00h
        clr TF0
        setb TR1
        setb TR0
```

```
    mov b, #40
ambil_frek2:
    cpl SOut
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    djnz b, ambil_frek2
    ;---
tunggu2:
    mov a, TL1
    jnz dapat2
    jnb TF0, tunggu2
    clr TR1
    clr TR0
    jmp ulang
dapat2:
    clr TR0
    clr TR1
    ;--- Hitung Jarak-2
    mov dph, TH0
    mov dpl, TL0
    mov DPar2, #0
    mov DPar1, #125
    call div_int

    mov MPar2, #0
    mov MPar1, #2
    call mul_int
    mov J2_2, dph
    mov J2_1, dpl

    ;--- Hitung Jarak-1
    mov dph, J1_2
    mov dpl, J1_1
    mov DPar2, #0
    mov DPar1, #125
    call div_int

    mov MPar2, #0
    mov MPar1, #2
    call mul_int
    mov J1_2, dph
    mov J1_1, dpl

    ;-- Cek Mana Yang Besar
    mov a, J2_2
    clr c
    subb a, J1_2
    jc J2_Lebih_Kecil
    jnz J2_Lebih_Besar

    mov a, J2_1
    clr c
    subb a, J1_1
    jc J2_Lebih_Kecil
    jnz J2_Lebih_Besar

    ;-- Jarak Sama, V = cm/s
```

```
    mov dg4, #0
    mov dg3, #0
    mov dg2, #0
    mov dg1, #0
    jmp ulang

J2_Lebih_Kecil:
    mov dph, J1_2
    mov dpl, J1_1
    mov SPar2, J2_2
    mov SPar1, J2_1
    call subb_int
    jmp Ubah_KeDesimal

J2_Lebih_Besar:
    mov dph, J2_2
    mov dpl, J2_1
    mov SPar2, J1_2
    mov SPar1, J1_1
    call subb_int

Ubah_KeDesimal:
    ;-- Kali 2 Dulu
    mov MPar2, #0
    mov MPar1, #2
    call mul_int
    ;-- Yang akan ditampilkan
    mov RBak2, dph      ; Rb-Rs-Pl-St
    mov RBak1, dpl

    ; Ambil Ribuan
    mov DPar2, #003h
    mov DPar1, #0E8h
    call div_int        ; Rb-Rs-Pl-St/1000 = Rb
    mov dg4, dpl        ; Get <Rb>
    ; Ambil ratusan
    mov MPar2, #003h
    mov MPar1, #0E8h
    call mul_int        ; Rb*1000
    mov SPar2, dph
    mov SPar1, dpl
    mov dph, RBak2
    mov dpl, RBak1
    call subb_int       ; Rb-Rs-Pl-St - Rb*1000 = Rs-Pl-St

    mov RBak2, dph      ; Rs-Pl-St
    mov RBak1, dpl

    mov DPar2, #0
    mov DPar1, #100
    call div_int        ; Rs-Pl-St/100 = Rs
    mov dg3, dpl        ; Get <Rs>
    ; Ambil Puluhan
    mov MPar2, #0
    mov MPar1, #100
    call mul_int        ; Rs*100
    mov SPar2, dph
    mov SPar1, dpl
    mov dph, RBak2
    mov dpl, RBak1
    call subb_int       ; Rs-Pl-St - Rs*100 = Pl-St

    mov RBak2, dph      ; Pl-St
    mov RBak1, dpl
```

```
        mov DPar2, #0
        mov DPar1, #10
        call div_int        ; Pl-St/10 = Pl
        mov dg2, dpl        ; Get <Pl>
        ; Ambil Satuan
        mov MPar2, #0
        mov MPar1, #10
        call mul_int        ; Pl*10
        mov SPar2, dph
        mov SPar1, dpl
        mov dph, RBak2
        mov dpl, RBak1
        call subb_int       ; Pl-St - Pl*10 = St

        mov dg1, dpl        ; Get <St>

        jmp ulang

;-------------------------------------------------------------------------------
T0_Vect:
        push psw
        clr TR0
        mov TH0, #03Ch
        mov TL0, #0B0h
        setb TR0
        djnz p50ms, T0_Vect_End
        clr TR0
        clr ET0
        clr EA
        setb Sdh5
    T0_Vect_End:
        pop psw
        reti

;-------------------------------------------------------------------------------
dly_key:
    ;-- Delay Sampai Tombol Dilepas
        push 0h
        push 1h
    dk_ulang:
        mov R0, #200
    dly_key_:
        call show7s
        djnz R0, dly_key_
        jnb Button, dk_ulang
        pop 1h
        pop 0h
        ret

;-------------------------------------------------------------------------------
show7s:
    ;-- Tampilkan Angka Ke Display
        push acc
        push 0h
        mov dptr, #db7s
        ;-- Show Digit-4
        mov a, dg4
        movc a, @a+dptr
        mov DisDat, a
        clr PS4
        call dly7s
        setb PS4
        ;-- Show Digit-3
```

```
        mov a, dg3
        movc a, @a+dptr
        mov DisDat, a
        clr PS3
        call dly7s
        setb PS3
        ;-- Show Digit-2
        mov a, dg2
        movc a, @a+dptr
        mov DisDat, a
        clr PS2
        call dly7s
        setb PS2
        ;-- Show Digit-1
        mov a, dg1
        movc a, @a+dptr
        mov DisDat, a
        clr PS1
        call dly7s
        setb PS1
        pop 0h
        pop acc
        ret
dly7s:
     ;-- Delay Tahan
        mov R0, #100
        djnz R0, $
        ret
db7s:
    ;-- Data Base Kombinasi Segmen
;      -gfedcba
    db 11000000b ; 0
    db 11111001b ; 1
    db 10100100b ; 2
    db 10110000b ; 3
    db 10011001b ; 4
    db 10010010b ; 5
    db 10000010b ; 6
    db 11111000b ; 7
    db 10000000b ; 8
    db 10010000b ; 9
    db 10001000b ; A
    db 10000011b ; B
    db 11000110b ; C
    db 10100001b ; D
    db 10000110b ; E
    db 10001110b ; F
    db 11111111b ; Blank (17)

;-------------------------------------------------------------------------------;
add_int:
    ; [DPH:DPL] + [APar2:APar1] -> [DPH:DPL]
    push acc
        mov a, APar1
        add a, dpl
        mov dpl, a
        mov a, APar2
        addc a, dph
        mov dph, a
    pop acc
    ret

;-------------------------------------------------------------------------------;
subb_int:
```

```
    ; [DPH:DPL] - [SPar2:SPar1] -> [DPH:DPL]
    push acc
        clr c
        mov a, dpl
        subb a, SPar1
        mov dpl, a
        mov a, dph
        subb a, SPar2
        mov dph, a
    pop acc
    ret

;-------------------------------------------------------------------------------;
mul_int:
    ; [DPH:DPL] X [MPar2:MPar1] -> [DPH:DPL]
    push acc
    push b
        mov a, dpl
        mov b, MPar1
        mul ab
        xch a, dpl
        push b
        mov b, MPar2
        mul ab
        pop b
        add a, b
        xch a, dph
        mov b, MPar1
        mul ab
        add a, dph
        mov dph, a
    pop b
    pop acc
    ret

;-------------------------------------------------------------------------------;
div_int:
    ; [DPH:DPL] / [DPar2:DPar1] -> [DPH:DPL]
    push acc
    push b
    push 2h
    push 3h
    push 4h
        mov r2, #16
        clr a
        mov r3, a
        mov r4, a
    di_loop:
        mov a, dpl
        add a, acc
        mov dpl, a
        mov a, dph
        rlc a
        mov dph, a
        mov a, r3
        rlc a
        mov r3, a
        mov a, r4
        rlc a
        mov r4, a
        mov a, r3
        subb a, DPar1
        mov b, a
        mov a, r4
```

```
        subb a, DPar2
        jc di_smaller
        mov r4, a
        mov r3, b
        orl dpl, #1
    di_smaller:
        djnz r2, di_loop
    pop 4h
    pop 3h
    pop 2h
    pop b
    pop acc
    ret

end
```

Features

- **Compatible with MCS-51™ Products**
- **2K Bytes of Reprogrammable Flash Memory**
  - **Endurance: 1,000 Write/Erase Cycles**
- **2.7V to 6V Operating Range**
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Two-level Program Memory Lock**
- **128 x 8-bit Internal RAM**
- **15 Programmable I/O Lines**
- **Two 16-bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial UART Channel**
- **Direct LED Drive Outputs**
- **On-chip Analog Comparator**
- **Low-power Idle and Power-down Modes**

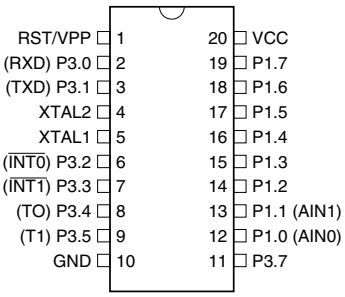
Description

The AT89C2051 is a low-voltage, high-performance CMOS 8-bit microcomputer with 2K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C2051 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89C2051 provides the following standard features: 2K bytes of Flash, 128 bytes of RAM, 15 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, a precision analog comparator, on-chip oscillator and clock circuitry. In addition, the AT89C2051 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Configuration

PDIP/SOIC

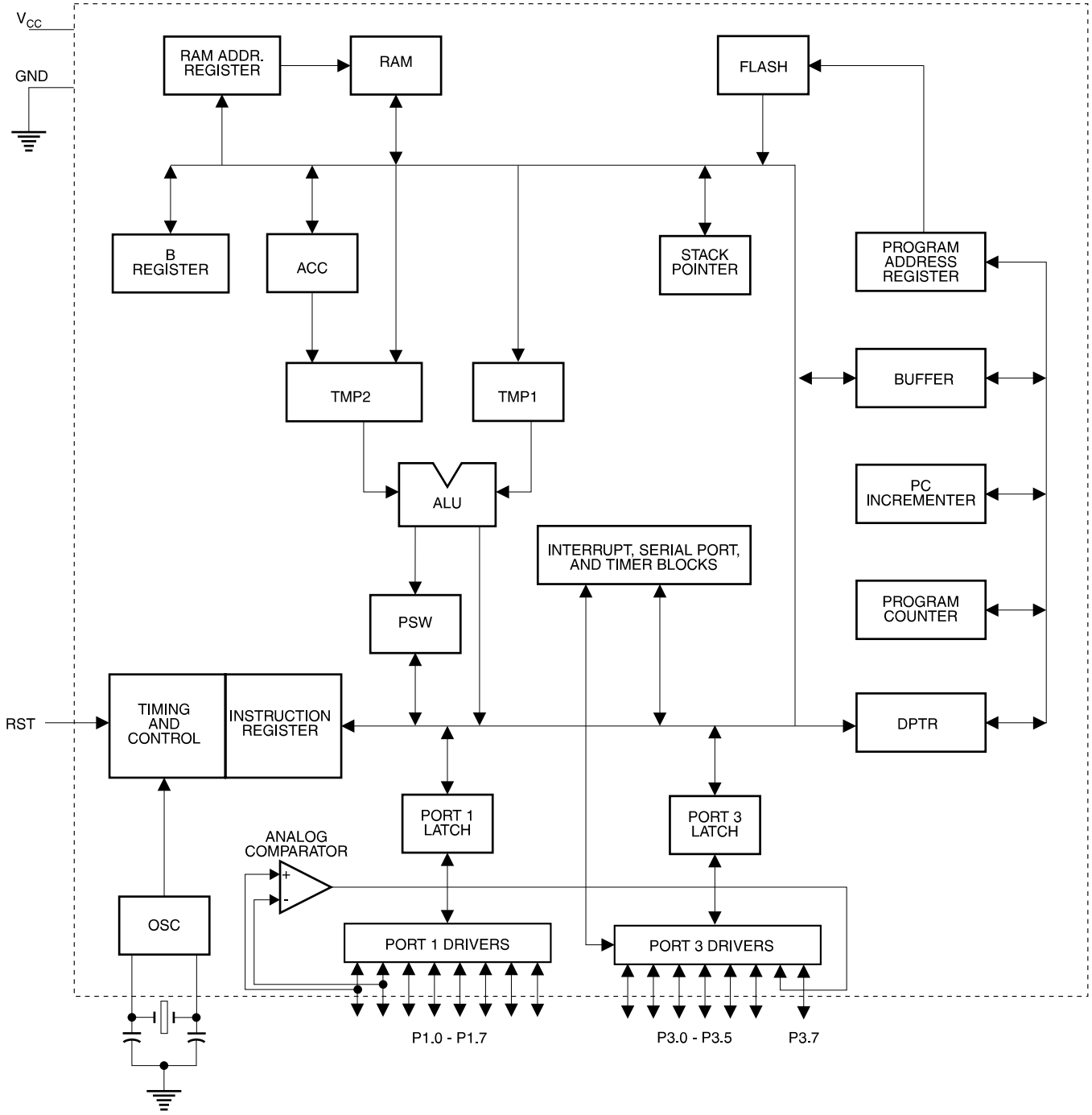


8-bit Microcontroller with 2K Bytes Flash

AT89C2051

Rev. 0368E–02/00

Block Diagram



Pin Description

VCC

Supply voltage.

GND

Ground.

Port 1

Port 1 is an 8-bit bi-irectional I/O port. Port pins P1.2 to P1.7 provide internal pullups. P1.0 and P1.1 require external pullups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (I_{IL}) because of the internal pullups.

Port 1 also receives code data during Flash programming and verification.

Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bi-irectional I/O pins with internal pullups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C2051 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. All I/O pins are reset to 1s as soon as RST goes high. Holding the RST pin high for two machine cycles while the oscillator is running resets the device.

Each machine cycle takes 12 oscillator or clock cycles.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

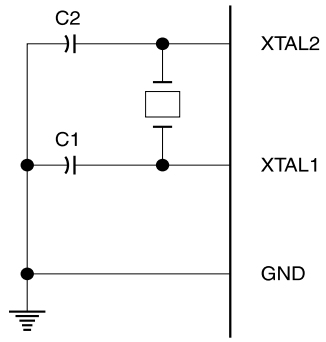
XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

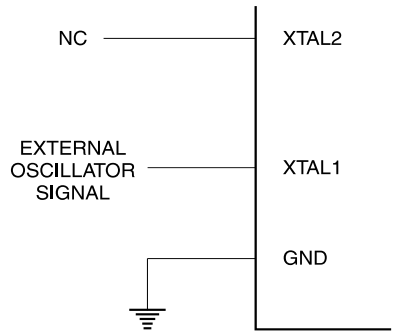
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in the table below.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Table 1. AT89C2051 SFR Map and Reset Values

0F8H									0FFH
0F0H	B 00000000								0F7H
0E8H									0EFH
0E0H	ACC 00000000								0E7H
0D8H									0DFH
0D0H	PSW 00000000								0D7H
0C8H									0CFH
0C0H									0C7H
0B8H	IP XXX00000								0BFH
0B0H	P3 11111111								0B7H
0A8H	IE 0XX00000								0AFH
0A0H									0A7H
98H	SCON 00000000	SBUF XXXXXXXX							9FH
90H	P1 11111111								97H
88H	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8FH
80H		SP 00000111	DPL 00000000	DPH 00000000				PCON 0XXX0000	87H

Restrictions on Certain Instructions

The AT89C2051 and is an economical and cost-effective member of Atmel's growing family of microcontrollers. It contains 2K bytes of flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K for the AT89C2051. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89C2051 (with 2K of memory), whereas LJMP 900H would not.

1. Branching instructions:

LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR

These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 7FFH for the 89C2051). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ With these conditional branching instructions the same rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

2. MOVX-related instructions, Data Memory:

The AT89C2051 contains 128 bytes of internal data memory. Thus, in the AT89C2051 the stack depth is limited to 128 bytes, the amount of available RAM. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the controller user to know the physical features and limitations of the device being used and adjust the instructions used correspondingly.

Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

Lock Bit Protection Modes[1]

Program Lock Bits			
	LB1	LB2	Protection Type
1	U	U	No program lock features.
2	P	U	Further programming of the Flash is disabled.
3	P	P	Same as mode 2, also verify is disabled.

Note: 1. The Lock Bits can only be erased with the Chip Erase operation.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

P1.0 and P1.1 should be set to "0" if no external pullups are used, or set to "1" if external pullups are used.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Power-down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

P1.0 and P1.1 should be set to "0" if no external pullups are used, or set to "1" if external pullups are used.

Programming The Flash

The AT89C2051 is shipped with the 2K bytes of on-chip PEROM code memory array in the erased state (i.e., contents = FFH) and ready to be programmed. The code memory array is programmed one byte at a time. *Once the array is programmed, to re-program any non-blank byte, the entire memory array needs to be erased electrically.*

Internal Address Counter: The AT89C2051 contains an internal PEROM address counter which is always reset to 000H on the rising edge of RST and is advanced by applying a positive going pulse to pin XTAL1.

Programming Algorithm: To program the AT89C2051, the following sequence is recommended.

1. Power-up sequence:
   Apply power between V_{CC} and GND pins
   Set RST and XTAL1 to GND
2. Set pin RST to "H"
   Set pin P3.2 to "H"
3. Apply the appropriate combination of "H" or "L" logic levels to pins P3.3, P3.4, P3.5, P3.7 to select one of the programming operations shown in the PEROM Programming Modes table.

To Program and Verify the Array:

4. Apply data for Code byte at location 000H to P1.0 to P1.7.
5. Raise RST to 12V to enable programming.
6. Pulse P3.2 once to program a byte in the PEROM array or the lock bits. The byte-write cycle is self-timed and typically takes 1.2 ms.
7. To verify the programmed data, lower RST from 12V to logic "H" level and set pins P3.3 to P3.7 to the appropiate levels. Output data can be read at the port P1 pins.
8. To program a byte at the next address location, pulse XTAL1 pin once to advance the internal address counter. Apply new data to the port P1 pins.
9. Repeat steps 5 through 8, changing data and advancing the address counter for the entire 2K bytes array or until the end of the object file is reached.
10. Power-off sequence:
    set XTAL1 to "L"
    set RST to "L"
    Turn V_{CC} power off

$\overline{\text{Data}}$ Polling: The AT89C2051 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P1.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The Progress of byte programming can also be monitored by the RDY/$\overline{\text{BSY}}$ output signal. Pin P3.1 is pulled low after P3.2 goes High during programming to indicate BUSY. P3.1 is pulled High again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed code data can be read back via the data lines for verification:

1. Reset the internal address counter to 000H by bringing RST from "L" to "H".
2. Apply the appropriate control signals for Read Code data and read the output data at the port P1 pins.
3. Pulse pin XTAL1 once to advance the internal address counter.
4. Read the next code data byte at the port P1 pins.
5. Repeat steps 3 and 4 until the entire array is read.

The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire PEROM array (2K bytes) and the two Lock Bits are erased electrically by using the proper combination of control signals and by holding P3.2 low for 10 ms. The code array is written with all "1"s in the Chip Erase operation and must be executed before any non-blank memory byte can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 000H, 001H, and 002H, except that P3.5 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(001H) = 21H indicates 89C2051

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST/VPP	P3.2/$\overline{PROG}$	P3.3	P3.4	P3.5	P3.7
Write Code Data[1][3]		12V		L	H	H	H
Read Code Data[1]		H	H	L	L	H	H
Write Lock	Bit - 1	12V		H	H	H	H
	Bit - 2	12V		H	H	L	L
Chip Erase		12V	(2)	H	L	L	L
Read Signature Byte		H	H	L	L	L	L

Notes:
1. The internal PEROM address counter is reset to 000H on the rising edge of RST and is advanced by a positive pulse at XTAL 1 pin.
2. Chip Erase requires a 10 ms $\overline{PROG}$ pulse.
3. P3.1 is pulled Low during programming to indicate RDY/$\overline{BSY}$.

Figure 3. Programming the Flash Memory

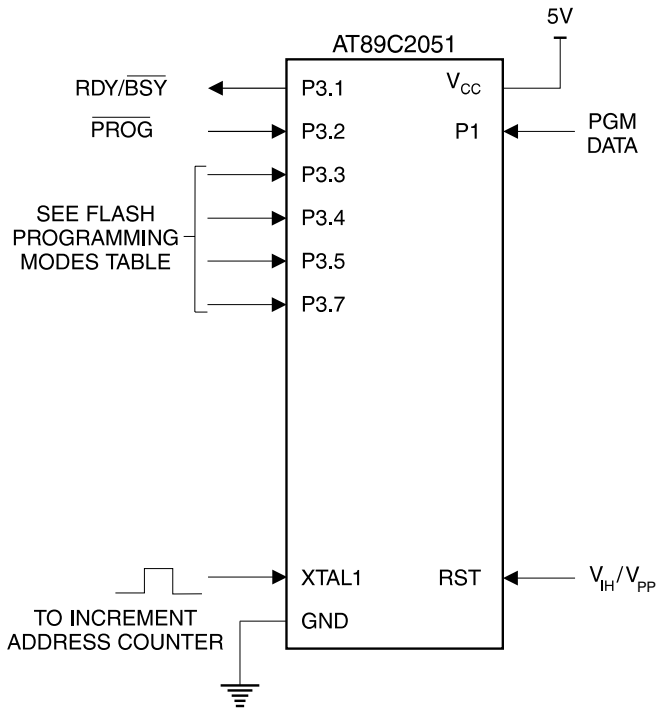
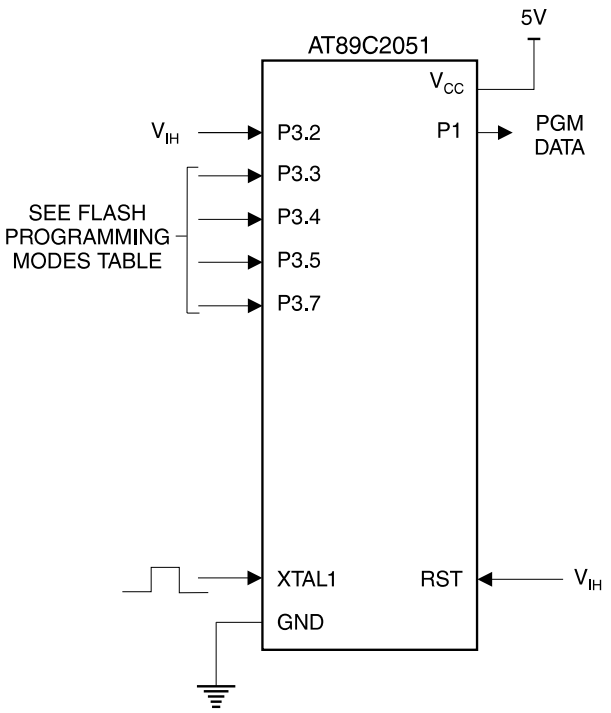


Figure 4. Verifying the Flash Memory



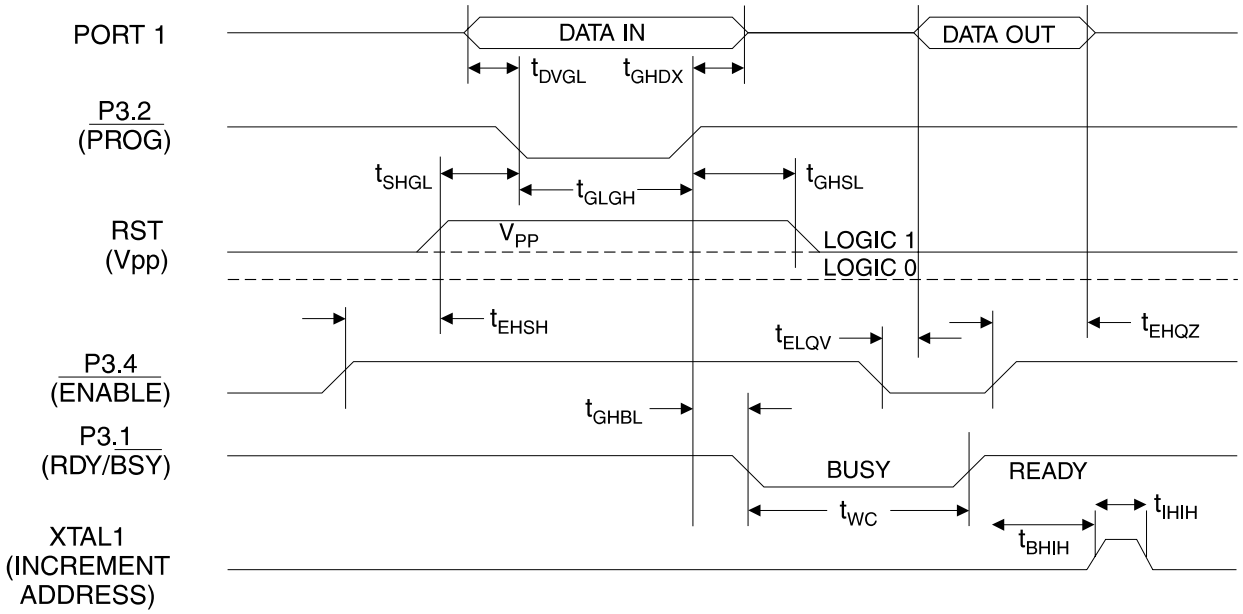
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		250	µA
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	1.0		µs
t_{GHDX}	Data Hold after $\overline{PROG}$	1.0		µs
t_{EHSH}	P3.4 ($\overline{ENABLE}$) High to V_{PP}	1.0		µs
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		1.0	µs
t_{EHQZ}	Data Float after $\overline{ENABLE}$	0	1.0	µs
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		50	ns
t_{WC}	Byte Write Cycle Time		2.0	ms
t_{BHIH}	RDY/$\overline{BSY}$\ to Increment Clock Delay	1.0		µs
t_{IHIL}	Increment Clock High	200		ns

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	25.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

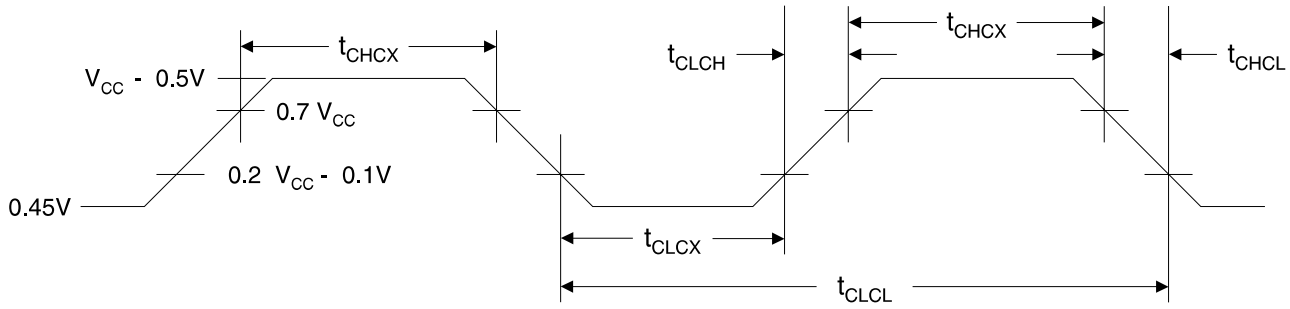
DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.0V to 6.0V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.2 V_{CC} - 0.1	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1, 3)	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 2.7V		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3)	I_{OH} = -80 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ± 10%		-750	µA
I_{LI}	Input Leakage Current (Port P1.0, P1.1)	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz, V_{CC} = 6V/3V		15/5.5	mA
		Idle Mode, 12 MHz, V_{CC} = 6V/3V P1.0 & P1.1 = 0V or V_{CC}		5/1	mA
	Power-down Mode(2)	V_{CC} = 6V P1.0 & P1.1 = 0V or V_{CC}		100	µA
		V_{CC} = 3V P1.0 & P1.1 = 0V or V_{CC}		20	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 20 mA
   Maximum total I_{OL} for all output pins: 80 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

External Clock Drive Waveforms



External Clock Drive

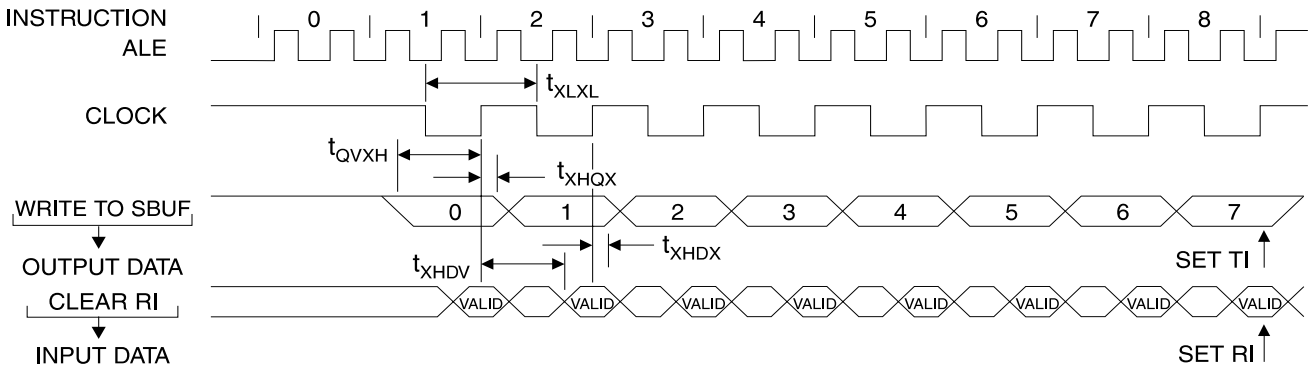
Symbol	Parameter	V_{CC} = 2.7V to 6.0V		V_{CC} = 4.0V to 6.0V		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	12	0	24	MHz
t_{CLCL}	Clock Period	83.3		41.6		ns
t_{CHCX}	High Time	30		15		ns
t_{CLCX}	Low Time	30		15		ns
t_{CLCH}	Rise Time		20		20	ns
t_{CHCL}	Fall Time		20		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

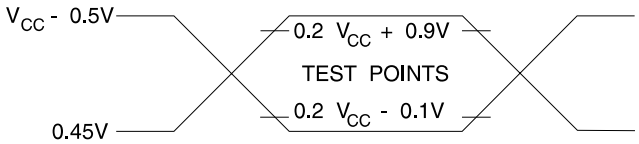
V_{CC} = 5.0V ± 20%; Load Capacitance = 80 pF

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

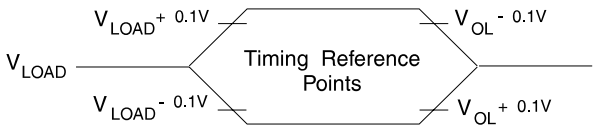


AC Testing Input/Output Waveforms(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

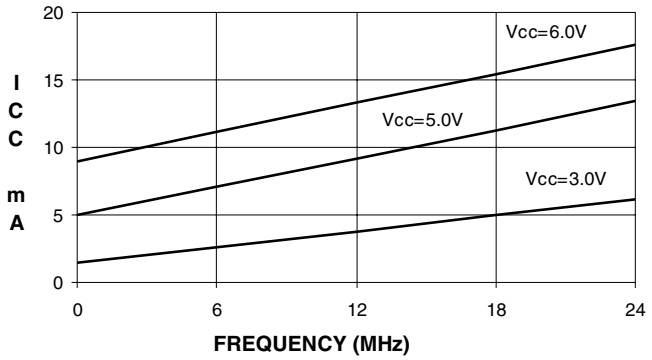
Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change frothe loaded V_{OH}/V_{OL} level occurs.

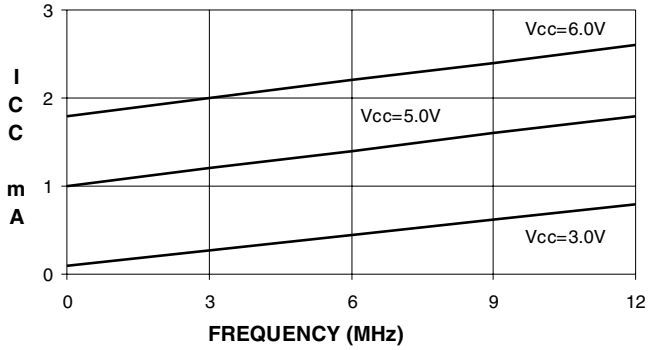
AT89C2051

TYPICAL ICC - ACTIVE (85°C)



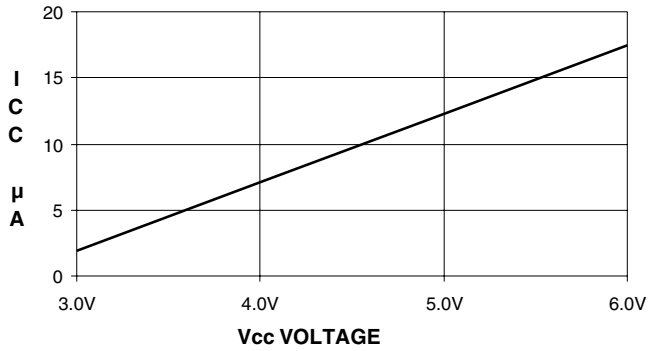
AT89C2051

TYPICAL ICC - IDLE (85°C)



AT89C2051

TYPICAL ICC vs. VOLTAGE- POWER DOWN (85°C)



Notes:
1. XTAL1 tied to GND for I_{CC} (power-down)
2. P.1.0 and P1.1 = V_{CC} or GND
3. Lock bits programmed

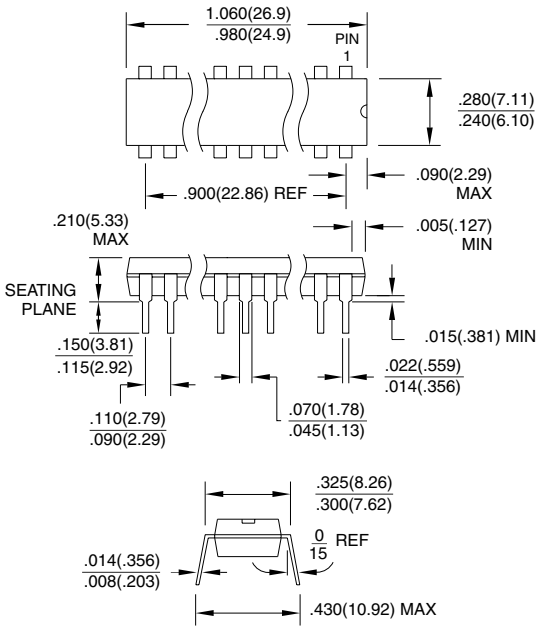
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	2.7V to 6.0V	AT89C2051-12PC AT89C2051-12SC	20P3 20S	Commercial (0°C to 70°C)
		AT89C2051-12PI AT89C2051-12SI	20P3 20S	Industrial (-40°C to 85°C)
24	4.0V to 6.0V	AT89C2051-24PC AT89C2051-24SC	20P3 20S	Commercial (0°C to 70°C)
		AT89C2051-24PI AT89C2051-24SI	20P3 20S	Industrial (-40°C to 85°C)

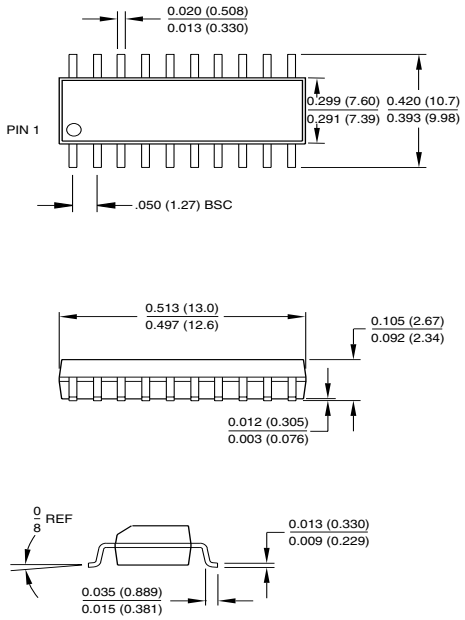
Package Type	
20P3	20-lead, 0.300” Wide, Plastic Dual In-line Package (PDIP)
20S	20-lead, 0.300” Wide, Plastic Gull Wing Small Outline (SOIC)

Packaging Information

20P3, 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 AD



20S, 20-lead, 0.300" Wide, Plastic Gull WIng Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



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0368E–02/00/xM

LM358, LM258, LM2904, LM2904A, LM2904V, NCV2904

Single Supply Dual Operational Amplifiers

Utilizing the circuit designs perfected for Quad Operational Amplifiers, these dual operational amplifiers feature low power drain, a common mode input voltage range extending to ground/V_{EE}, and single supply or split supply operation. The LM358 series is equivalent to one−half of an LM324.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V, with quiescent currents about one−fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

Features

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation
- Pb−Free Packages are Available
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

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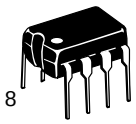
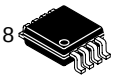


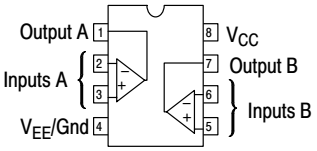
PDIP−8
N, AN, VN SUFFIX
CASE 626

SOIC−8
D, VD SUFFIX
CASE 751



Micro8™
DMR2 SUFFIX
CASE 846A

PIN CONNECTIONS

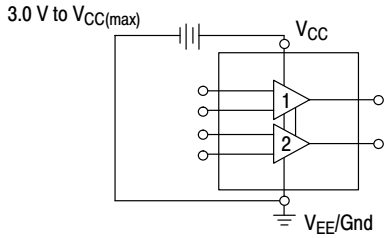


ORDERING INFORMATION

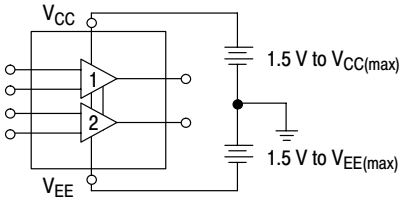
See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 11 of this data sheet.



Single Supply



Split Supplies

Figure 1.

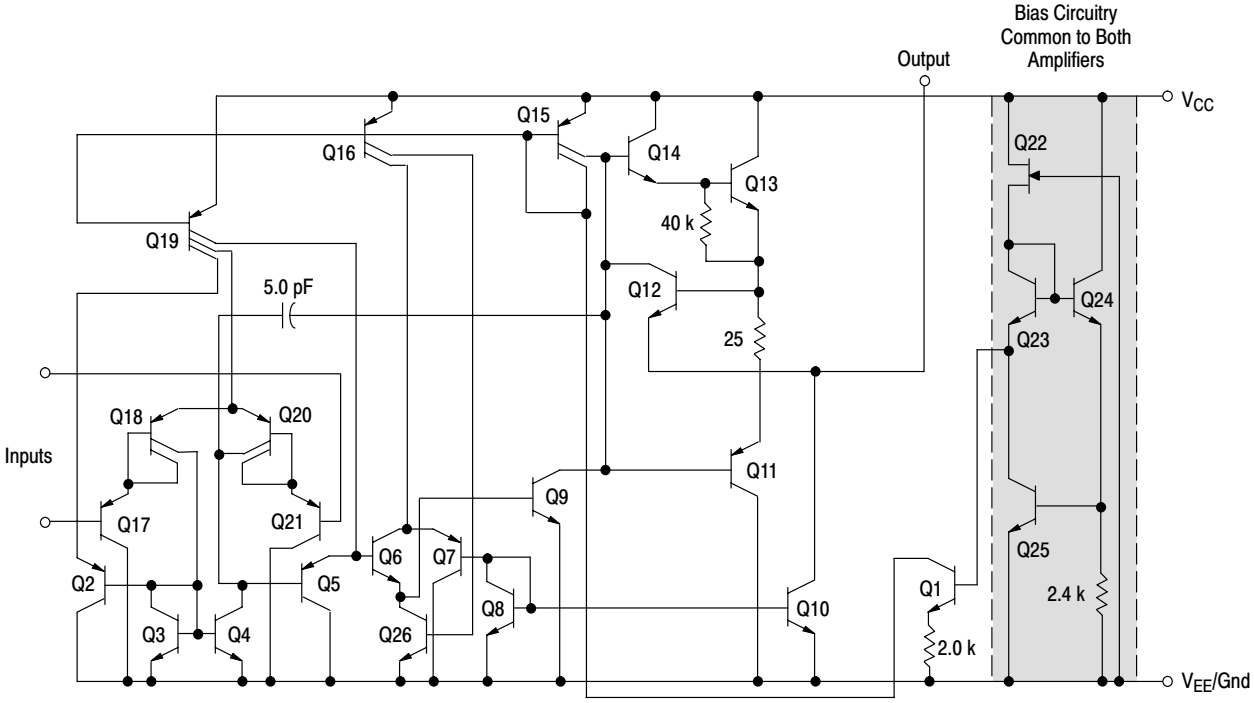


Figure 2. Representative Schematic Diagram
(One−Half of Circuit Shown)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	Vdc
Input Common Mode Voltage Range (Note 2)	V_{ICR}	−0.3 to 32	Vdc
Output Short Circuit Duration	t_{SC}	Continuous	
Junction Temperature	T_J	150	°C
Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	238	°C/W
Storage Temperature Range	T_{stg}	−55 to +125	°C
ESD Protection at any Pin Human Body Model Machine Model	V_{esd}	 2000 200	V
Operating Ambient Temperature Range LM258 LM358 LM2904/LM2904A LM2904V, NCV2904 (Note 4)	T_A	 −25 to +85 0 to +70 −40 to +105 −40 to +125	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Split Power Supplies.
2. For Supply Voltages less than 32 V the absolute maximum input voltage is equal to the supply voltage.
3. $R_{\theta JA}$ for Case 846A.
4. *NCV2904 is qualified for automotive use.*

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LM258			LM358			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V, V_{IC} = 0 V to V_{CC} −1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω	V_{IO}							mV
T_A = 25°C		−	2.0	5.0	−	2.0	7.0	
$T_A = T_{high}$ (Note 5)		−	−	7.0	−	−	9.0	
$T_A = T_{low}$ (Note 5)		−	−	7.0	−	−	9.0	
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 5)	$\Delta V_{IO}/\Delta T$	−	7.0	−	−	7.0	−	μV/°C
Input Offset Current	I_{IO}	−	3.0	30	−	5.0	50	nA
$T_A = T_{high}$ to T_{low} (Note 5)		−	−	100	−	−	150	
Input Bias Current	I_{IB}	−	−45	−150	−	−45	−250	
$T_A = T_{high}$ to T_{low} (Note 5)		−	−50	−300	−	−50	−500	
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low} (Note 5)	$\Delta I_{IO}/\Delta T$	−	10	−	−	10	−	pA/°C
Input Common Mode Voltage Range (Note 6), V_{CC} = 30 V	V_{ICR}	0	−	28.3	0	−	28.3	V
V_{CC} = 30 V, $T_A = T_{high}$ to T_{low}		0	−	28	0	−	28	
Differential Input Voltage Range	V_{IDR}	−	−	V_{CC}	−	−	V_{CC}	V
Large Signal Open Loop Voltage Gain	A_{VOL}							V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,		50	100	−	25	100	−	
$T_A = T_{high}$ to T_{low} (Note 5)		25	−	−	15	−	−	
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	−	−120	−	−	−120	−	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	−	65	70	−	dB
Power Supply Rejection	PSR	65	100	−	65	100	−	dB
Output Voltage−High Limit $T_A = T_{high}$ to T_{low} (Note 5)	V_{OH}							V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	−	3.3	3.5	−	
V_{CC} = 30 V, R_L = 2.0 kΩ		26	−	−	26	−	−	
V_{CC} = 30 V, R_L = 10 kΩ		27	28	−	27	28	−	
Output Voltage−Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low} (Note 5)	V_{OL}	−	5.0	20	−	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	−	20	40	−	mA
Output Sink Current	I_{O-}							
V_{ID} = −1.0 V, V_{CC} = 15 V		10	20	−	10	20	−	mA
V_{ID} = −1.0 V, V_O = 200 mV		12	50	−	12	50	−	μA
Output Short Circuit to Ground (Note 7)	I_{SC}	−	40	60	−	40	60	mA
Power Supply Current (Total Device) $T_A = T_{high}$ to T_{low} (Note 5)	I_{CC}							mA
V_{CC} = 30 V, V_O = 0 V, R_L = ∞		−	1.5	3.0	−	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		−	0.7	1.2	−	0.7	1.2	

5. LM258: T_{low} = −25°C, T_{high} = +85°C; LM358: T_{low} = 0°C, T_{high} = +70°C
   LM2904/LM2904A: T_{low} = −40°C, T_{high} = +105°C; LM2904V & NCV2904: T_{low} = −40°C, T_{high} = +125°C
   NCV2904 is qualified for automotive use.
6. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} − 1.7 V.
7. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LM2904			LM2904A			LM2904V, NCV2904			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V, V_{IC} = 0 V to V_{CC} −1.7 V, $V_O \simeq$ 1.4 V, R_S = 0 Ω	V_{IO}										mV
T_A = 25°C		−	2.0	7.0	−	2.0	7.0	−	−	7.0	
$T_A = T_{high}$ (Note 8)		−	−	10	−	−	10	−	−	13	
$T_A = T_{low}$ (Note 8)		−	−	10	−	−	10	−	−	10	
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 8)	$\Delta V_{IO}/\Delta T$	−	7.0	−	−	7.0	−	−	7.0	−	μV/°C
Input Offset Current	I_{IO}	−	5.0	50	−	5.0	50	−	5.0	50	nA
$T_A = T_{high}$ to T_{low} (Note 8)		−	45	200	−	45	200	−	45	200	
Input Bias Current	I_{IB}	−	−45	−250	−	−45	−100	−	−45	−250	
$T_A = T_{high}$ to T_{low} (Note 8)		−	−50	−500	−	−50	−250	−	−50	−500	
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low} (Note 8)	$\Delta I_{IO}/\Delta T$	−	10	−	−	10	−	−	10	−	pA/°C
Input Common Mode Voltage Range (Note 9), V_{CC} = 30 V	V_{ICR}	0	−	24.3	0	−	24.3	0	−	24.3	V
V_{CC} = 30 V, $T_A = T_{high}$ to T_{low}		0	−	24	0	−	24	0	−	24	
Differential Input Voltage Range	V_{IDR}	−	−	V_{CC}	−	−	V_{CC}	−	−	V_{CC}	V
Large Signal Open Loop Voltage Gain	A_{VOL}										V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,		25	100	−	25	100	−	25	100	−	
$T_A = T_{high}$ to T_{low} (Note 8)		15	−	−	15	−	−	15	−	−	
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	−	−120	−	−	−120	−	−	−120	−	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	50	70	−	50	70	−	50	70	−	dB
Power Supply Rejection	PSR	50	100	−	50	100	−	50	100	−	dB
Output Voltage−High Limit $T_A = T_{high}$ to T_{low} (Note 8)	V_{OH}										V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	−	3.3	3.5	−	3.3	3.5	−	
V_{CC} = 30 V, R_L = 2.0 kΩ		22	−	−	22	−	−	22	−	−	
V_{CC} = 30 V, R_L = 10 kΩ		23	24	−	23	24	−	23	24	−	
Output Voltage−Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low} (Note 8)	V_{OL}	−	5.0	20	−	5.0	20	−	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	−	20	40	−	20	40	−	mA
Output Sink Current	I_{O-}										
V_{ID} = −1.0 V, V_{CC} = 15 V		10	20	−	10	20	−	10	20	−	mA
V_{ID} = −1.0 V, V_O = 200 mV		−	−	−	−	−	−	−	−	−	μA
Output Short Circuit to Ground (Note 10)	I_{SC}	−	40	60	−	40	60	−	40	60	mA
Power Supply Current (Total Device) $T_A = T_{high}$ to T_{low} (Note 8)	I_{CC}										mA
V_{CC} = 30 V, V_O = 0 V, R_L = ∞		−	1.5	3.0	−	1.5	3.0	−	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		−	0.7	1.2	−	0.7	1.2	−	0.7	1.2	

8. LM258: T_{low} = −25°C, T_{high} = +85°C; LM358: T_{low} = 0°C, T_{high} = +70°C
   LM2904/LM2904A: T_{low} = −40°C, T_{high} = +105°C; LM2904V & NCV2904: T_{low} = −40°C, T_{high} = +125°C
   NCV2904 is qualified for automotive use.
9. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} − 1.7 V.
10. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

CIRCUIT DESCRIPTION

The LM358 series is made using two internally compensated, two−stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single−ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal−voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

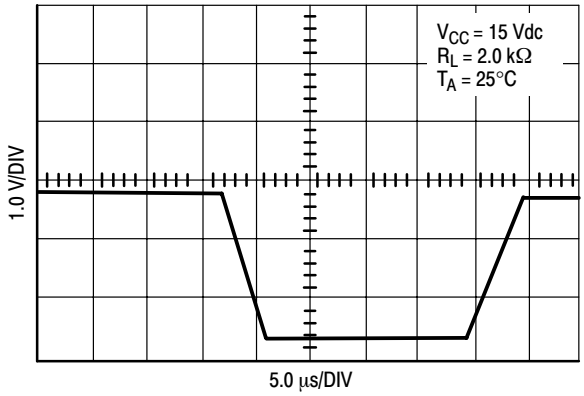


Figure 3. Large Signal Voltage Follower Response

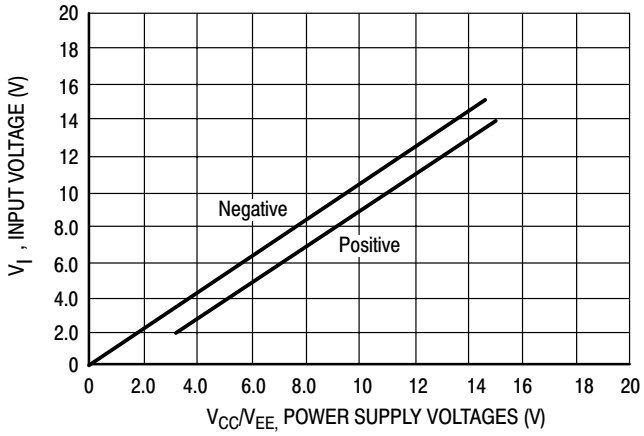


Figure 4. Input Voltage Range

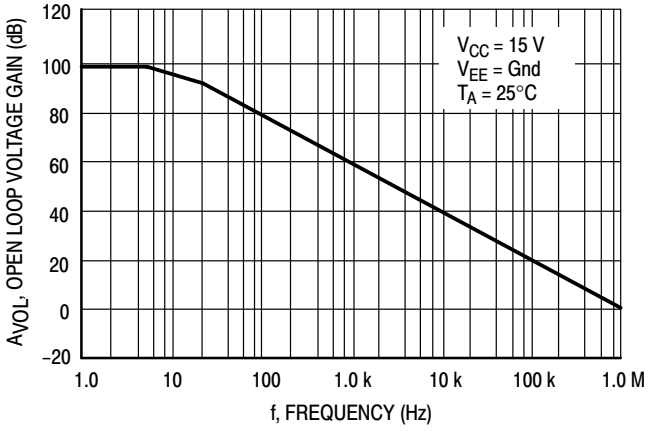


Figure 5. Large−Signal Open Loop Voltage Gain

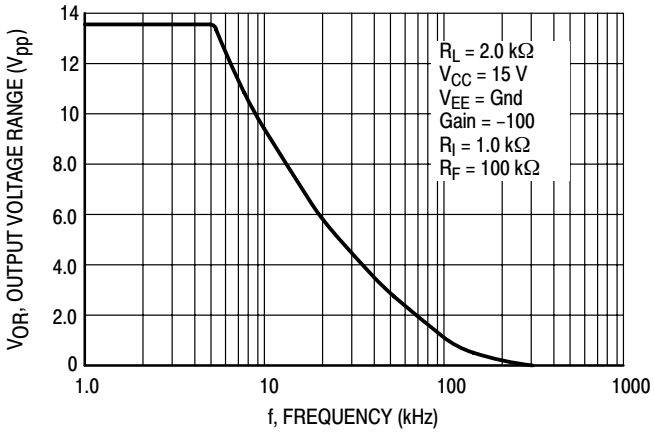


Figure 6. Large−Signal Frequency Response

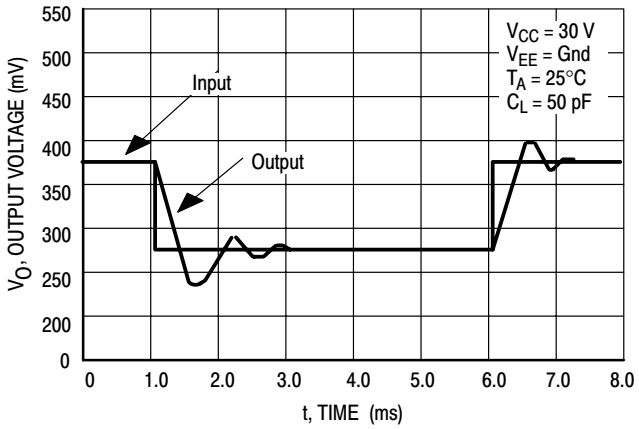


Figure 7. Small Signal Voltage Follower Pulse Response (Noninverting)

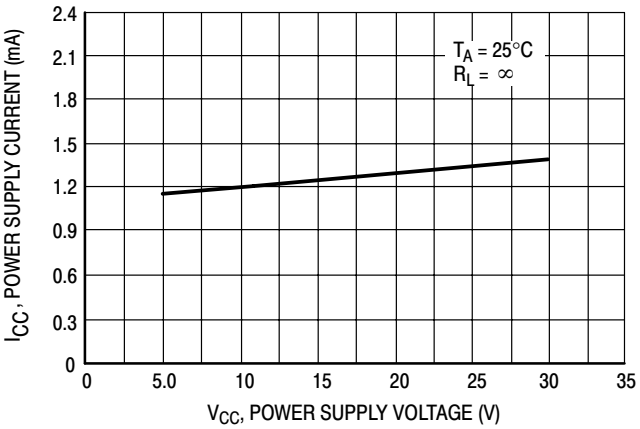


Figure 8. Power Supply Current versus Power Supply Voltage

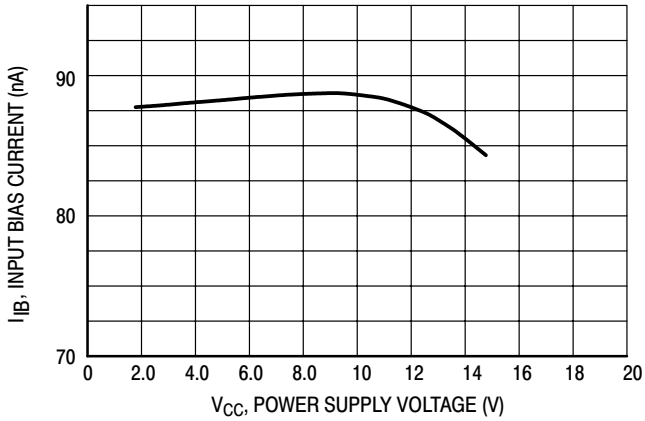


Figure 9. Input Bias Current versus Supply Voltage

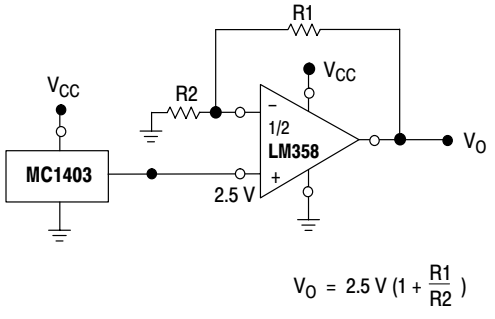


Figure 10. Voltage Reference

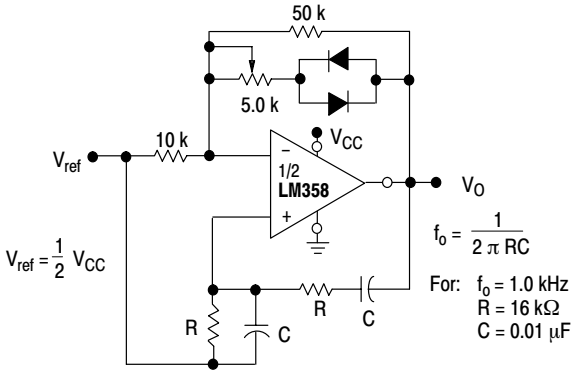


Figure 11. Wien Bridge Oscillator

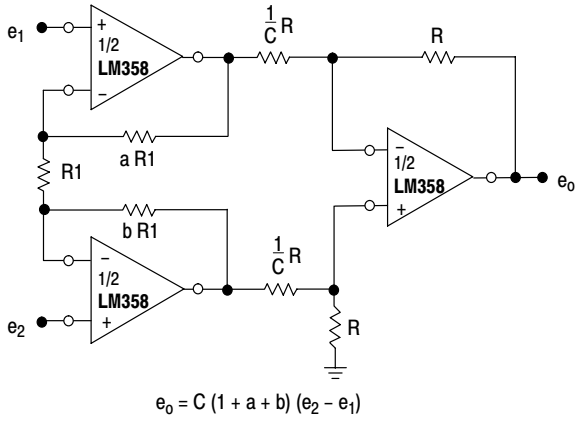


Figure 12. High Impedance Differential Amplifier

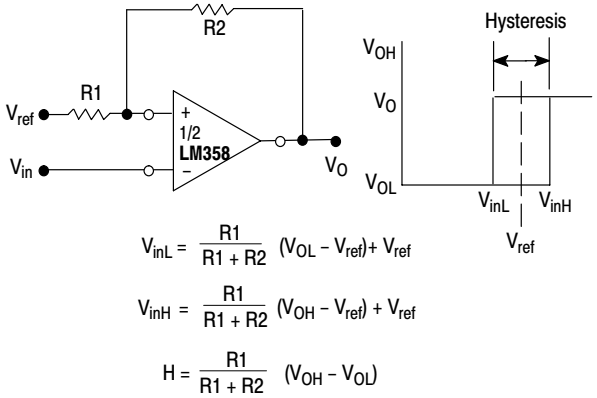


Figure 13. Comparator with Hysteresis

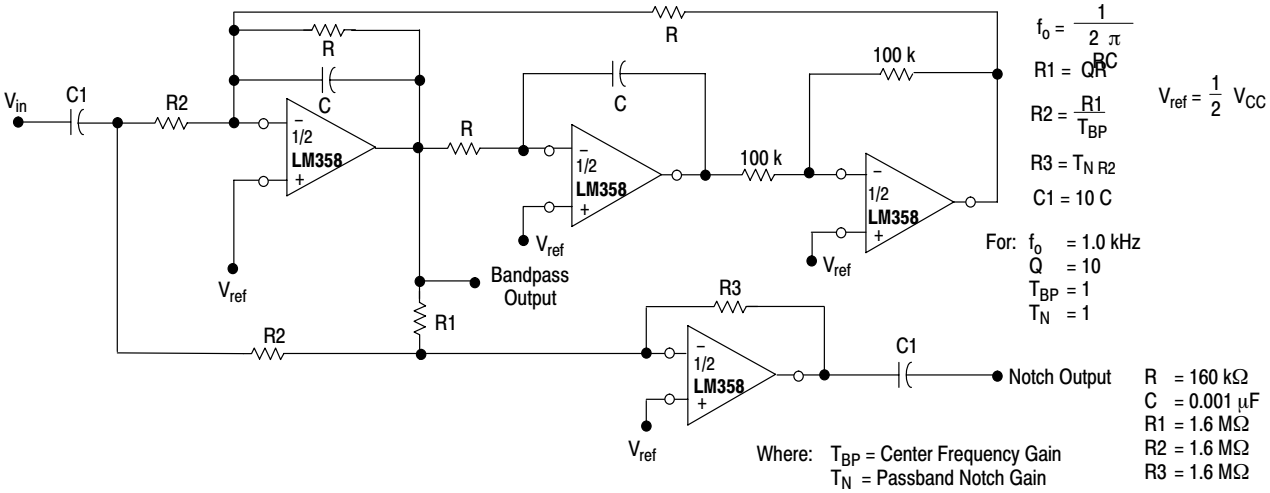
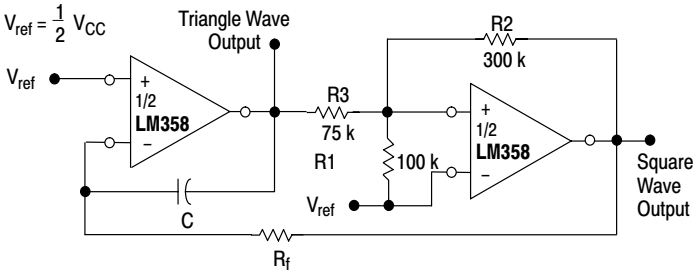
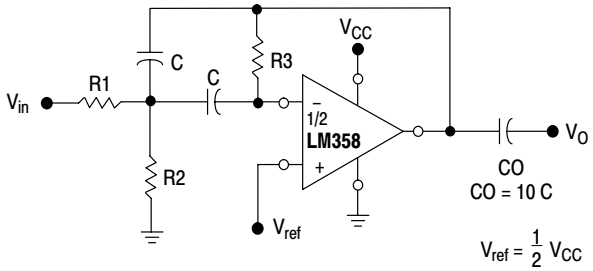


Figure 14. Bi−Quad Filter



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if, } R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 15. Function Generator



Given: f_o = center frequency

$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \frac{Q}{\pi\, f_o\, C}$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier. $\frac{Q_o\, f_o}{BW} < 0.1$

Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Figure 16. Multiple Feedback Bandpass Filter

ORDERING INFORMATION

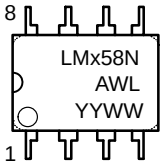
Device	Operating Temperature Range	Package	Shipping†
LM358D	0°C to +70°C	SOIC−8	98 Units/Rail
LM358DR2		SOIC−8	2500 Tape & Reel
LM358DR2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
LM358DMR2		Micro8	4000 Tape & Reel
LM358DMR2G		Micro8 (Pb−Free)	4000 Tape & Reel
LM358N		PDIP−8	50 Units/Rail
LM358NG		PDIP−8 (Pb−Free)	50 Units/Rail
LM258D	−25°C to +85°C	SOIC−8	98 Units/Rail
LM258DR2		SOIC−8	2500 Tape & Reel
LM258DR2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
LM258DMR2		Micro8	4000 Tape & Reel
LM258N		PDIP−8	50 Units/Rail
LM2904D	−40°C to +105°C	SOIC−8	98 Units/Rail
LM2904DR2		SOIC−8	2500 Tape & Reel
LM2904DR2G		SOIC−8 (Pb−Free)	2500 Tape & Reel
LM2904DMR2		Micro8	2500 Tape & Reel
LM2904DMR2G		Micro8 (Pb−Free)	2500 Tape & Reel
LM2904N		PDIP−8	50 Units/Rail
LM2904ADMR2		Micro8	4000 Tape & Reel
LM2904AN		PDIP−8	50 Units/Rail
LM2904VD	−40°C to +125°C	SOIC−8	98 Units/Rail
LM2904VDG		SOIC−8 (Pb−Free)	98 Units/Rail
LM2904VDR2		SOIC−8	2500 Tape & Reel
LM2904VDMR2		Micro8	4000 Tape & Reel
LM2904VN		PDIP−8	50 Units/Rail
NCV2904DR2*		SOIC−8	2500 Tape & Reel
NCV2904DMR2*		Micro8	4000 Tape & Reel

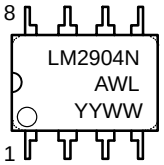
*NCV2904 is qualified for automotive use.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

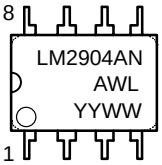
MARKING DIAGRAMS

PDIP−8
N SUFFIX
CASE 626

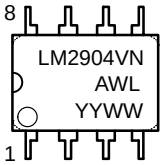




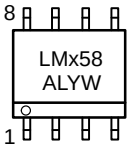
PDIP−8
AN SUFFIX
CASE 626

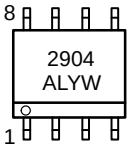


PDIP−8
VN SUFFIX
CASE 626

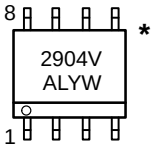


SOIC−8
D SUFFIX
CASE 751

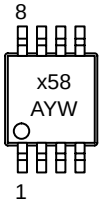


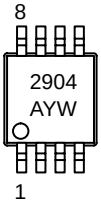


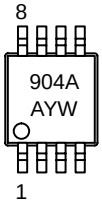
SOIC−8
VD SUFFIX
CASE 751

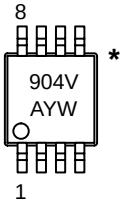


Micro8
DMR2 SUFFIX
CASE 846A







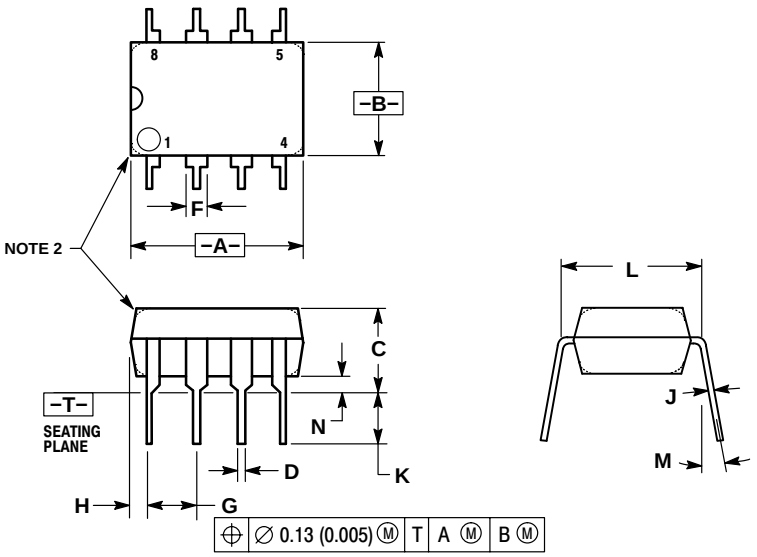


x	= 2 or 3
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

*This diagram also applies to NCV2904

PACKAGE DIMENSIONS

PDIP−8
N, AN, VN SUFFIX
CASE 626−05
ISSUE L

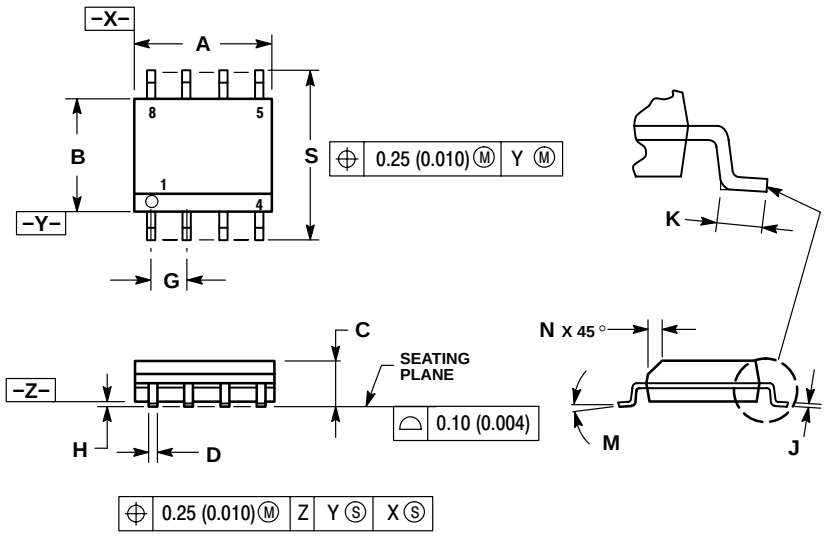


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PACKAGE DIMENSIONS

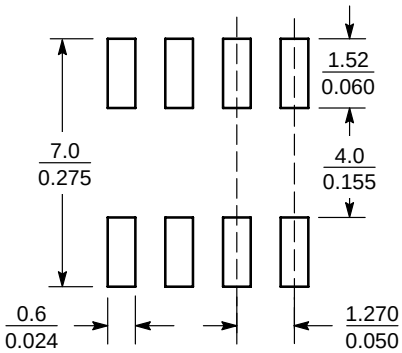
SOIC−8
D, VD SUFFIX
CASE 751−07
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

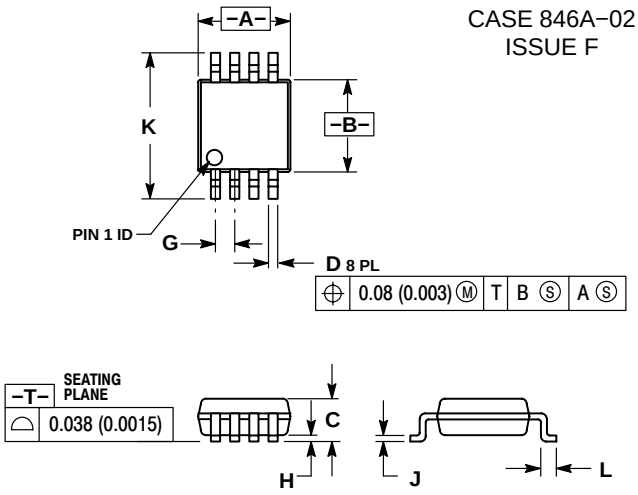


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

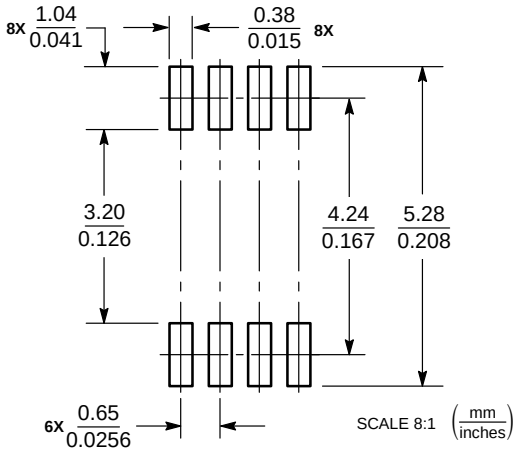
Micro8
DMR2 SUFFIX
CASE 846A−02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



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